Yiyang LING

Email | Homepage | Github

Area of Interest

My research interest lies in robotics and computer vision. Currently, I am working on generating rich manipulation tasks for training language-conditioned multitask policies with Large Language Models.

Education

Shanghai Jiao Tong University *Shanghai, China*

Major in Computer Science (ACM Honors Class) *Sept 2020 - Present*

- **GPA:** 3.74/4.3, Ranking: 14/35
- **Courses:** Scientific computing (99/100), Math Tools in Computer Science (99/100), Computational Complexity (98/100), Deep Learning and Its Applications (97/100), Model Checking (96/100)

Research Experience

University of California San Diego *San Diego, US*

Visiting Undergraduate, advised by Prof. **Xiaolong Wang** *Jun 2023 - Present*

- Designing a novel simulation task generation pipeline through Large Language Models to generate achievable and diverse manipulation tasks.
- Leveraging the generated tasks for training multitask policies and evaluating their generalization capabilities in both simulation and real world.
- Exploiting the grounding and coding ability of Large Language Models.

Shanghai Jiao Tong University *Shanghai, China*

Research Assistant, advised by Prof. **Cewu Lu** *Sept 2022 - Feb 2023*

- Focused on few-shot or zero-shot methods for detection of deformable objects.

Course Projects

Quantum Inspired Tensorized Cross-Network Embedding

Project for Deep Learning and Its Application *Fall 2022*

- Proposed a scalable tensorized cross-network embedding method based on contrastive learning by introducing the utilization of CP Decomposition and intra/inter-network sub-embeddings.
- Achieved to save storage space and accelerate embedding learning simultaneously in a unified training pipeline.

Compiler for Mx*

Project for Compiler Design and Implementation *Spring 2022*

- Designed and implemented a compiler from Mx*, a simplified programming language similar to C++, to RV32I instructions.

RISC-V CPU

Project for Computer Architecture *Fall 2021*

- Designed and implemented a five-stage CPU pipeline supporting most part of RV32I Instruction set using Verilog.

Publications

GenSim: Generating Robotic Simulation Tasks via Large Language Models
Lirui Wang, **Yiyang Ling***, Zhecheng Yuan*, Mohit Shridhar, Chen Bao, Yuzhe Qin, Bailin Wang, Huazhe Xu, Xiaolong Wang
In submission

TC-CNE: Scalable and Efficient Contrastive Cross-Network Embedding via Tensorized Representation
Hao Xiong, **Yiyang Ling**, Junchi Yan
In submission

Work Experience

Shanghai Jiao Tong University *Shanghai, China*

Teaching Assistant of **Algorithm Design and Analysis** *Spring 2023*

Awards and Honors

2020-2023 **Scholarship,** Zhiyuan College Honors Scholarship (Top 5% in SJTU each year) *Shanghai Jiao Tong University*

2020-2023 **Scholarship,** Scholarship for Outstanding Undergraduates *Shanghai Jiao Tong University*

Skills

Programming Python, C++, Rust, Java, Verilog.

Miscellaneous LaTeX, SQL, Git, Matlab.

Language English, Chinese.