Joshua Gabriel Dela Rosa

joshua04@yonsei.ac.kr | +82-1-7742-3348
github.com/dsa-shua

TECHNICAL SKILLS

- Programming: C/C++, Verilog/System Verilog, Python, Shell Script, Makefile, MATLAB, CUDA
- Hardware: Xilinx PYNQ-Z2 FPGA, Arduino, ESP32, Raspberry Pi
- Software: Xilinx Vivado and Vitis, HSPICE, Logism, Git/Github, Verilator, LTSpice, PSpice, Chipyard (Chisel, RocketChip)
- Operating Systems: Linux/UNIX (macOS)

EDUCATION

Yonsei University Sept. 2, 2019 - Feb. 26, 2024
- Bachelor of Science in Electrical and Electronics Engineering Seoul, South Korea
- Major in Computer-VLSI, and Electrical Power Engineering
- GPA: 3.54 / 4.3

MOST RECENT PROJECTS

Xilinx FPGA-Based Systolic Array Hardware and Firmware Design Feb. 2024
- Designed and implemented an output stationary systolic array for the Xilinx PYNQ-Z2 FPGA board using Xilinx Vivado written in Verilog/System Verilog and wrote the firmware in Xilinx Vitis to send inputs, instructions and read results of the PL fabric using the built-in ARM processor.
- The hardware design involves a base half-word processing element (PE) cell that performs a MAC operation. The array is arranged in an 8x8 tile where the edge PE cells are interfaced with a parallel shift register that pipelines and shifts the inputs required for performing matrix multiplication. A small memory and a controller that receives instructions from the ARM processor is included which manages the flow of data and operation of the hardware.
- A firmware is used to control the PL fabric by setting up the AXI GPIO and interrupts (to let the processor know matrix multiplication is done) needed by the PL fabric. The firmware includes a library of APIs that users can utilize to send matrices to the FPGA, perform the operation and read the results.

Xilinx FPGA-Based Arcade Game May-Jun. 2023
- Designed and implemented a runner arcade game in Xilinx PYNQ-Z2 FPGA board. The main objective is to run for a certain amount of distance while collecting coins and avoiding obstacles along the way. Each coin collected adds a score while collision per barrier reduces life points by 1. The game ends when the user runs out of life points or if the penguin runs a certain amount of distance.
- The Processing Logic (PL) part of the board consists of a state-machine which interfaces with the graphics generator, coin and barrier generators, and the life-points and score trackers which manages the flow of the game. The state-machine also receives inputs from the user through the GPIO buttons and switches to control the penguin runner. The sprite generators for coins and barriers are constantly monitored by the state machine to check for collision with the penguin. The System Verilog code is written and verified using Xilinx Vivado suite.
- The Processing System (PS) part of the board handles the audio interface of the project. C/C++ code is used to send audio data to the audio codec for the background music. The sound effects for coin collection and barrier collision is achieved by interrupting the processor and sending the appropriate bits to indicate a coin or barrier collision. The programming and testing for the PS system is done using the Xilinx Vitis (SDK) program.

Laser Based Visual Light Communications Asynchronous PPM with Relay Protocol Sept.-Dec. 2023
- Designed a protocol and algorithm to solve the non-line of sight problem in visual light communications (VLC). The protocol involves other devices aside from the main TX and RX and reroute the signal to ensure that the message is received by the RX even if the main communication line is blocked.
- The project is realized using two ESP32 microcontrollers as main TX and the RELAY and an Arduino UNO as the main RX. Off-the-shelf CDS photoresistors and laser modules were used as main components for the VLC communication.
- The project is a team project with 3 other Korean students each with their own responsibilities who worked together with the professor and TA. The team communicated in Korean instead of English.

8-Bit Ripple Carry Adder Design Dec. 2023
- Designed an 8-bit RCA using HSPICE which used static CMOS logic using a 45 nm process. The design started from the design of a low-power high speed transistors for the inverters, AND gates, and XOR gates used in the design.
- The design achieved low power consumption and high speed performance due to transistor folding, shared diffusion, minimized interconnect, and careful placement of the logic gates during layout design.
- The design achieves half the power consumption required and about 1.6X faster than the specification due the techniques used to improve performance.

SKILL SET

- FPGA logic design and testing, timing analysis.
- Programming skills, problem solving skills.
- Digital and analog circuit design skills and implementation.

SOFT SKILLS

- Language Proficiency: English, Korean.
- Can work with people of different backgrounds and cultures.
- Problem solving skills, creativity, comfortable with challenging situations.