Joshua Gabriel Dela Rosa

joshua04@yonsei.ac.kr | +82-1-7742-3348
github.com/dsa-shua | linkedin.com/in/joshua-dela-rosa-1394a5234/

TECHNICAL SKILLS

- Programming: C/C++, Verilog/System Verilog, Scala (Chisel3), Python, Shell Script, Makefile, MATLAB, CUDA
- Hardware: Xilinx PYNQ-Z2 FPGA, Arduino, Raspberry Pi, ESP32
- Software: Xilinx Vivado and Vitis, HSPICE, Chipyard (Chisel, RocketChip), Logism, Git/Github, Verilator, LTSpice, PSpice
- Operating Systems: Linux/UNIX (macOS), Windows

EDUCATION

Yonsei University Sept. 2019 - Feb. 2024 (Expected)
- Bachelor of Science in Electrical and Electronics Engineering Seoul, South Korea
- Major in Computer-VLSI, and Electrical Power Engineering
- GPA: 3.54 / 4.3

PROJECTS (Most Recent)

Xilinx FPGA-Based Arcade Game Spring 2023
- Designed and implemented a runner arcade game in Xilinx PYNQ-Z2 FPGA board. The main objective is to run for a certain amount of distance while collecting coins and avoiding obstacles along the way. Each coin collected adds a score while collision per barrier reduces life points by 1. The game ends when the user runs out of life points or if the penguin runs a certain amount of distance.
- The Processing Logic (PL) part of the board consists of a state-machine which interfaces with the graphics generator, coin and barrier generators, and the life-points and score trackers which manages the flow of the game. The state-machine also receives inputs from the user through the GPIO buttons and switches to control the penguin runner. The sprite generators for coins and barriers are constantly monitored by the state machine to check for collision with the penguin. The System Verilog code is written and verified using Xilinx Vivado suite.
- The Processing System (PS) part of the board handles the audio interface of the project. C/C++ code is used to send audio data to the audio codec for the background music. The sound effects for coin collection and barrier collision is achieved by interrupting the processor and sending the appropriate bits to indicate a coin or barrier collision. The programming and testing for the PS system is done using the Xilinx Vitis (SDK) program.

Laser Based Visual Light Communications Asynchronous PPM with Relay Protocol Fall 2023
- Designed a protocol and algorithm to solve the non-line of sight problem in visual light communications (VLC). The protocol involves other devices aside from the main TX and RX and reroute the signal to ensure that the message is received by the RX even if the main communication line is blocked.
- The project is realized using two ESP32 microcontrollers as main TX and the RELAY and an Arduino UNO as the main RX. Off-the-shelf CDS photoresistors and laser modules were used as main components for the VLC communication.
- The project is a team project with 3 other Korean students each with their own responsibilities who worked together with the professor and TA. The team communicated in Korean instead of English.

8-Bit Ripple Carry Adder Design Fall 2023
- Designed an 8-bit RCA using HSPICE which used static CMOS logic using a 45 nm process. The design started from the design of a low-power high speed transistors for the inverters, AND gates, and XOR gates used in the design.
- The design achieved low power consumption and high speed performance due to transistor folding, shared diffusion, minimized interconnect, and careful placement of the logic gates during layout design.
- The design achieves half the power consumption required and about 1.6X faster than the specification due the techniques used to improve performance.

Three Stage Op-Amp Design Spring 2023
- Designed a three-stage op-amp (shunt-series amplifier with high CMRR, near ideal I/O impedances and high phase margin using a nulling resistor and Miller capacitor compensation.
- Design includes the use of a PMOS based differential to single-ended amplifier followed by a NMOS common source stage with a Class AB inverted CMOS push-pull stage simulated using PSpice.
- The design also achieves a gain of 10 in an inverting amplifier topology while achieving power consumption less than 1W.

ACTIVITY

Chisel Programming Summer 2023
- Attended a summer internship for learning about Chisel programming using Scala and learned about Berkeley's RocketChip, BOOM, and Gemmini accelerators and architectures.

SKILL SET

- Proficiency in embedded and computer systems, computer programming languages, hardware systems.
- Proficiency in both digital and analog circuit design.

SOFT SKILLS

- Language Proficiency: English, Korean.
- Can work with people of different backgrounds and cultures.
- Problem solving skills, creativity, comfortable with challenging situations.