Advanced Substrate Design for Resolving Random Orientation Challenges in LED Chip Integration

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ABSTRACT

The Fluidic Self-Assembly process enables the mass assembly of LED chips; however, when the P/N contact orientations are randomly arranged, it can be challenging to supply power effectively. In conventional methods, this issue has been addressed by designing and using specially fabricated chips with indistinguishable electrode orientations. However, this approach requires additional fabrication steps, reducing overall efficiency. To overcome this limitation, a structure is needed that allows stable power delivery while utilizing standard LED chips with predetermined P/N contact orientations. In this study, we propose a method that integrates Through-Silicon Via technology and Printed Circuit Board techniques to enable effective power supply to LED chips assembled through the Fluidic Self-Assembly process. This approach enhances the efficiency of Fluidic Self-Assembly research using conventional LED chips and provides a method for implementing LED displays without requiring additional fabrication steps.

Key Words: Fluidic Self- Assembly, Through-Silicon Via, Printed Circuit Board, Micro LED, Soldering, Electrode Alignment

1. Introduction

Micro LED displays refer to arrays of LED elements with dimensions of less than 100 μm in both width and height. Compared to OLED displays, they exhibit several advantages, including immunity to burn-in effects, longer lifespan, higher contrast ratio, faster response times, and superior energy efficiency. Due to these advantages, Micro LED displays, which consist of independently operating Micro LEDs, are gaining attention as a next-generation display technology. Currently, the primary methods for transferring LEDs onto display panels are Pick & Place and Transfer Printing techniques. Pick & Place: This method uses robotic equipment to mechanically position each LED pixel onto the display panel [1]. Transfer Printing: This involves forming red, green, and blue (RGB) pixels on separate wafers and transferring them onto a display substrate using a stamp-like tool [2,3]. However, the size of the stamp is constrained by the size of the growth wafer. These methods rely on serial processes and require a large number of transfer operations to fabricate Micro LED displays from LEDs smaller than 100 μm. This makes

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precise alignment of Micro-sized chips on substrates increasingly challenging [4-7]. Furthermore, the small size and lightweight nature of Micro LEDs exacerbate issues such as electrostatic forces and gravitational effects, making high-speed, precise transfers difficult to achieve. For these reasons, both methods are inefficient and unsuitable for the commercial production of Micro LED displays due to their high time consumption and technical limitations.

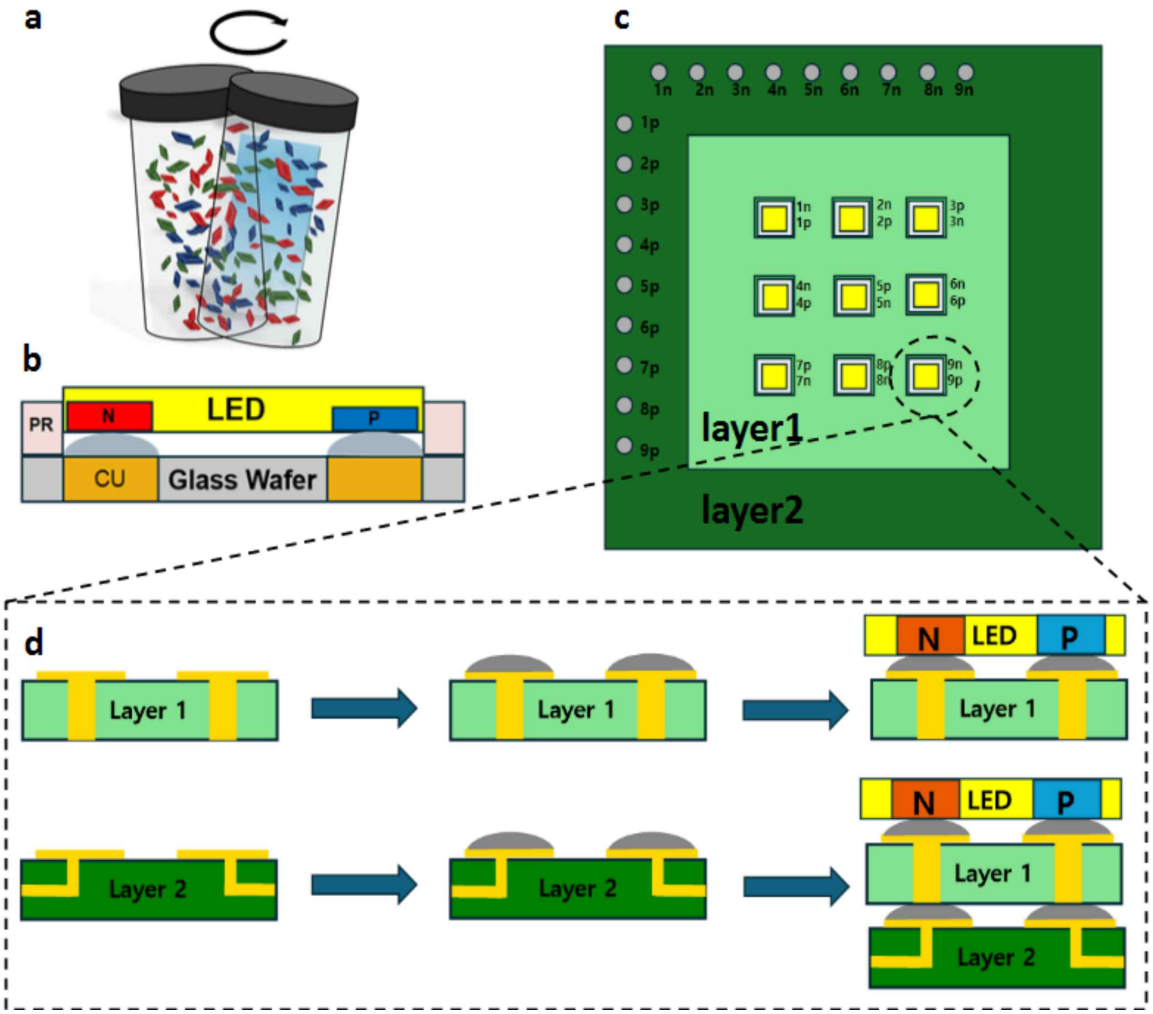

Fig. 1 Schematic of LED Transfer Design Utilizing FSA Concept and PCB.
(a) Conceptual schematic of the FSA assembly process. (b) Structure of the TSV substrate and the expected cross-sectional view after LED transfer. (c) Schematic showing the arrangement and placement of LEDs, as well as the structural connections between Layer 1 and Layer 2. (d) Enlarged view of Fig. 1c, illustrating the connection sequence

between LEDs and Layer 1, and between Layer 1 and Layer 2.

To commercialize and mass-produce Micro LED displays, it is essential to develop highly efficient and low-cost transfer technologies. In response to this need, the parallel transfer method known as FSA (Fluidic Self-Assembly) has been proposed. FSA is a method that uses the flow of fluids and surface tension to transfer particles or components onto a substrate in a parallel fashion [8,9]. In this process, a substrate pre-coated with an alloy at the assembly positions is combined with bulk LED chips that have metal pads. When the fluid flow and temperature are applied, the molten alloy solder on the substrate bonds with the gold pads of the chips, enabling assembly (Fig. 1a). In other words, FSA is a parallel process where multiple LEDs can be assembled onto the substrate simultaneously, making it well-suited for mass transfer and highly efficient in terms of time [1,10,11]. Due to these advantages, significant research has been conducted to commercialize Micro LED displays using FSA [8,9,12-15]. However, when using conventional LED chips with distinguishable P/N contact orientations in the FSA process, a critical issue arises. The direction of the P/N contacts becomes inconsistent and random due to the flow dynamics of the fluid, causing chips to be assembled on the substrate in irregular orientations. This inconsistency prevents the pre-formed wiring on the assembly substrate from aligning correctly, leading to operational issues.

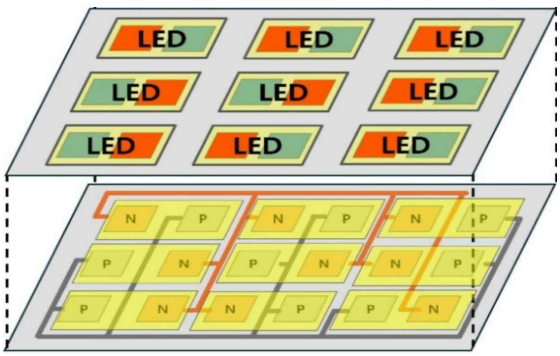

Fig. 2 Schematic of the PCB Circuit Design for Identifying and Powering LEDs with Randomly Transferred P/N Contacts.

To address this issue, previous FSA studies have resolved the wiring formation problem by designing and fabricating chips with symmetrical P/N contacts that lack directional orientation [8,9,13,14]. For example, there are circular chips where the P contact is located at the center, and the N contact is symmetrically positioned on both sides [13,14]. However, fabricating such specially designed chips for FSA research incurs high costs and time consumption, which can reduce research efficiency. Therefore, it is necessary to find a method that allows power to be applied to chips assembled with random contact orientations on the substrate after performing the FSA process using commercially available chips with directional P/N contacts instead of specially designed chips. Thus, we propose a new method that integrates TSV (Through-Silicon Via) technology and PCB (Printed Circuit Board) technology into the conventional FSA process. This method enables power application to LED chips assembled with random P/N orientations on the substrate. First, before assembling LED chips onto the substrate, a substrate with gold pads for electrode connections to the PCB layer is fabricated using TSV packaging technology. Then, the binding sites for the LED transfer are formed on the substrate using SU-8 (Negative PR). The SU-8 forms well-shaped structures tailored to the size and shape of the LED chips used in the experiment [15]. Following this, dip soldering is performed, and the LED chips are assembled into the formed structures via the FSA process. Fig. 1b shows the appearance of a single LED chip assembled on the fabricated TSV substrate. After completing the FSA process, the randomly oriented P/N contacts of each LED chip assembled in the binding sites are identified through image processing. Based on the identified P/N contact positions, a PCB with corresponding wiring is fabricated and connected to the TSV substrate to enable power activation of the LED chips (Fig. 2). This method allows the electrical

connection and illumination of standard LED chips with directional P/N contacts, rather than specially fabricated chips. To demonstrate the concept of electrical connection between two substrates using TSV and PCB technologies, the FSA process was applied, and LED chips of size 5×5 mm² were manually assembled. Binding sites of 6.5×6.5 mm² were designed on a PCB substrate with the same structure as the TSV, accommodating 9 LEDs arranged in a 3×3 configuration. Copper-plated via holes (3×3×2) were formed in positions corresponding to the P/N contacts of the chips to be assembled on the PCB substrate. LED chips were randomly oriented and assembled onto the fabricated TSV substrate. Based on the randomly oriented P/N contact positions, a PCB substrate of 11.5×11.5 cm² was designed and fabricated to form the wiring and supply power. Next, the two completed substrates were aligned, and an electrical connection was established between the TSV substrate with assembled chips and the power-supplying PCB substrate through soldering. Fig. 1c shows the overall assembly of the 9 LED chips and the two fabricated PCB substrates, while Fig. 1d provides an enlarged view of a single chip, illustrating the connection sequence between LED-Layer 1 and Layer 1-Layer 2. After establishing the electrical connection, power was applied, and the LEDs were successfully illuminated (Fig. 4).

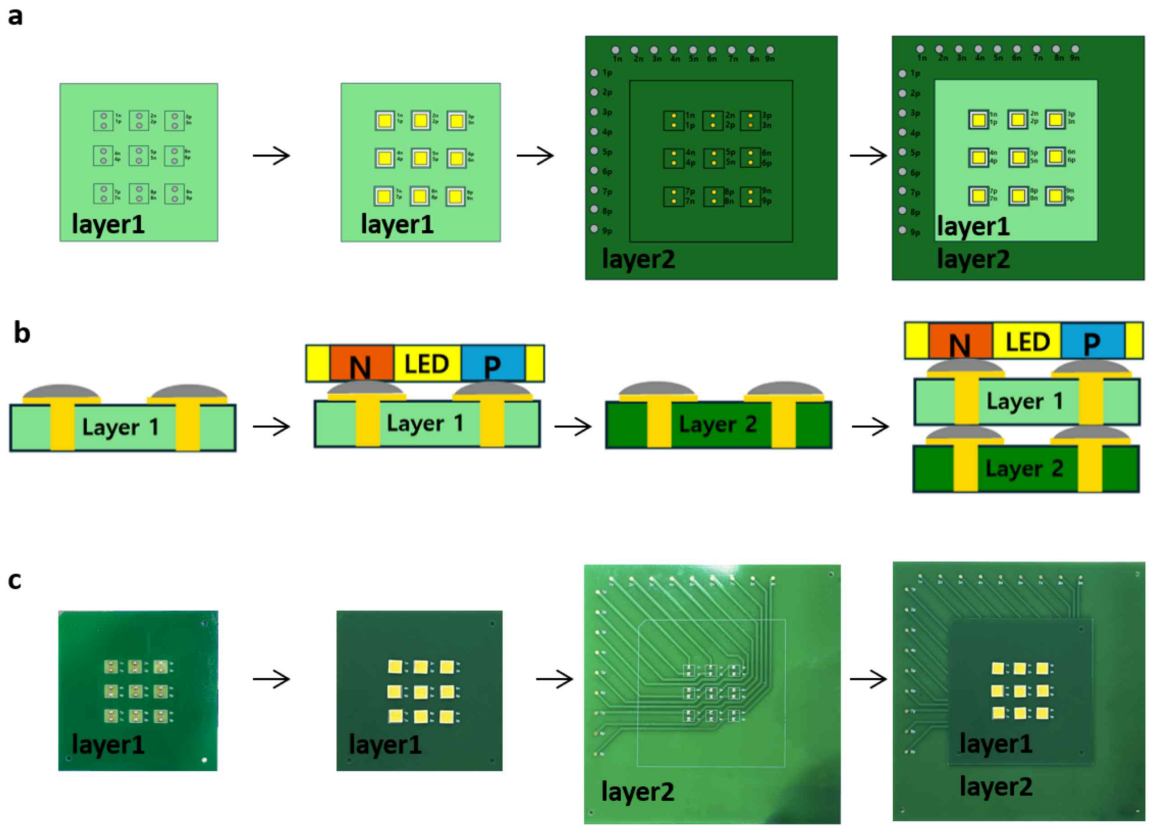

Fig. 3 Schematic of Layer 1-LED Connection, Layer 1-Layer 2 Connection, and PCB Design for Layer 1 and Layer 2. (a) Top-view schematic illustrating the sequence of connections: Layer 1 soldering → Layer 1-LED assembly → Layer 2 soldering → Layer 1-Layer 2 bonding. (b) Side view of a single chip showing the connection process. (c) Actual

photographs of the fabricated Layer 1 and Layer 2 PCBs and their assembly.

2. Results of the Experiment

Flux was applied to the metal pads of the Layer 1 PCB substrate, which utilized TSV technology, to enable wetting with the alloy, and soldering was successfully performed. Following this, LED chips were assembled onto the soldered Layer 1. The P/N contact positional data of the LED chips, which were randomly oriented on Layer 1, were obtained. Based on this information, wiring was designed and formed on the Layer 2 PCB. Soldering was then performed on the metal pads of the Layer 2 PCB, and Layer 1 (with assembled chips) and Layer 2 were aligned and bonded through heating. Voltage was applied to the final substrate, which was completed by combining TSV and PCB technologies, and the successful illumination of the LEDs was confirmed (Fig. 4). Fig. 5a shows the I-V curve measured using a probe station on a standalone LED chip (not assembled on the substrate) with applied voltages ranging from 0V to 10V. Fig. 5b presents the I-V curve for an LED chip assembled on the substrate and connected through the Layer 1 and Layer 2 PCBs under the same conditions. The similarity between the two curves confirms the successful electrical connection between the LED chip, Layer 1 PCB, and Layer 2 PCB[16].

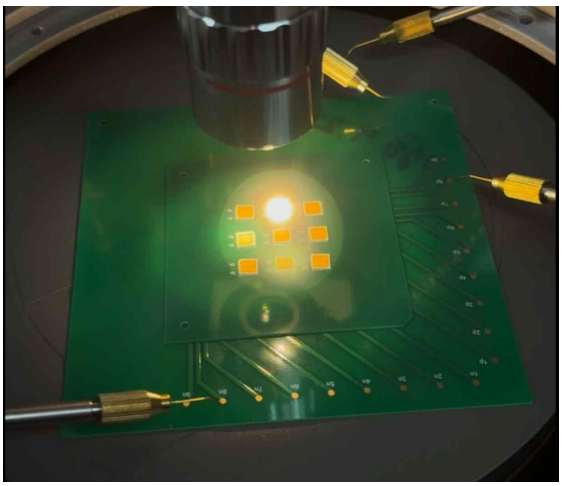

Fig. 4 Photograph of Successfully Illuminated LED.

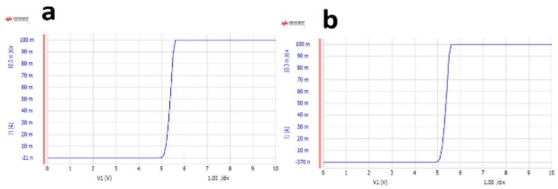

Fig. 5 LED I-V Curves (a)I-V curve measured for a standalone LED (not assembled on the substrate). (b) I-V curve measured for an LED connected through the Layer 1 and Layer 2 PCBs.

3. Methods

3.1 chip preparation

The LED chip used in this study, GW Q9LR331, has dimensions of 5 × 5 × 0.7 mm^3. The anode and cathode measure 4.5 × 1.9 mm^2, and the gap between the two electrodes is 0.4 mm

3.2 substrate preparation

The PCB design consists of two layers. Layer 1 is a square-shaped substrate measuring 6.5 × 6.5 cm^2, made from FR-4 material. It includes 18 pads for electrode connections. Layer 1 is equipped with 9 binding sites for LED connections, with guide lines drawn to match the LED size required for transfer. Each binding site measures 5 × 5 mm^2, and the gap between binding sites is 5 mm. The N and P electrodes within each binding site are designed to connect the electrodes of the LED chips to Layer 2, with dimensions of 1.5 × 1.5 mm^2. At the center of the N and P electrodes, there are copper-plated via holes used as pathways to connect to the lower layer, with a diameter of 0.2 mm. Layer 2 includes 36 pads and is made from FR-4 material, measuring 11.5 × 11.5 cm^2. To ensure proper electrical connections with the LED chips, 18 pads located in the upper-left corner of Layer 2 are wired, and alignment guidelines for attaching Layer 1 are marked. Fig. 3c (first and third images) shows photographs of Layer 1 and Layer 2 after soldering was

completed during fabrication. Both Layer 1 and Layer 2 include alignment routers with a diameter of 2.0 mm located at the upper-right, lower-left, and lower-right corners to facilitate precise alignment. Each layer is 0.8 mm thick, ensuring easy soldering and precise inter-layer connections, thereby guaranteeing stable electrical performance for the LEDs. The P/N contact orientation of the LEDs to be assembled on Layer 1 was arbitrarily determined, and the wiring on Layer 2 was designed and fabricated to match the arbitrary P/N contact positions.

3.3 Layer1-Chip Bonding

To bond the chips to the assembly substrate, soldering solution was prepared by melting a solder alloy with a melting point of 138°C and applying it to the copper (Cu) pads of the Layer 1 PCB substrate. The process of creating the soldering solution is as follows: A solder alloy with a melting point of 138°C was placed in a stainless-steel pot, and 50 mL of DI water was added. The mixture was heated to 180°C until the alloy was completely melted. To remove surface oxides, 100 μL of HCl was added to the solution, lowering its pH to 3. This solution was then applied to the Cu pads of the substrate to create an alloy coating. To enhance adhesion between the alloy and the Cu pads of the chips, as well as to remove residual oxides, flux was applied to the coated alloy. Care was taken to avoid excessive application of the solder. After preparing the soldered substrate, the chips were placed and aligned on the Layer 1 PCB according to the pre-designed P/N contact orientations. The aligned assembly was then placed on a 160°C hot plate to secure the chips to the substrate. Fig. 1 d (top section) and Fig. 3 (first and second steps) illustrate the Layer 1-Chip bonding process.

3.4 Layer1-Layer2 Bonding

To bond Layer 1 and Layer 2, a field's metal alloy with a lower melting point of 62°C was used, considering the already secured Layer 1-chip assembly with the 138°C alloy. The process of preparing the soldering solution and applying it to the substrate follows the same steps as described in Section 2.2, where the 138°C alloy was utilized. The soldering solution was prepared as follows: A 62°C melting-point alloy was placed in a stainless-steel pot, and 50 mL of DI water was added. The solution was heated to 85°C until the alloy was completely melted To remove surface oxides, 100 μL of HCl was added, reducing the solution's pH to 3. This alloy solution was then applied to the Cu pads of the Layer 2 PCB substrate through a wetting process to create a coating. Next, flux was applied to the electrode areas of Layer 1 to enhance the bonding strength between the layers and to remove oxide films on the pads. The Layer 1 substrate (with assembled chips) and Layer 2 were aligned precisely using alignment routers on a 90°C hot plate. The bonding process was then carried out, with the 62°C alloy forming the connection between the two layers. Once the bonding was complete, the assembly was cooled naturally to solidify the connection. Fig. 1d (bottom section) and Fig. 3 (third and fourth steps) illustrate the Layer 1-Layer 2 bonding process.

4. Conclusion

In this study, we proposed a method to improve the assembly of chips with randomly oriented P/N contacts after the FSA process by utilizing TSV technology and PCB technology. A PCB substrate was fabricated using TSV technology, and chips with random P/N contact orientations were assembled onto the substrate. Subsequently, a PCB substrate was designed and fabricated based on the positional data of the random P/N contacts, forming the required wiring. The two substrates were then electrically connected via soldering, and it was confirmed that power could successfully be supplied to LED chips with randomly oriented P/N contacts. This research eliminates the need to fabricate special chips with symmetrical P/N contacts, such as circular chips, for FSA studies. Instead, it provides a method to conduct research using conventional chips, significantly enhancing the efficiency of FSA research. Moreover, it demonstrates that displays can be implemented through the FSA process even with standard chips, expanding the range of Micro LEDs that can be utilized. Future

research will aim to extend this technology by applying FSA techniques to smaller Micro LED chips. The next step involves fabricating a TSV substrate for assembling chips, creating a PCB substrate based on the positional data of P/N contacts, and establishing electrical connections between the completed TSV substrate and PCB. This will allow power to be supplied to the Micro LED chips, enabling illumination. Such advancements will serve as a critical foundation for the commercialization and mass production of Micro LED displays.

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