AN58304

PSoC® 3 and PSoC 5 – Pin Selection for Analog Designs

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Software Version: PSoC® Creator™ 1.0
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AN58304 provides an overview of the analog routing matrix in PSoC® 3 and PSoC 5. This matrix is used to interconnect analog blocks and GPIO pins. A good understanding of the analog routing and pin connections can help the designer make selections to achieve the best possible analog performance. PSoC Creator™ will do a good job routing most designs, but with some assistance from the designer, better performance can be achieved. Topics such as LCD and Capsense routing are not covered in this application note.

Contents

PSoC 3 and PSoC 5 Internal Analog Routing

Prior to discussing which pins are better than others for a particular operation or application, it is best to understand the underlying analog structure of the PSoC 3 and PSoC 5 parts.

This application note focuses on connections between the analog blocks and GPIO pins. Digital routing, SIO, USB, and pins used for connecting the external crystals are not discussed.

PSoC 3 and PSoC 5 can be divided into an analog and digital section. The top section of the silicon is mostly analog and the bottom section is digital. The analog section consists of several analog blocks such as a Delta-Sigma ADC (DSM), comparators, DACs, and SC/CT blocks. The digital section contains the CPU, RAM, ROM, DMA, UDBs, Clocks, and so on.

The entire chip is surrounded by pins. Most of these pins are general purpose I/O or GPIO pins. The GPIO pins can be configured for eight different modes: seven digital and one analog input/output mode. This application note concentrates only on the analog mode for these pins.

Analog globals (AG) and analog mux buses (AMUXBUS) provide analog connectivity between GPIOs and the various analog blocks. As shown in Figure 1, there are 16 AGs that are divided between four quadrants. Each quadrant contains four analog globals: (AGR[7:4], AGR[3:0], AGL[7:4], and AGL[3:0]). The analog mux bus may be connected to any of the GPIO pins and most of the analog block inputs and outputs. It may be divided between the left and right half of the chip or configured as a single bus that wraps around the entire chip. Together, the analog mux bus and analog globals provide up to 18 paths between the analog blocks and GPIO pins. Additionally, there are about 20 dedicated

paths between GPIOs and analog blocks. The dedicated routes provide low resistive paths between GPIOs and devices such as current DACs and uncommitted opamps (operational amplifiers).

Best Analog Ports

The largest parts of the PSoC 3 and PSoC 5 families have more than seven full 8-pin ports or 56 GPIOs that can be used for analog input and output. Of these seven ports, three have a slight analog performance advantage **P0[7:0], P3[7:0],** and **P4[7:0]**. These ports reside in the analog upper portion of the chip. The analog globals, AGL[7:4] and AGR[7:4] that connect to these ports, also reside only in the upper analog section of the part, which give these ports a slight signal-to-noise.

Figure 1. PSoC 3 and PSoC 5 Analog/Digital Layout

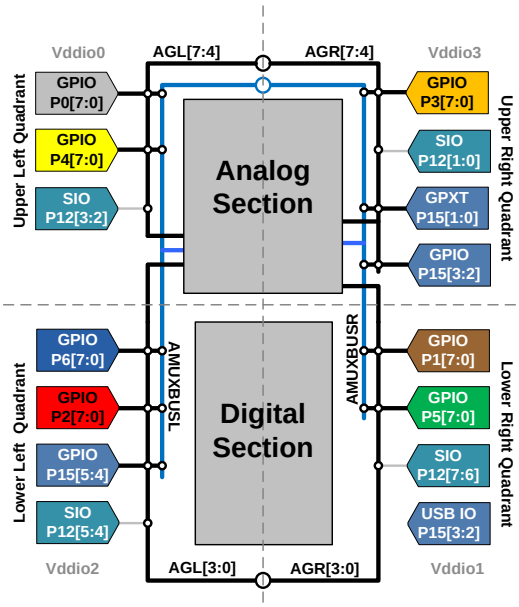
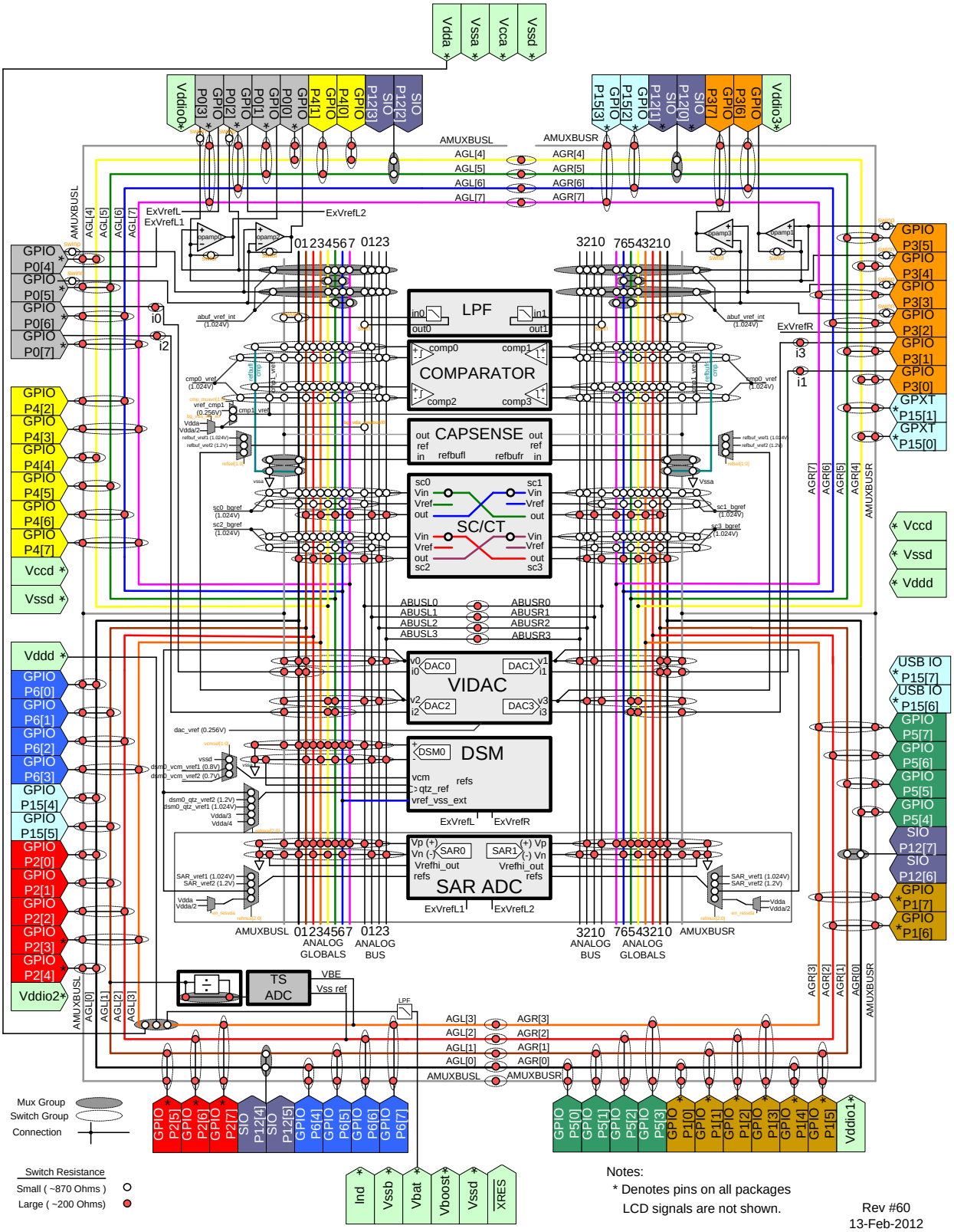


Figure 2. PSoC 3 and PSoC 5 Analog Diagram



PSoC Creator routes the analog signals for the user. However, the designer can dictate a preferred route by selecting a preferred GPIO for a given signal manually. This can be accomplished in the Pins section of the Design Wide Resource Editor in PSoC Creator.

The PSoC 3 and PSoC 5 Analog Diagram in Figure 2 is a detailed view of the analog section. This diagram shows all possible analog routes and switches between analog blocks and GPIOs. It is important to take the time to understand the basic interconnection between the GPIO pins and the internal analog blocks to be able to get the most out of your design.

Each Package has a different combination of GPIO pins available to the user. Table 1 below lists the available pin for each of the packages available for PSoC 3 and PSoC 5.

Table 1. GPIOs per package

Ports	100-pin TQFP	68-pin QFN	48-pin QFN	48-pin SSOP
Port 0	P0[7:0]	P0[7:0]	P0[7:0]	P0[7:0]
Port 1	P1[7:0]	P1[7:0]	P1[7:0]	P1[7:0]
Port 2	P2[7:0]	P2[7:0]	P2[7:3]	P2[7:3]
Port 3	P3[7:0]	P3[7:0]	NA	NA
Port 4	P4[7:0]	NA	NA	NA
Port 5	P5[7:0]	NA	NA	NA
Port 6	P6[7:0]	NA	NA	NA
Port 12	P12[7:0]	P12[7:0]	P12[3:0]	P12[3:0]
Port 15	P15[7:0]	P15[7:0]	P15[7:6], [3:0]	P15[7:6], [3:0]

Analog Mux Bus (AMUXBUS)

There are two AMUXBUS routes in PSoC 3 and PSoC 5 devices. The AMUXBUSL may be connected to any of the GPIOs on the left side. The AMUXBUSR can connect to all GPIOs on the right side of the device. The left and right AMUXBUS may be shorted together with an analog switch to create a single bus that can be connected to all GPIO pins. It is possible to use the AMUXBUS to connect all GPIOs to a single analog block such as the Delta-Sigma ADC.

Analog Globals (AGs)

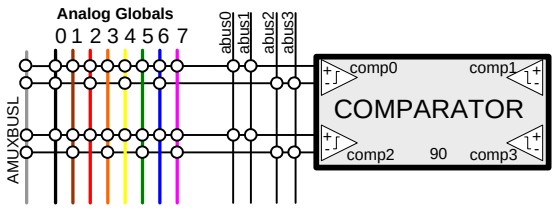
The PSoC 3 and PSoC 5 devices are divided into four quadrants as shown in Figure 1. The analog global bus has eight routes on each side: AGL[7:0] on the left and AGR[7:0] on the right. Within each side, the bus is divided into two groups: AGR[3:0] and AGR[7:4] for the right side and AGL[3:0] and AGL[7:4] for the left side. The lower four globals on each side are routed to the GPIO in the lower half of the part and the upper four globals on each side are routed to the GPIO in the upper half of the device. All eight analog globals on each side get routed to analog blocks on the same side. Analog globals can be used as single ended or differential signal paths.

The globals on the left and right half may operate independently or they may be joined through the switches that are shown at the top and bottom. The analog globals AGL[3:0] and AGR[3:0] are routed down and around the digital blocks. The other busses AGL[7:4] and AGR[7:4] stay up in the analog section where there is likely to be less digital switching noise and the paths are shorter (less resistive). In the Analog Diagram, each analog block is capable of connecting to various analog busses. These connections form an analog connection matrix between analog blocks and GPIO pins. Analog blocks may be interconnected to each other or to GPIOs. The small circles indicate switches that connect the paths that intersect. The On resistance of the switches colored red is about 200 ohms. The On resistance of the white switches is about 870 ohms. Note that the connection between the pins and analog globals or AMUXBUS is with the lower resistance switches.

Most of the switches can be addressed individually, which means that any combination of switches can be connected at any time. Not all analog block connections are connected to every analog bus. Although this would provide the most routing flexibility, it would significantly impact both the performance, due to added capacitance, and the cost because of the additional size.

To achieve a good tradeoff between cost, performance and routing, analog global bus connections between GPIOs and some analog block terminals are not fully populated. The connection patterns to the analogs buses often alternate between adjacent blocks and GPIOs. For example, in Figure 3, the negative input to the two comparators connects to a different set of analog globals. The negative input to comparator 0 connects to the odd analog globals and comparator 2 connects to the even analog globals.

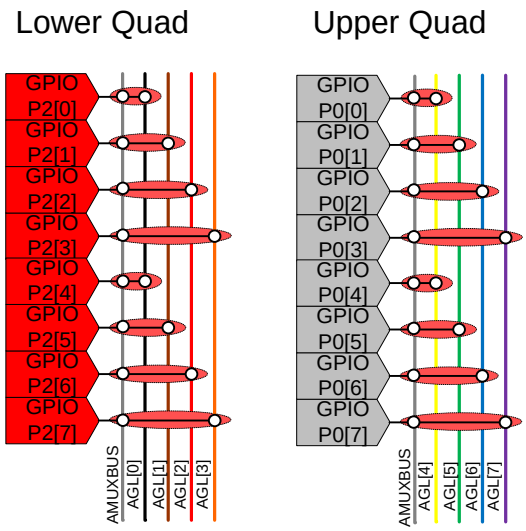
Figure 3. Comparator Connections



GPIO Connection to Analog Busses

Each GPIO pin may be connected to an analog global, the AMUXBUS, or both simultaneously. Two pins of each port share the same analog global connection. Figure 4 illustrates in two examples how the GPIOs are actually connected to the analog global busses. PSoC Creator makes these connections for the user when analog wires and muxes are placed between analog blocks and GPIOs.

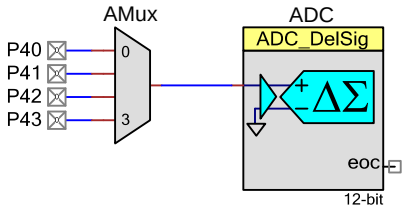
Figure 4. GPIO Connection to AG[n] and AMUXBUS



Optimizing Routing Resources

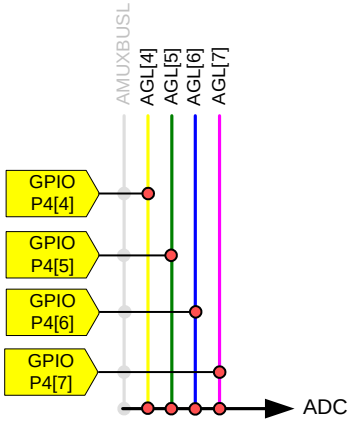
Although PSoC 3 and PSoC 5 contain much more analog routing resources than previous families, there is still a finite set of analog routes. Making the right pin assignments can mean the difference between a design fitting into a particular part and not having sufficient routing resources. Take the following example in Figure 5 where an analog mux is used to connect four signals to the ADC.

Figure 5. Example 1 Schematic



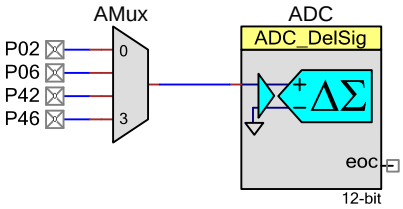
With the pins P4[3:0] selected, Figure 6 is an example of how the signals may be routed. Notice that all four of the analog globals AGL[7:4] are used. No other signals can be routed in that section using these globals.

Figure 6. Example 1 Internal Routing



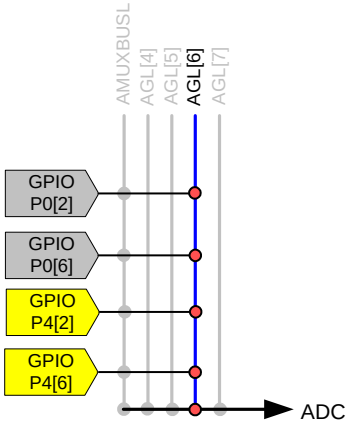
If the same schematic is used, but a different combination of pins (P0[2], P0[6], P4[2], P4[6]) selected we get a different result. See Figure 7.

Figure 7. Example 2 Schematic



This time a much more efficient use of internal routing resources are used as shown in Figure 8. Notice that only one analog global, AGL[6] is used, leaving three analog globals to route other signals. This relatively small change in pin selection could easily make the difference between a design fitting in the part or running out of routing resources.

Figure 8. Example 2 Internal Routing

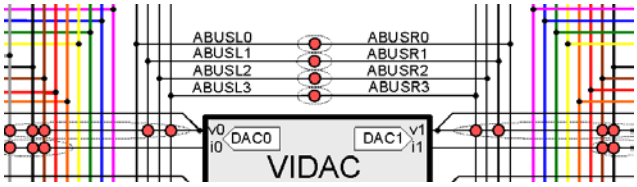


These two simple examples demonstrate the power of understanding the internal routing diagram.

Analog Local Bus (abus)

Internal to the analog section, there are eight additional analog local bus (abus) routes, four in the left half abusl[3:0] and four in the right half abusr[3:0] as shown in the Analog Diagram. These are local routes for interconnecting analog blocks but not to GPIOs. They help to save the analog globals to route to GPIOs. The left and right sides may be shorted together with four analog switches, as see in Figure 9.

Figure 9. Left and Right abus Interconnect



Routing Example

Figure 10 and Figure 11 illustrate a PSoC Creator Schematic and one possible route. Analog Global AGL[7] is used to connect GPIO P4[3] to the input of TIA_1 and the negative input to the ADC_DelSig_1. Analog bus abusl0 connects the output of TIA_1 to the positive input to ADC_DelSig_1. One of the analog globals AGL[6,4,2,0] could have been used instead of abusl0, but these are most valuable routing signals to and from GPIOs.

Figure 10. Example Signal Path Schematic

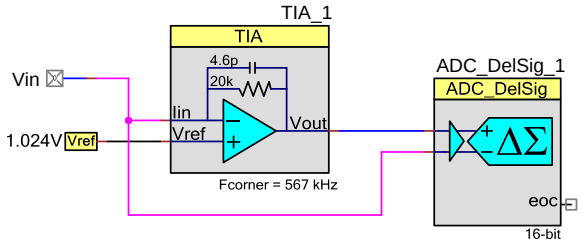
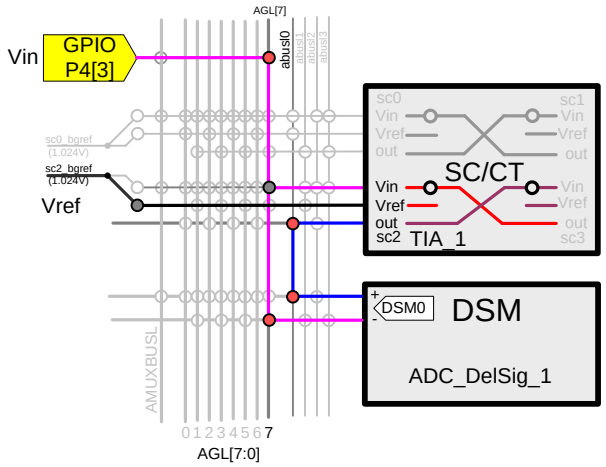


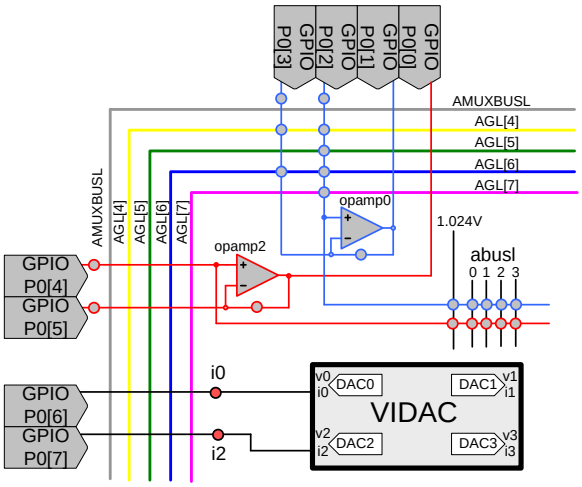
Figure 11. Example of Signal Path Route



Direct Routes to GPIO Pins

Several direct routes bypass the amuxbus, analog globals, and the analog local bus to connect analog blocks directly to GPIOs. The opamps and VIDACs both have direct connections that are used to maximize performance. Figure 12 is a simplified section of the analog routing diagram that shows some of these direct connections.

Figure 12. Dedicated GPIO Connections



IDAC Pin Selection

Each IDAC (current DAC) output may be routed to a GPIO in several ways. Using the analog globals or the analog mux bus works fine as long as the maximum current is limited to the two lower ranges of 32 µA or 255 µA. When using the high current range of 2 mA, the resistance in the path and analog switches may cause an excessive voltage drop and limit the compliance voltage of the current source at the pin. A path through the analog globals can be 500 ohms or more. To minimize the voltage drop, make sure that one of the pins listed in Table 2 is used to connect the output of the IDAC. This dedicated route is less than 200 ohms from IDAC to GPIO. PSoC Creator selects the appropriate IDAC to make sure that connection is made. Using these dedicated pins also frees up routing resources that can be used for other parts of the design. These dedicated pins can be used no matter what IDAC range is used. Therefore, you can use the dedicated pins any time an IDAC is used to maximize routing resources. Figure 12 shows these dedicated routes for DAC0 and DAC2.

Table 2. Dedicated IDAC Connections

IDAC	GPIO Pin
DAC0	P0[6]
DAC1	P3[0]
DAC2	P0[7]
DAC3	P3[1]

Opamp Pin Selection

The opamps are connected to the GPIOs in such a way that they can be used without any internal analog global busses, See Figure 12. If all connections to the opamp are external through the GPIOs, it is a good idea to use the dedicated pins. In many cases, the opamp may be used as a buffer to an internally generated signal, such as a buffer to a VDAC output. In this case the dedicated opamp input pins may be ignored and used for another purpose. After the opamp is enabled, the dedicated output GPIO will always be driven by the output of the opamp. This GPIO is now dedicated to the opamp output and cannot be used for another signal. Even if this signal is only used internally, the dedicated output pin will be driven by the opamp. This guarantees that the resistance between the opamp and GPIO pin is low, about 5 ohms. If you must use a different pin for the output, the dedicated output pin still outputs the signal. If the opamp is not used, it has no affect on the GPIOs directly connected to it. These GPIO pins operate as any of the other GPIOs when the opamp is disabled. The dedicated GPIO connections to the opamps are summarized in Table 3.

Table 3. Dedicated Opamp Connections

OPAMP	GPIO Pin (Non-inverting)	GPIO Pin (Inverting)	GPIO Pin (Output)
Opamp0	P0[2]	P0[3]	P0[1]
Opamp1	P3[5]	P3[4]	P3[6]
Opamp2	P0[4]	P0[5]	P0[0]
Opamp3	P3[3]	P3[2]	P3[7]

Reference Voltage Pins

External references can be used to enhance the accuracy or change the range of the ADCs. There are connections for external references for both the Delta-Sigma and SAR ADCs. The SAR ADC is only available in the CY8C55 family. The internal reference is accurate up to 0.1% over the operating temperature range depending on the device selected. An external reference can increase the accuracy beyond 0.1%. For the Delta-Sigma ADC, either pins P0[3] or P3[2] may be used for an external reference. Pins P0[2] or P0[4] are used for the SAR ADC external reference.

Pins P0[3] and P3[2] can also be used to bypass the reference voltage used for the Delta-Sigma ADC with a filter capacitor. A capacitor in the range of 1 µF to 10 µF is used to filter out low frequency noise on the internal reference voltage.

Table 4 is a summary of all the dedicated routes to GPIO pins on ports 0 and 3. It is a good idea to keep this list in mind when selecting GPIO connections to an IDAC and opamp, or when required to connect a bypass capacitor to an ADC reference. If you look close, the analog diagram in Figure 2 details each of these connections.

Table 4. GPIO Direct Routes

Port	Description
P0[0]	Opamp2 output
P0[1]	Opamp0 output
P0[2]	Opamp0 non-inverting input ExVrefL2 SAR ADC reference input
P0[3]	Opamp0 inverting input ExVrefL DCM (DelSig ADC) reference input Internal Reference bypass capacitor
P0[4]	Opamp2 non-inverting input ExVrefL1 SAR ADC reference input
P0[5]	Opamp2 inverting input
P0[6]	VIDAC0 current sink/source connection
P0[7]	VIDAC2 current sink/source connection
P3[0]	VIDAC1 current sink/source connection
P3[1]	VIDAC3 current sink/source connection
P3[2]	Opamp3 inverting input ExVrefL DCM (DelSig ADC) reference input Internal Reference bypass capacitor
P3[3]	Opamp3 non-inverting input
P3[4]	Opamp1 inverting input
P3[5]	Opamp1 non-inverting input
P3[6]	Opamp1 output
P3[7]	Opamp3 output

Separating Analog and Digital Signals

Depending on the sensor or source, many if not most analog signals tend to be relatively high impedance, at times as high as several megaohms. Digital signals on the other hand are usually low impedance on the order of 10 to 50 ohms with fast edge times of tens of nanoseconds or faster.

When these two signals are placed in close proximity on a circuit board, or are on adjacent pins, the fast rise and fall times of the digital signal can easily be capacitively coupled to the analog signal. Therefore, when selecting pins for analog and digital functions, it is recommended that analog and high speed digital signals be kept away from each other when possible. This coupling can occur both internal to the chip at the I/O pads and on the circuit board traces. Isolating these signals by at least one pin reduces this coupling both internally and externally. If possible it is good design practice to keep analog and digital signals on opposite sides of the chip. This also helps when it is time to lay out the circuit board.

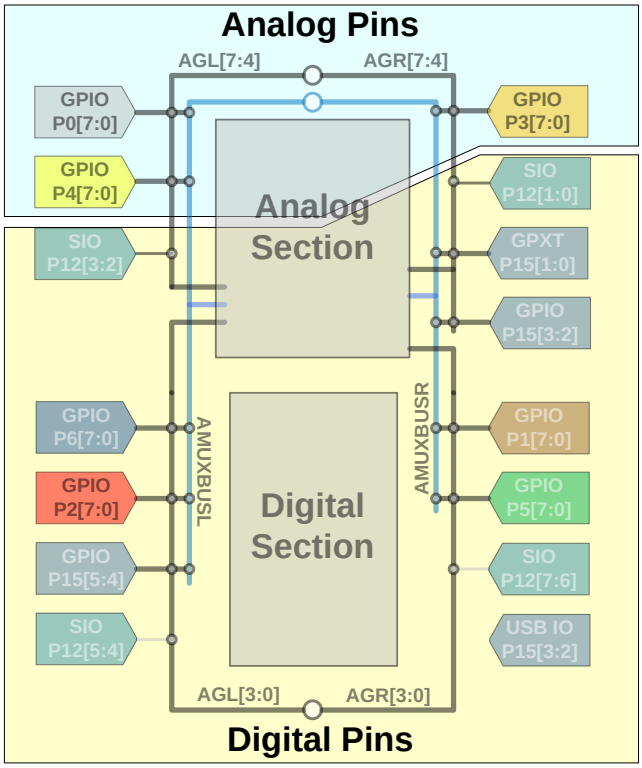
A few easy steps can be used to plan a pinout for optimal analog performance.

Design Steps

1. Determine how many analog pins/ports are required for a given design.
2. Determine which signals can or should use the dedicated routes between the analog block and the GPIO pin. Make these pin assignments first.
3. Start with port 0 and work out in both directions to port 4 and port 3 and select the analog GPIO pins needed for the design.
4. Draw a line between the analog GPIO pins selected and the rest of the pins required for the design.
5. Keep all analog GPIOs on one side of the line and all digital GPIOs on the other.

Follow these simple steps to isolate the analog and digital signals on both the chip and your circuit board. Figure 13 shows an ideal separation between analog and digital ports.

Figure 13. Ideal Analog and Digital Separation



Sometimes a design may have a mix of precision analog, low resolution analog, low speed digital, and high speed digital. The low precision and low speed digital can be used to isolate the precision analog and high speed digital. See Figure 14 for an example.

Connecting to the Sigma_Delta ADC

The analog blocks are equally distributed between the left and right sides of the chip. Currently, there is just one Delta-Sigma ADC, which is placed on the left side and only has direct connections to the routing resources on the left side. Signals may be routed from the right side of the part, but only by connecting the left and right analog globals together. When pins from the right side of the part must connect to the ADC, the analog globals on the right side must be connected to the corresponding analog globals on the left side. For example, if pin P3[7] needs to be routed to the ADC, the pin is first connected to AGR[7]. Then AGL[7] must then be connected to AGR[7] to route to the ADC. However, if pin P0[7] is selected, then only analog global AGL[7] is used instead of both AGR[7] and AGL[7]. (See the top section Analog Diagram for clarity). All of the left analog globals (AGL[7:0]) may be connected to the corresponding right analog globals (AGR[7:0]). See Figure 15.

Figure 14. Three Signal Sections

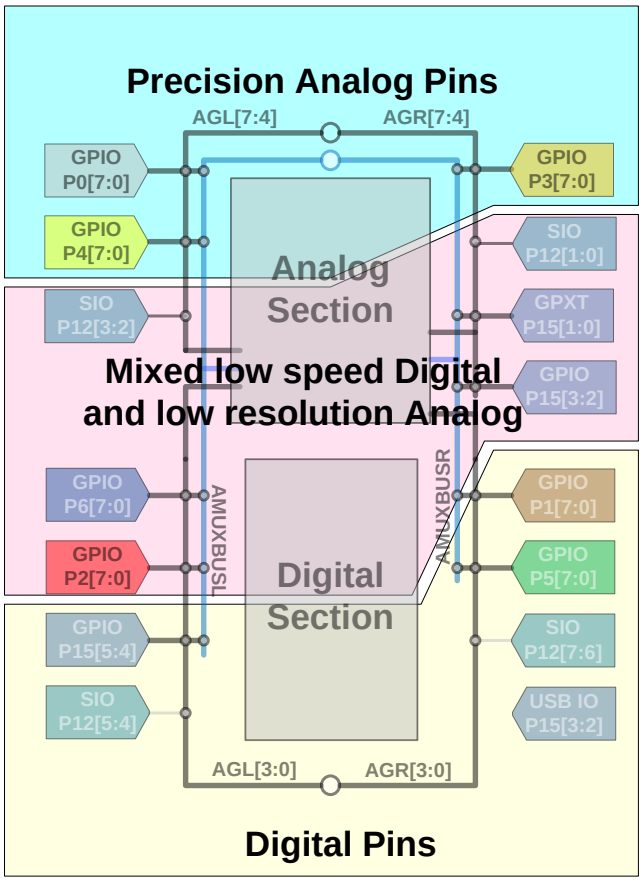
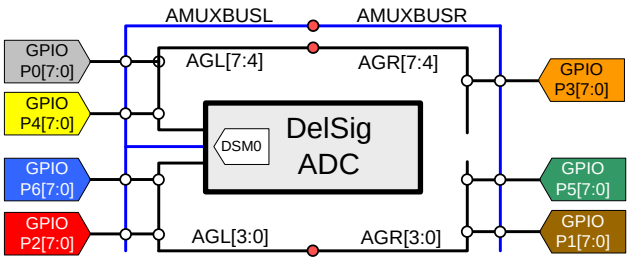


Figure 15. DelSig ADC Analog Connections



Summary

Because there are sufficient analog routing resources for most applications, designers should not be concerned with getting the most efficient hardware usage. For those cases where most analog resources are used or maximum analog performance is required, the topics discussed in this application note will help to optimize the design. The single most important thing that will help to improve your design, is to understand the PSoC 3 and PSoC 5 analog architecture shown in Figure 2, and make pin selections based on this knowledge.

All GPIO pins work fine for analog input, but ports P0[7:0], P3[7:0], and P4[7:0] may provide a measurable advantage in signal-to-noise performance than the remaining ports. Care should always be taken to keep digital signals away from sensitive analog signals, both on the PSoC and on the PCB.

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**	2828695	MEH	12/15/2009	New application note.
*A	2991540	SRIH	07/22/2010	Fixed branding discrepancies
*B	3371422	MEH	09/14/2011	Rewrite of several paragraphs and added or updated Figures, 2, 5,6,7,8,13
*C	3655552	MEH	06/26/2012	Updated PSoC 3 and PSoC 5 Internal Analog Routing. Updated Summary. Updated in new template.

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