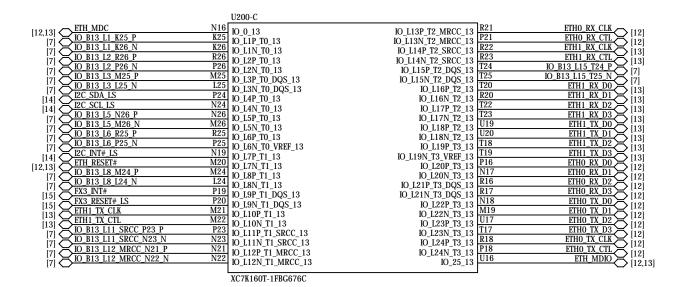
D D Mercury KX1 FPGA Module Revision 3 **Sheet 1: Cover** Sheet 15: USB 3.0 Controller (EZ-USB FX3)  $\mathbf{C}$ Sheet 16: USB 3.0 Controller / Peripherals Sheet 2: FPGA Bank 0/12/13/14 Sheet 3: FPGA Bank 15/16/32/33 Sheet 17: Power 3.3V / 1.0V / 5.0V Sheet 18: Power 1.2V / 1.8V / 2.0V Sheet 4: FPGA Bank 34/MGT Sheet 5: FPGA Power / Analog Reference Sheet 19: Power DDR3 / 2.5V / VTT Sheet 6: FPGA Decoupling Sheet 20: Mechanics **Sheet 7: Module Connector** Sheet 8: Real Time Clock/EEPROM/FLASH/Oscillator Sheet 9: DDR3 SDRAM Channel A Sheet 10: DDR3 SDRAM Channel B (lower bits) Sheet 11: DDR3 SDRAM Channel B (upper bits) Sheet 12: Gigabit Ethernet PHY 0 Sheet 13: Gigabit Ethernet PHY 1 Sheet 14: Rechargeable Battery/User LEDs DNE = do not equip© 2015 by Enclustra GmbH Confidential **Enclustra GmbH** 1 COVER Mercury KX1 23 Apr 2015

## 5 FPGA Bank 12 VCCO = VCC B12Bank is not available in XC7K70T D IO\_B12\_L13\_MRCC\_Y22\_P U21 IO\_0\_12 U22 IO\_L1P\_T0\_12 IO\_L13P\_T2\_MRCC\_12 | Y22 | AA22 | IO\_L13N\_T2\_MRCC\_12 | AC22 [7] | IO B12 L1 U22 P | IO B12 L1 V22 N | IO B12 L2 U24 P | IO B12 L2 U25 N | IO B12 L2 U25 N IO L13P T2 MRCC 12 IO L13P T2 MRCC 12 IO L14P T2 SRCC 12 IO L14P T2 SRCC 12 IO L15P T2 DQS 12 IO L15P T2 DQS 12 IO L16P T2 12 IO L16P T3 12 IO L16P T3 12 IO L16P T3 12 IO L16P T3 12 IO L20P T3 12 IO L21P T3 DQS 12 IO L22P T3 12 IO L22P T3 12 IO L22P T3 12 IO L22P T3 12 IO L23P T3 12 IO L24P T3 12 IO L24P T3 12 IO L24P T3 12 IO L25 12 IO L24P T3 12 IO L25 12 IO L25 12 IO L20 IO IO\_B12\_L13\_MRCC\_AA22\_N IO\_B12\_L14\_SRCC\_AC23\_P V22 IO\_L1N\_T0\_12 IO B12 L14 SRCC AC24 N IO B12 L15 W20 P IO B12 L15 Y21 N IO\_L2P\_T0\_12 IO\_L2N\_T0\_12 10 B12 L2 U25 N 10 B12 L3 V23 P 10 B12 L3 V24 N 10 B12 L4 U26 P 10 B12 L4 U26 P 10 B12 L5 W25 P 10 B12 L5 W25 P 10 B12 L6 V21 P 10 B12 L6 V21 P 10 B12 L7 AA25 P 10 B12 L7 AA25 P 10 B12 L8 W23 P 10 B12 L8 W24 N 10 B12 L8 W24 N 10 B12 L9 AB26 P 10 B12 L9 AB26 P V23 IO\_L3P\_T0\_DQS\_12 V24 IO\_L3N\_T0\_DQS\_12 IO\_B12\_L16\_AD23\_P IO\_B12\_L16\_AD24\_N U26 IO\_L4P\_T0\_12 V26 IO\_L4N\_T0\_12 | 10 B12 L16 AD24 N | 10 B12 L17 AB22 P | 10 B12 L17 AC22 N | 10 B12 L18 AB21 P | 10 B12 L18 AB21 P | 10 B12 L18 AD21 P | 10 B12 L19 VREF AE21 N | 10 B12 L20 AF24 P | 10 B12 L20 AF25 N | 10 B12 L21 AD26 P | 10 B12 L21 AD26 P | 10 B12 L22 AE23 N | 10 B12 L22 AE23 N | 10 B12 L22 AF23 N | W25 IO\_L4N\_T0\_12 W25 IO\_L5P\_T0\_12 W26 IO\_L5N\_T0\_12 V21 IO\_L6P\_T0\_12 IO L5N TO 12 IO\_L6P\_T0\_12 IO\_L6N\_T0\_VREF\_12 IO\_L7P\_T1\_12 IO\_L7N\_T1\_12 IO\_L8P\_T1\_12 W24 IO\_L8P\_T1\_12 W24 IO\_L8N\_T1\_12 AB26 IO\_L9P\_T1\_DQS\_12 AC26 IO\_L9N\_T1\_DQS\_12 IO\_L9N\_T1\_DQS\_12 IO B12 L22 AF23 N IO B12 L23 AD25 P IO\_L10P\_T1\_12 IO\_L10N\_T1\_12 IO\_B12\_L23\_AE25\_N IO\_B12\_L24\_AE22\_P IO\_L11P\_T1\_SRCC\_12 IO\_L11N\_T1\_SRCC\_12 10 B12 L12 MRCC Y23 P 10 B12 L12 MRCC AA24 N IO\_L12P\_T1\_MRCC\_12 IO\_L12N\_T1\_MRCC\_12 XC7K160T-1FBG676C FPGA Bank 0 $VCCO = VCC\_CFG\_B13$ VCC\_CFG\_B13 VCC\_CFG\_B13 VREF\_ADC U200-A FPGA INII# [3,7,15] FPGA PROG# [3,7,8,14,15,16] FPGA DONE [7,15] [2] FPGA\_VF\_P [2] FPGA\_VF\_N N12 VP\_0 P11 VN\_0 INIT BO PROGRAM\_B\_ DONE ( VREFP\_0 FPGA\_CFGBVS N11 VREFN\_0 R200 4k7 CFGBVS\_0 FLASH\_CLK\_FPGA\_CCLK [2,7,8,16] R12 DXP\_0 DXN\_0 CCLK\_0 GND\_ADC [7,16] JTAG\_TDI [7,16] JTAG\_TDO [7,16] JTAG\_TCK [7,16] JTAG\_TMS FPGA\_MODE [7,15] M1\_0 | 12\_ ם ומד TDO\_0 TCK O TMS 0 XC7K160T-1FBG676C TDI and TMS have internal pullups. **ADC Anti-Alias Filter** [7] \rightarrow \frac{\text{FPGA\_V\_P}}{} FPGA\_VF\_P [2] 1n 25V FPGA\_VF\_N [2]

## FPGA Bank 13

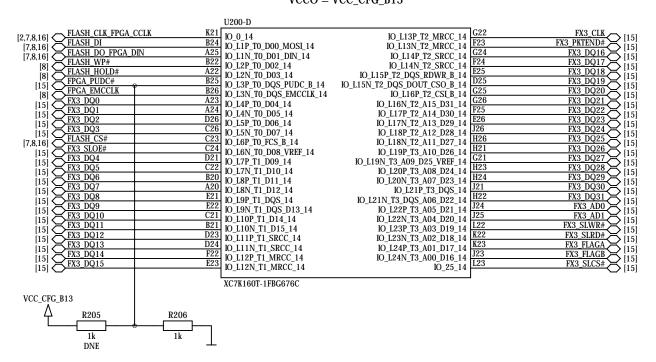
VCCO = VCC\_CFG\_B13

D



## FPGA Bank 14

VCCO = VCC\_CFG\_B13



## **FPGA Mode**

		Configuration
Default	0 1	Active Serial Passive Serial

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Company	Enclustra GmbH			
Sheet name	2_FPGA_BANK0_12_13_14			
Project	Mercury KX1			
Revision R3	Designed MH	Date 23 Apr 2015	Sheet/sheets 2 / 20	

