



Enclustra User Schematics

Disclaimer

User schematics do not include proprietary Enclustra design elements, such as power supply circuits. These circuits use optimized designs which are extremely compact and remain proprietary to Enclustra. The user manual provides all necessary information to use the module and its interfaces.

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Full schematics, including a full bill-of-materials, are available through the purchase of a hardware licence for the product in question. Please contact Enclustra Sales for more information.

Note: DNE = Do Not Equip (parts not equipped by default)

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D

Mercury+ KX2 FPGA Module

Revision 2.2

C

- Sheet 1: Cover
- Sheet 2: FPGA Banks 0 | 14 | Configuration
- Sheet 3: FPGA Banks 12 | 13 | 15 | 16 | MGT
- Sheet 4: FPGA Banks 32 | 33 | 34
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- Sheet 6: FPGA Decoupling
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B

A

D

C

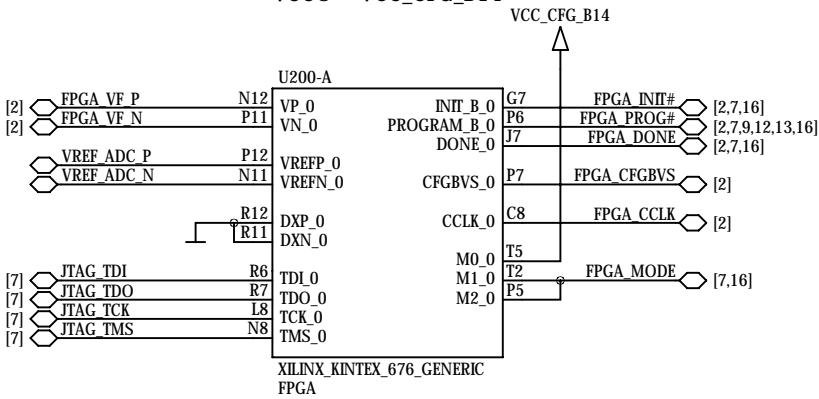
B

A

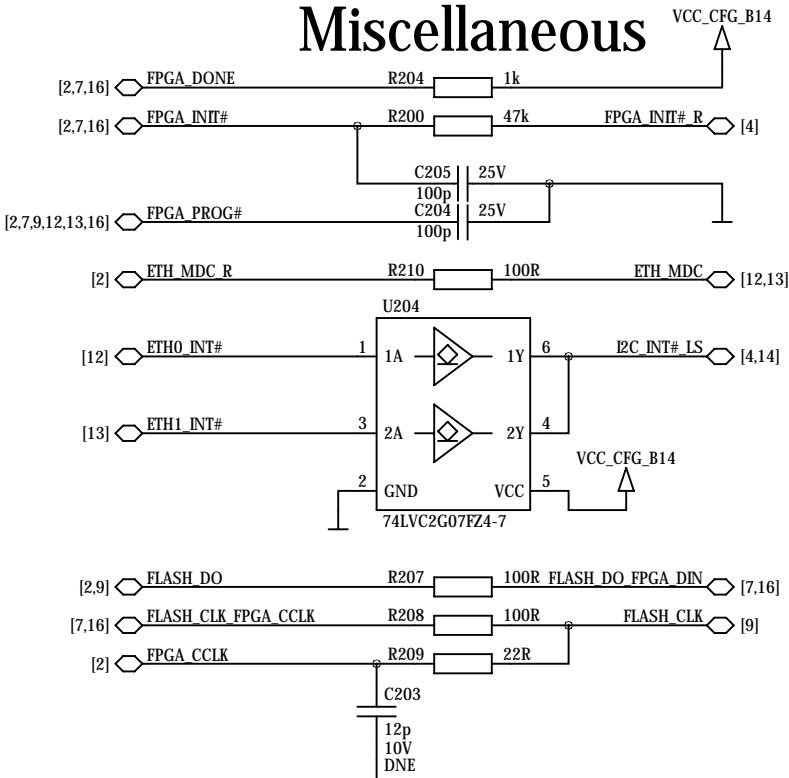
D

FPGA Bank 0

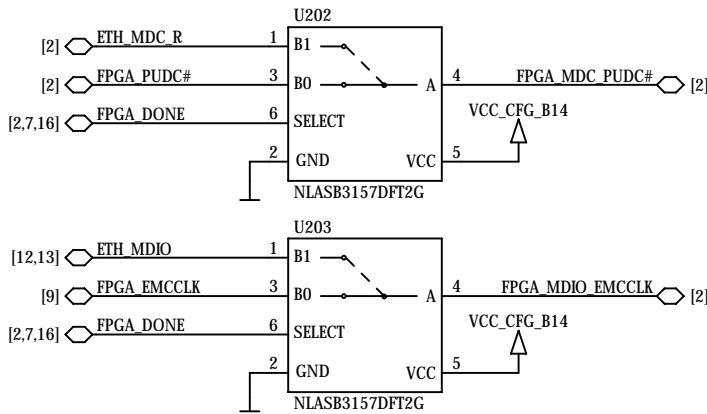
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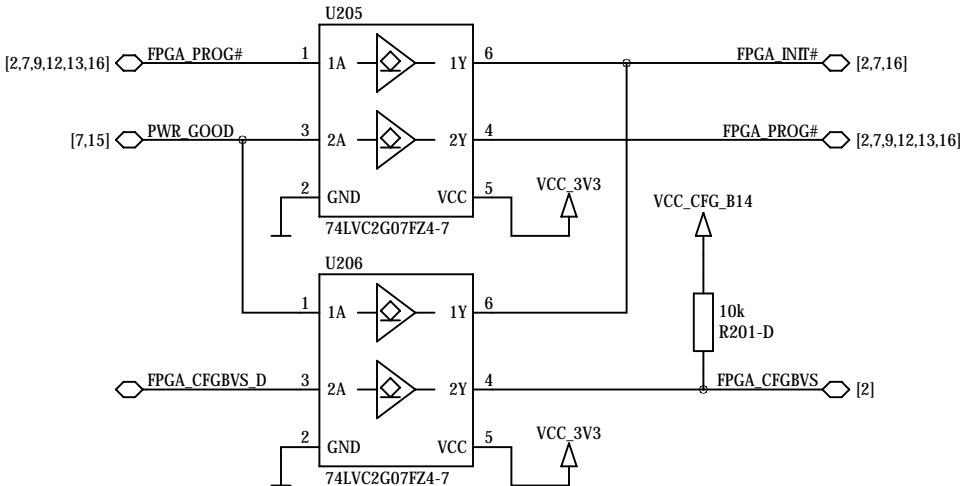
Miscellaneous



MDIO Multiplexer

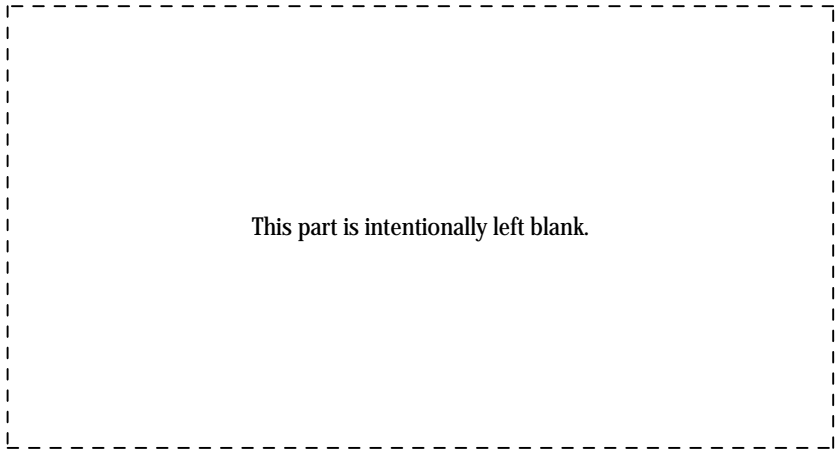


Reset Circuit



Voltage Select Detection

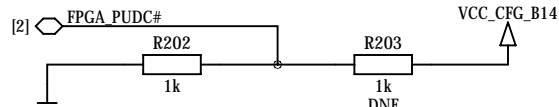
not included in user schematics



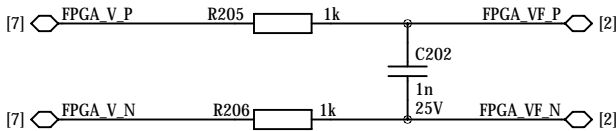
FPGA Mode

		Configuration
Default	0 1	Active Serial Passive Serial

Pull-Up During Configuration

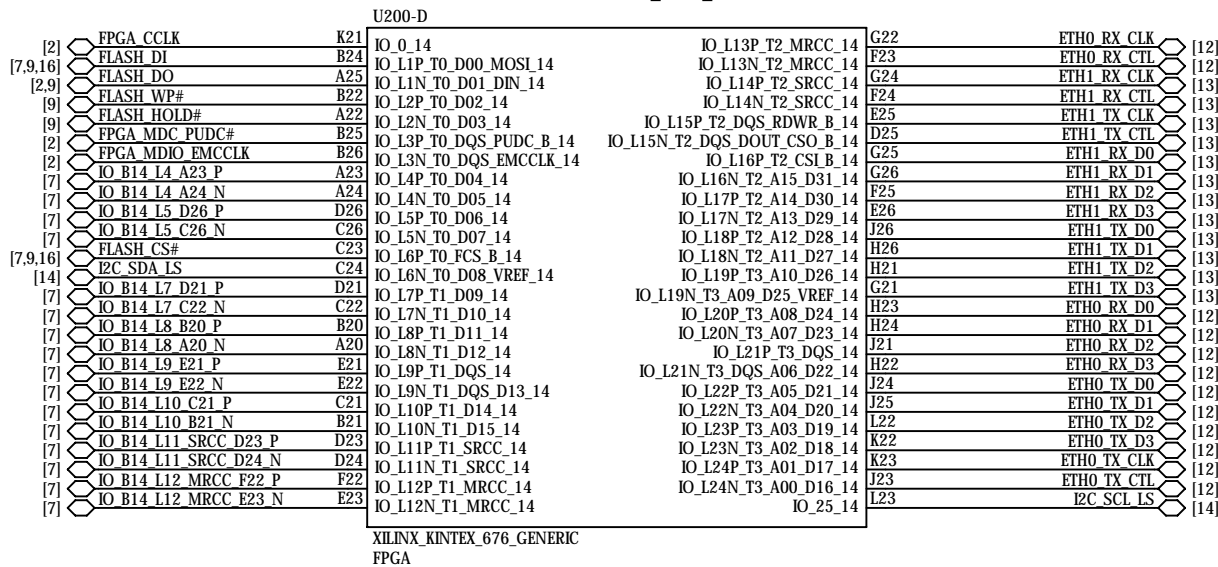


ADC Anti-Alias Filter



FPGA Bank 14

VCCO = VCC_CFG_B14



A

D

C

B

A

D

FPGA Bank 12

VCCO = VCC_IO_B12

Bank is not available in XC7K70T

U200-B									
[7]	IO B12 U21	U21	IO_0_12	IO_L13P_T2_MRCC_12	Y22	IO B12 L13 MRCC Y22 P	[7]		
[7]	IO B12 L1 U22 P	U22	IO_L1P_T0_12	IO_L13N_T2_MRCC_12	AA22	IO B12 L13 MRCC AA22 N	[7]		
[7]	IO B12 L1 V22 N	V22	IO_L1N_T0_12	IO_L14P_T2_SRCC_12	AC23	IO B12 L14 SRCC AC23 P	[7]		
[7]	IO B12 L2 U24 P	U24	IO_L2P_T0_12	IO_L14N_T2_SRCC_12	AC24	IO B12 L14 SRCC AC24 N	[7]		
[7]	IO B12 L2 V25 N	U25	IO_L2N_T0_12	IO_L15P_T2_DQS_12	W20	IO B12 L15 W20 P	[7]		
[7]	IO B12 L3 V23 P	V23	IO_L3P_T0_DQS_12	IO_L15N_T2_DQS_12	Y21	IO B12 L15 Y21 N	[7]		
[7]	IO B12 L3 V24 N	V24	IO_L3N_T0_DQS_12	IO_L16P_T2_12	AD23	IO B12 L16 AD23 P	[7]		
[7]	IO B12 L4 U26 P	U26	IO_L4P_T0_12	IO_L16N_T2_12	AD24	IO B12 L16 AD24 N	[7]		
[7]	IO B12 L4 V26 N	V26	IO_L4N_T0_12	IO_L17P_T2_12	AB22	IO B12 L17 AB22 P	[7]		
[7]	IO B12 L5 W25 P	W25	IO_L5P_T0_12	IO_L17N_T2_12	AC22	IO B12 L17 AC22 N	[7]		
[7]	IO B12 L5 W26 N	W26	IO_L5N_T0_12	IO_L18P_T2_12	AB21	IO B12 L18 AB21 P	[7]		
[7]	IO B12 L6 V21 P	V21	IO_L6P_T0_12	IO_L18N_T2_12	AC21	IO B12 L18 AC21 N	[7]		
[7]	IO B12 L6 VREF W21 N	W21	IO_L6N_T0_VREF_12	IO_L19P_T3_12	AD21	IO B12 L19 AD21 P	[7]		
[7]	IO B12 L7 AA25 P	AA25	IO_L7P_T1_12	IO_L19N_T3_VREF_12	AE21	IO B12 L19 VREF AE21 N	[7]		
[7]	IO B12 L7 AB25 N	AB25	IO_L7N_T1_12	IO_L20P_T3_12	AF24	IO B12 L20 AF24 P	[7]		
[7]	IO B12 L8 W23 P	W23	IO_L8P_T1_12	IO_L20N_T3_12	AF25	IO B12 L20 AF25 N	[7]		
[7]	IO B12 L8 W24 N	W24	IO_L8N_T1_12	IO_L21P_T3_DQS_12	AD26	IO B12 L21 AD26 P	[7]		
[7]	IO B12 L9 AB26 P	AB26	IO_L9P_T1_DQS_12	IO_L21N_T3_DQS_12	AE26	IO B12 L21 AE26 N	[7]		
[7]	IO B12 L9 AC26 N	AC26	IO_L9N_T1_DQS_12	IO_L22P_T3_12	AE23	IO B12 L22 AE23 P	[7]		
[7]	IO B12 L10 Y25 P	Y25	IO_L10P_T1_12	IO_L22N_T3_12	AF23	IO B12 L22 AF23 N	[7]		
[7]	IO B12 L10 Y26 N	Y26	IO_L10N_T1_12	IO_L23P_T3_12	AD25	IO B12 L23 AD25 P	[7]		
[7]	IO B12 L11 SRCC AA23 P	AA23	IO_L11P_T1_SRCC_12	IO_L23N_T3_12	AE25	IO B12 L23 AE25 N	[7]		
[7]	IO B12 L11 SRCC AB24 N	AB24	IO_L11N_T1_SRCC_12	IO_L24P_T3_12	AE22	IO B12 L24 AE22 P	[7]		
[7]	IO B12 L12 MRCC Y23 P	Y23	IO_L12P_T1_MRCC_12	IO_L24N_T3_12	AF22	IO B12 L24 AF22 N	[7]		
[7]	IO B12 L12 MRCC AA24 N	AA24	IO_L12N_T1_MRCC_12	IO_25_12	Y20	IO B12 Y20	[7]		

XILINX_KINTEX_676_GENERIC
FPGA

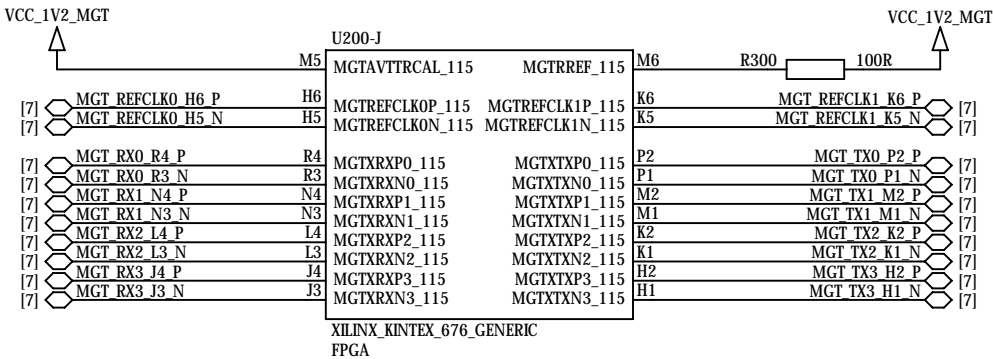
FPGA Bank 15

VCCO = VCC_IO_B15

U200-E									
[8]	IO B15 K15	K15	IO_0_15	IO_L13P_T2_MRCC_15	E18	IO B15 L13 MRCC E18 P	[7]		
[7]	IO B15 L1 AD0 C16 P	C16	IO_L1P_T0_AD0P_15	IO_L13N_T2_MRCC_15	D18	IO B15 L13 MRCC D18 N	[7]		
[7]	IO B15 L1 AD0 B16 N	B16	IO_L1N_T0_AD0N_15	IO_L14P_T2_SRCC_15	H17	IO B15 L14 SRCC H17 P	[7]		
[7]	IO B15 L2 AD8 A18 P	A18	IO_L2P_T0_AD8P_15	IO_L14N_T2_SRCC_15	H18	IO B15 L14 SRCC H18 N	[7]		
[7]	IO B15 L2 AD8 A19 N	A19	IO_L2N_T0_AD8N_15	IO_L15P_T2_DQS_15	D19	IO B15 L15 D19 P	[7]		
[7]	IO B15 L3 AD1 B17 P	B17	IO_L3P_T0_DQS_AD1P_15	IO_L15N_T2_DQS_ADV_B_15	D20	IO B15 L15 D20 N	[7]		
[7]	IO B15 L3 AD1 A17 N	A17	IO_L3N_T0_DQS_AD1N_15	IO_L16P_T2_A28_15	G19	IO B15 L16 G19 P	[7]		
[7]	IO B15 L4 AD9 C19 P	C19	IO_L4P_T0_AD9P_15	IO_L16N_T2_A27_15	F20	IO B15 L16 F20 N	[7]		
[7]	IO B15 L4 AD9 B19 N	B19	IO_L4N_T0_AD9N_15	IO_L17P_T2_A26_15	F19	IO B15 L17 F19 P	[7]		
[7]	IO B15 L5 AD2 C17 P	C17	IO_L5P_T0_AD2P_15	IO_L17N_T2_A25_15	E20	IO B15 L17 E20 N	[7]		
[7]	IO B15 L5 AD2 C18 N	C18	IO_L5N_T0_AD2N_15	IO_L18P_T2_A24_15	H19	IO B15 L18 H19 P	[7]		
[7]	IO B15 L6 D15 P	D15	IO_L6P_T0_15	IO_L18N_T2_A23_15	G20	IO B15 L18 G20 N	[7]		
[8]	IO B15 L6 VREF D16 N	D16	IO_L6N_T0_VREF_15	IO_L19P_T3_A22_15	K20	IO B15 L19 K20 P	[7]		
[8]	IO B15 L7 AD10 H16 P	H16	IO_L7P_T1_AD10P_15	IO_L19N_T3_A21_VREF_15	J20	IO B15 L19 VREF J20 N	[7]		
[8]	IO B15 L7 AD10 G16 N	G16	IO_L7N_T1_AD10N_15	IO_L20P_T3_A20_15	J18	IO B15 L20 J18 P	[7]		
[8]	IO B15 L8 AD3 G15 P	G15	IO_L8P_T1_AD3P_15	IO_L20N_T3_A19_15	J19	IO B15 L20 J19 N	[7]		
[8]	IO B15 L8 AD3 F15 N	F15	IO_L8N_T1_AD3N_15	IO_L21P_T3_DQS_15	L19	IO B15 L21 L19 P	[7]		
[8]	IO B15 L9 AD11 J15 P	J15	IO_L9P_T1_DQS_AD11P_15	IO_L21N_T3_DQS_A18_15	L20	IO B15 L21 L20 N	[7]		
[8]	IO B15 L9 AD11 J16 N	J16	IO_L9N_T1_DQS_AD11N_15	IO_L22P_T3_A17_15	K16	IO B15 L22 K16 P	[7]		
[8]	IO B15 L10 AD4 E15 P	E15	IO_L10P_T1_AD4P_15	IO_L22N_T3_A16_15	K17	IO B15 L22 K17 N	[7]		
[8]	IO B15 L10 AD4 E16 N	E16	IO_L10N_T1_AD4N_15	IO_L23P_T3_FOE_B_15	M17	IO B15 L23 M17 P	[7]		
[7]	IO B15 L11 SRCC AD12 G17 P	G17	IO_L11P_T1_SRCC_AD12P_15	IO_L23N_T3_FWE_B_15	L18	IO B15 L23 L18 N	[7]		
[7]	IO B15 L11 SRCC AD12 F18 N	F18	IO_L11N_T1_SRCC_AD12N_15	IO_L24P_T3_RS1_15	L17	IO B15 L24 L17 P	[7]		
[7]	IO B15 L12 MRCC AD5 F17 P	F17	IO_L12P_T1_MRCC_AD5P_15	IO_L24N_T3_RS0_15	K18	IO B15 L24 K18 N	[7]		
[8]	IO B15 L12 MRCC AD5 E17 N	E17	IO_L12N_T1_MRCC_AD5N_15	IO_25_15	M16	IO B15 M16	[8]		

XILINX_KINTEX_676_GENERIC
FPGA

FPGA MGT Bank 115



A

FPGA Bank 13

VCCO = VCC_IO_B13

U200-C									
[8]	IO B13 N16	N16	IO_0_13	IO_L13P_T2_MRCC_13	R21	IO B13 L13 MRCC R21 P	[8]		
[8]	IO B13 L1 K25 P	K25	IO_L1P_T0_13	IO_L13N_T2_MRCC_13	P21	IO B13 L13 MRCC P21 N	[8]		
[8]	IO B13 L1 K26 N	K26	IO_L1N_T0_13	IO_L14P_T2_SRCC_13	R22	IO B13 L14 SRCC R22 P	[8]		
[8]	IO B13 L2 R26 P	R26	IO_L2P_T0_13	IO_L14N_T2_SRCC_13	R23	IO B13 L14 SRCC R23 N	[8]		
[8]	IO B13 L2 P26 N	P26	IO_L2N_T0_13	IO_L15P_T2_DQS_13	T24	IO B13 L15 T24 P	[8]		
[8]	IO B13 L3 M25 P	M25	IO_L3P_T0_DQS_13	IO_L15N_T2_DQS_13	T25	IO B13 L15 T25 N	[8]		
[8]	IO B13 L3 L25 N	L25	IO_L3N_T0_DQS_13	IO_L16P_T2_13	T20	IO B13 L16 T20 P	[8]		
[8]	IO B13 L4 P24 P	P24	IO_L4P_T0_13	IO_L16N_T2_13	R20	IO B13 L16 R20 N	[8]		
[8]	IO B13 L4 N24 N	N24	IO_L4N_T0_13	IO_L17P_T2_13	T22	IO B13 L17 T22 P	[8]		
[8]	IO B13 L5 N26 P	N26	IO_L17N_T2_13	IO_L17P_T2_13	T23	IO B13 L17 T23 N	[8]		
[8]	IO B13 L5 M26 N	M26	IO_L5N_T0_13	IO_L18P_T2_13	U19	IO B13 L18 U19 P	[8]		
[8]	IO B13 L6 R25 P	R25	IO_L6P_T0_13	IO_L18N_T2_13	U20	IO B13 L18 U20 N	[8]		
[8]	IO B13 L6 VREF P25 N	P25	IO_L6N_T0_VREF_13	IO_L19P_T3_13	T18	IO B13 L19 T18 P	[8]		
[8]	IO B13 L7 N19 P	N19	IO_L7P_T1_13	IO_L19N_T3_VREF_13	T19	IO B13 L19 VREF T19 N	[8]		
[8]	IO B13 L7 M20 N	M20	IO_L7N_T1_13	IO_L20P_T3_13	P16	IO B13 L20 P16 P	[8]		
[8]	IO B13 L8 M24 P	M24	IO_L8P_T1_13	IO_L20N_T3_13	N17	IO B13 L20 N17 N	[8]		
[8]	IO B13 L8 L24 N	L24	IO_L8N_T1_13	IO_L21P_T3_DQS_13	R16	IO B13 L21 R16 P	[8]		
[8]	IO B13 L9 P19 P	P19	IO_L9P_T1_DQS_13	IO_L21N_T3_DQS_13	R17	IO B13 L21 R17 N	[8]		
[8]	IO B13 L9 P20 N	P20	IO_L9N_T1_DQS_13	IO_L22P_T3_13	N18	IO B13 L22 N18 P	[8]		
[8]	IO B13 L10 M21 P	M21	IO_L10P_T1_13	IO_L22N_T3_13	M19	IO B13 L22 M19 N	[8]		
[8]	IO B13 L10 M22 N	M22	IO_L10N_T1_13	IO_L23P_T3_13	U17	IO B13 L23 U17 P	[8]		
[8]	IO B13 L11 SRCC P23 P	P23	IO_L11P_T1_SRCC_13	IO_L23N_T3_13	T17	IO B13 L23 T17 N	[8]		
[8]	IO B13 L11 SRCC N23 N	N23	IO_L11N_T1_SRCC_13	IO_L24P_T3_13	R18	IO B13 L24 R18 P	[8]		
[8]	IO B13 L12 MRCC N21 P	N21	IO_L12P_T1_MRCC_13	IO_L24N_T3_13	P18	IO B13 L24 P18 N	[8]		
[8]	IO B13 L12 MRCC N22 N	N22	IO_L12N_T1_MRCC_13	IO_25_13	U16	IO B13 U16	[8]		

XILINX_KINTEX_676_GENERIC
FPGA

D

FPGA Bank 16

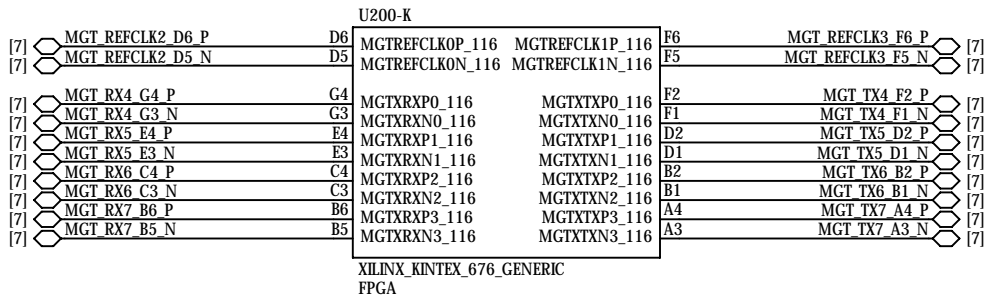
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U200-F									
[8]	IO B16 J8	J8	IO_0_16	IO_L13P_T2_MRCC_16	C12	IO B16 L13 MRCC C12 P	[7]		
[8]	IO B16 L1 H9 P	H9	IO_L1P_T0_16	IO_L13N_T2_MRCC_16	C11	IO B16 L13 MRCC C11 N	[7]		
[8]	IO B16 L1 H8 N	H8	IO_L1N_T0_16	IO_L14P_T2_SRCC_16	E11	IO B16 L14 SRCC E11 P	[7]		
[8]	IO B16 L2 G10 P	G10	IO_L2P_T0_16	IO_L14N_T2_SRCC_16	D11	IO B16 L14 SRCC D11 N	[7]		
[7]	IO B16 L2 G9 N	G9	IO_L2N_T0_16	IO_L15P_T2_DQS_16	F14	IO B16 L15 F14 P	[7]		
[7]	IO B16 L3 J13 P	J13	IO_L3P_T0_DQS_16	IO_L15N_T2_DQS_16	F13	IO B16 L15 F13 N	[7]		
[7]	IO B16 L3 H13 N	H13	IO_L3N_T0_DQS_16	IO_L16P_T2_16	G12	IO B16 L16 G12 P	[7]		
[7]	IO B16 L4 J11 P	J11	IO_L4P_T0_16	IO_L16N_T2_16	F12	IO B16 L16 F12 N	[7]		
[7]	IO B16 L4 J10 N	J10	IO_L4N_T0_16	IO_L17P_T2_16	D14	IO B16 L17 D14 P	[7]		
[7]	IO B16 L5 H14 P	H14	IO_L5P_T0_16	IO_L17N_T2_16	D13	IO B16 L17 D13 N	[7]		
[7]	IO B16 L5 G14 N	G14	IO_L5N_T0_16	IO_L18P_T2_16	E13	IO B16 L18 E13 P	[7]		
[7]	IO B16 L6 H12 P	H12	IO_L6P_T0_16	IO_L18N_T2_16	E12	IO B16 L18 E12 N	[7]		
[7]	IO B16 L6 VREF H11 N	H11	IO_L6N_T0_VREF_16	IO_L19P_T3_16	C14	IO B16 L19 C14 P	[7]		
[7]	IO B16 L7 F9 P	F9	IO_L7P_T1_16	IO_L19N_T3_VREF_16	C13	IO B16 L19 VREF C13 N	[7]		
[8]	IO B16 L7 F8 N	F8	IO_L7N_T1_16	IO_L20P_T3_16	B12	IO B16 L20 B12 P	[7]		
[8]	IO B16 L8 D9 P	D9	IO_L8P_T1_16	IO_L20N_T3_16	B11	IO B16 L20 B11 N	[7]		
[8]	IO B16 L8 D8 N	D8	IO_L8N_T1_16	IO_L21P_T3_DQS_16	B14	IO B16 L21 B14 P	[7]		
[8]	IO B16 L9 A9 P	A9	IO_L9P_T1_DQS_16	IO_L21N_T3_DQS_16	A14	IO B16 L21 A14 N	[7]		
[8]	IO B16 L9 A8 N	A8	IO_L9N_T1_DQS_16	IO_L22P_T3_16	B10	IO B16 L22 B10 P	[7]		
[8]	IO B16 L10 C9 P	C9	IO_L10P_T1_16	IO_L22N_T3_16	A10	IO B16 L22 A10 N	[7]		
[8]	IO B16 L10 B9 N	B9	IO_L10N_T1_16	IO_L23P_T3_16	B15	IO B16 L23 B15 P	[7]		
[7]	IO B16 L11 SRCC G11 P	G11	IO_L11P_T1_SRCC_16	IO_L23N_T3_16	A15	IO B16 L23 A15 N	[7]		
[7]	IO B16 L11 SRCC F10 N	F10	IO_L11N_T1_SRCC_16	IO_L24P_T3_16	A13	IO B16 L24 A13 P	[7]		
[8]	IO B16 L12 MRCC E10 P	E10	IO_L12P_T1_MRCC_16	IO_L24N_T3_16	A12	IO B16 L24 A12 N	[7]		
[8]	IO B16 L12 MRCC D10 N	D10	IO_L12N_T1_MRCC_16	IO_25_16	J14	IO B16 J14	[8]		

XILINX_KINTEX_676_GENERIC
FPGA

B

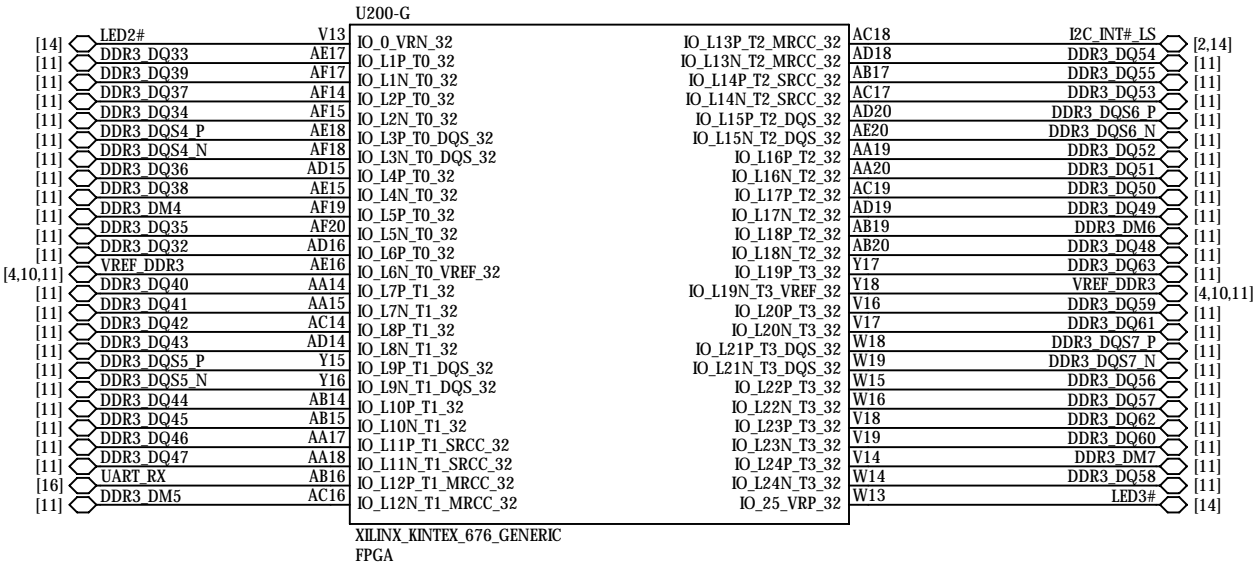
FPGA MGT Bank 116



FPGA Bank 32

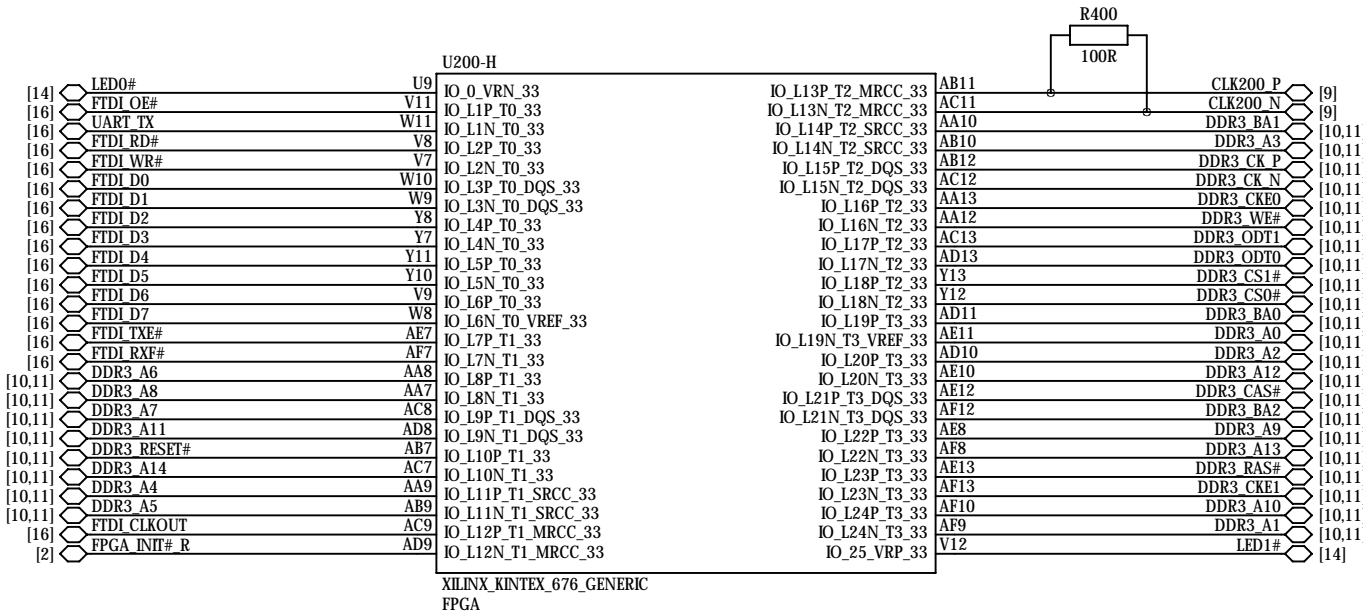
VCCO = VCC_DDR3

Bank is not available in XC7K70T



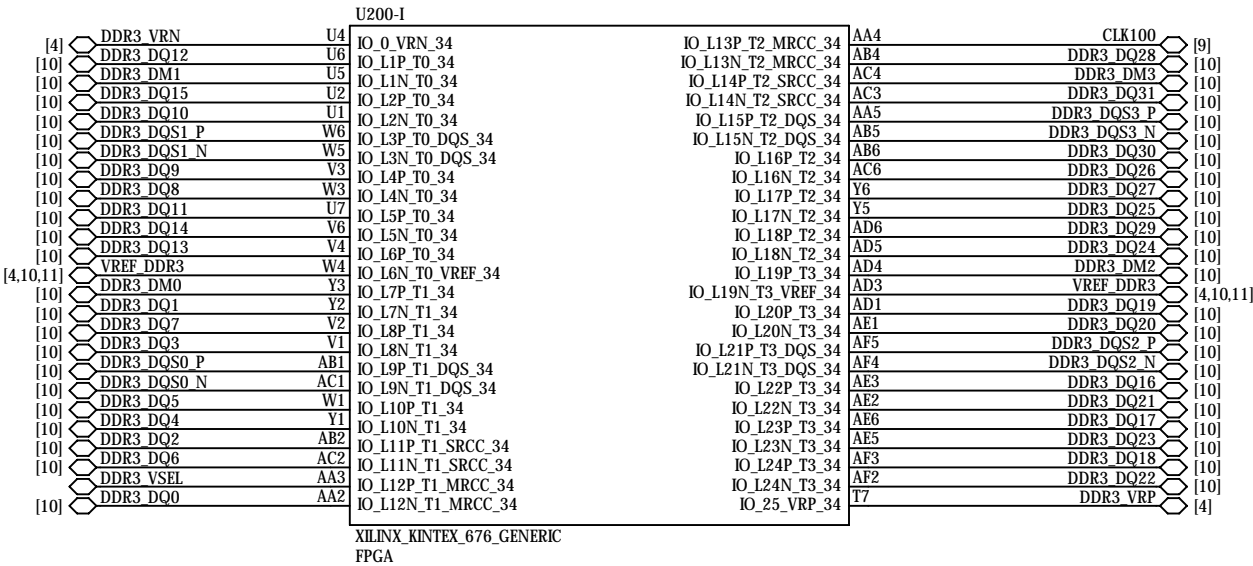
FPGA Bank 33

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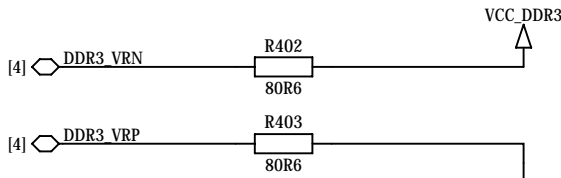


FPGA Bank 34

VCCO = VCC_DDR3



FPGA Driver Calibration

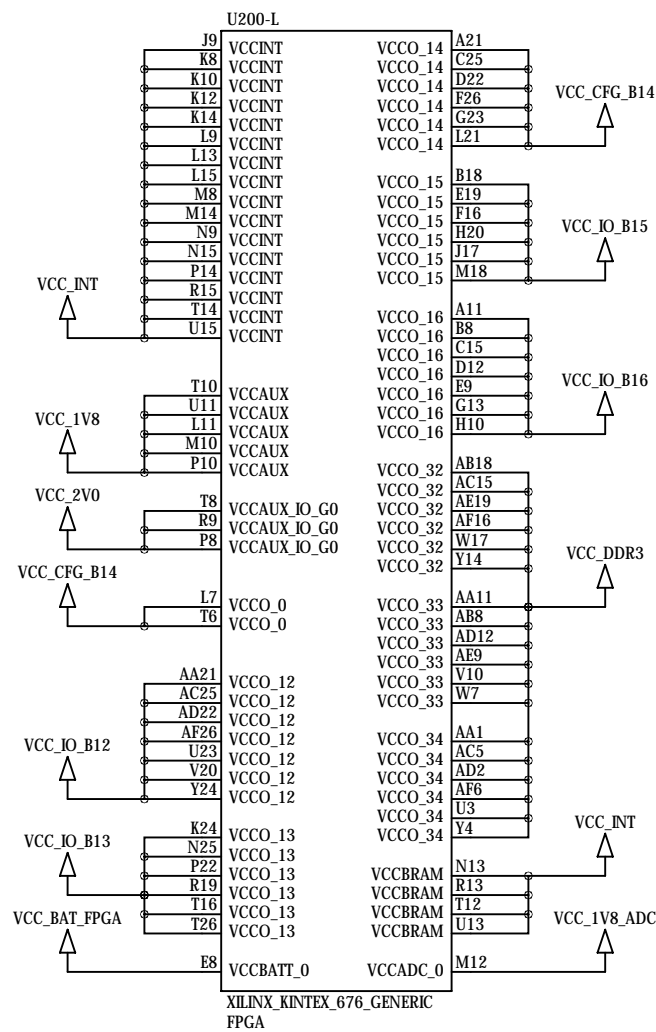


DDR3 VREF Decoupling

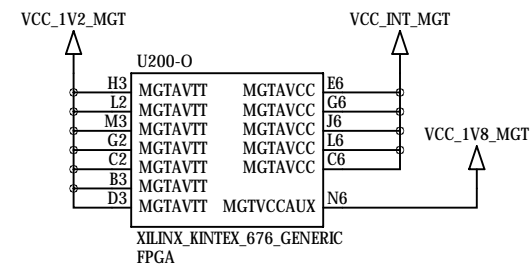
not included in user schematics

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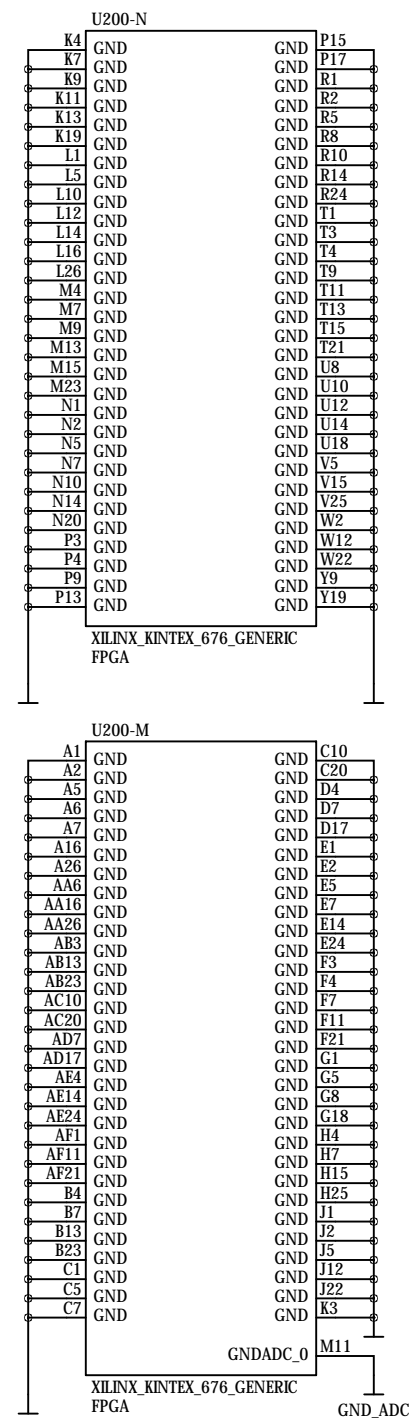
FPGA Power



FPGA MGT Power



FPGA Ground



MGT Power Filters

not included in user schematics

This part is intentionally left blank.

FPGA ADC Supply Filter

not included in user schematics

This part is intentionally left blank.

Analog Reference Voltage

not included in user schematics

This part is intentionally left blank.



D

D

C

C

B

B

A

A

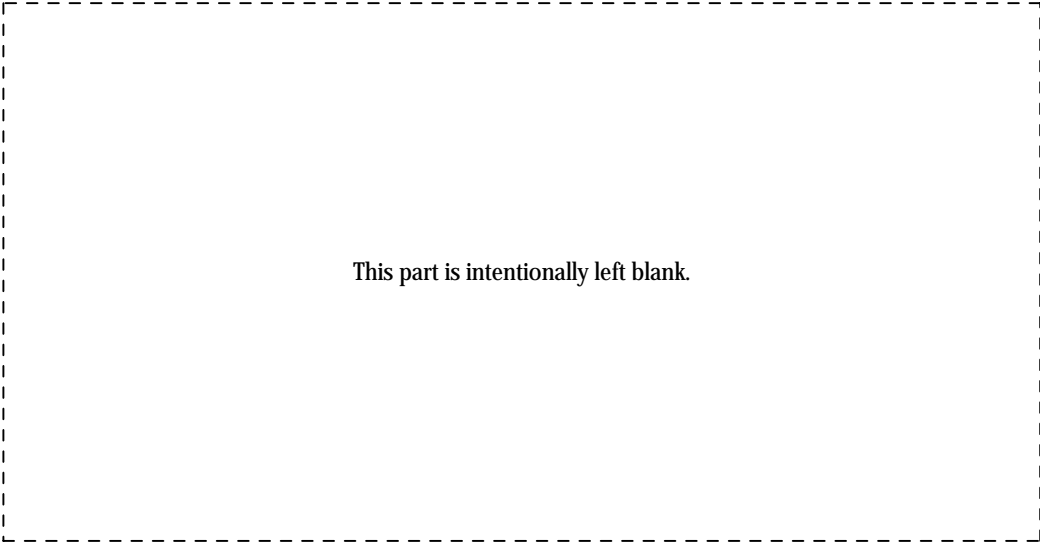
FPGA Decoupling

not included in user schematics

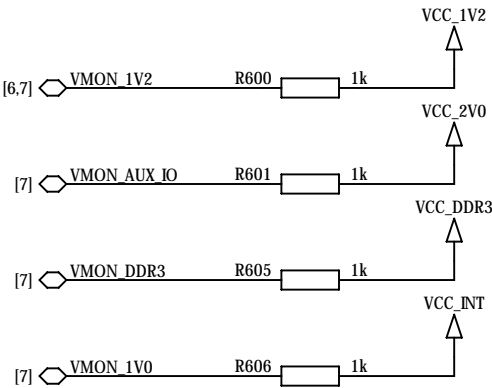


Power Decoupling

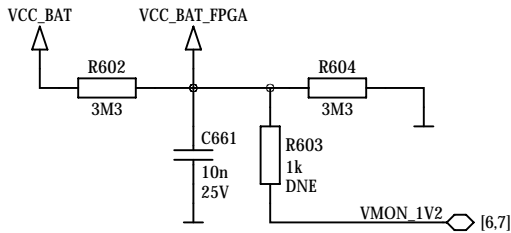
not included in user schematics



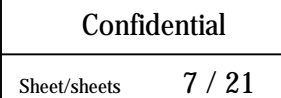
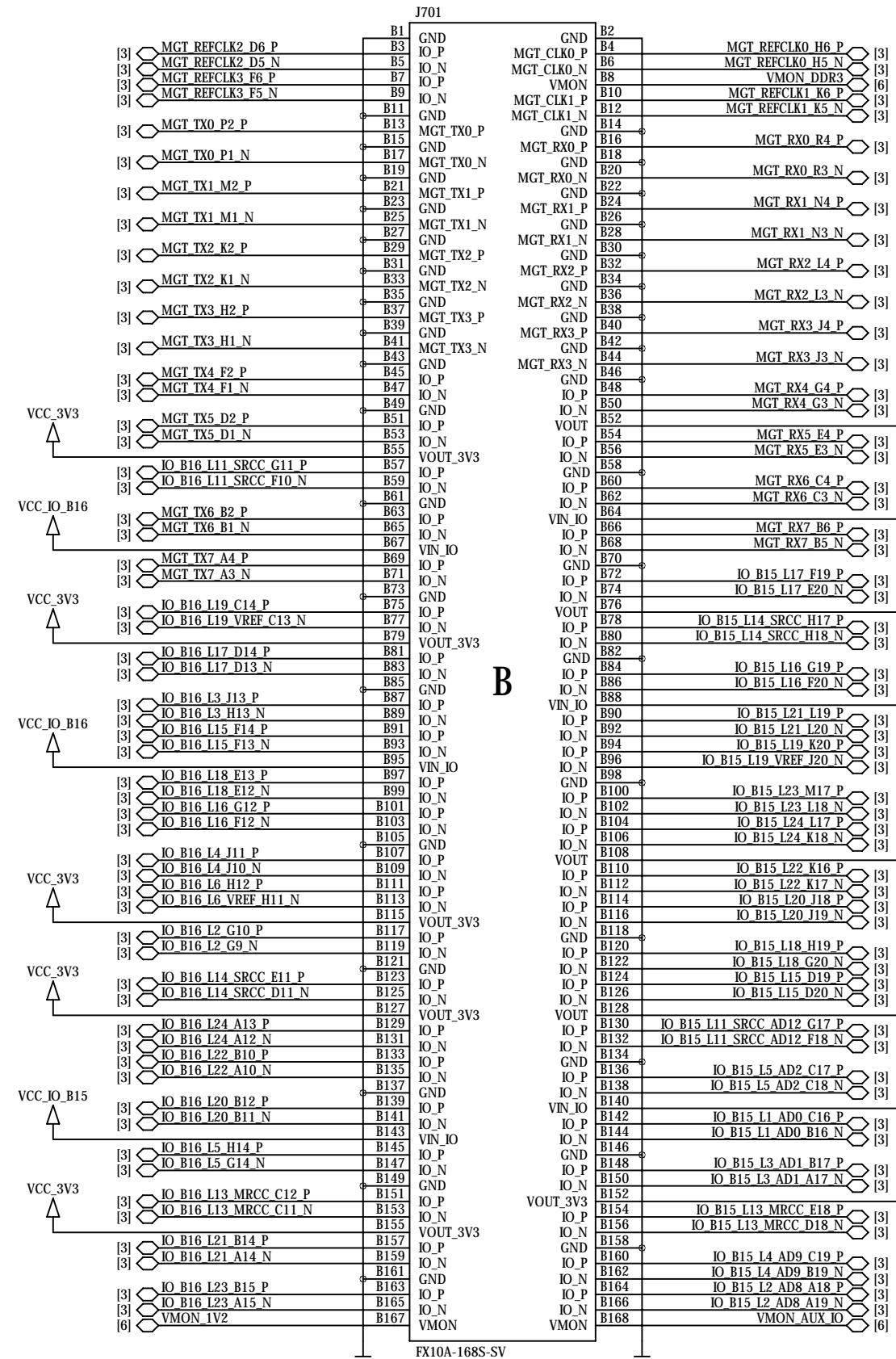
Voltage Monitoring



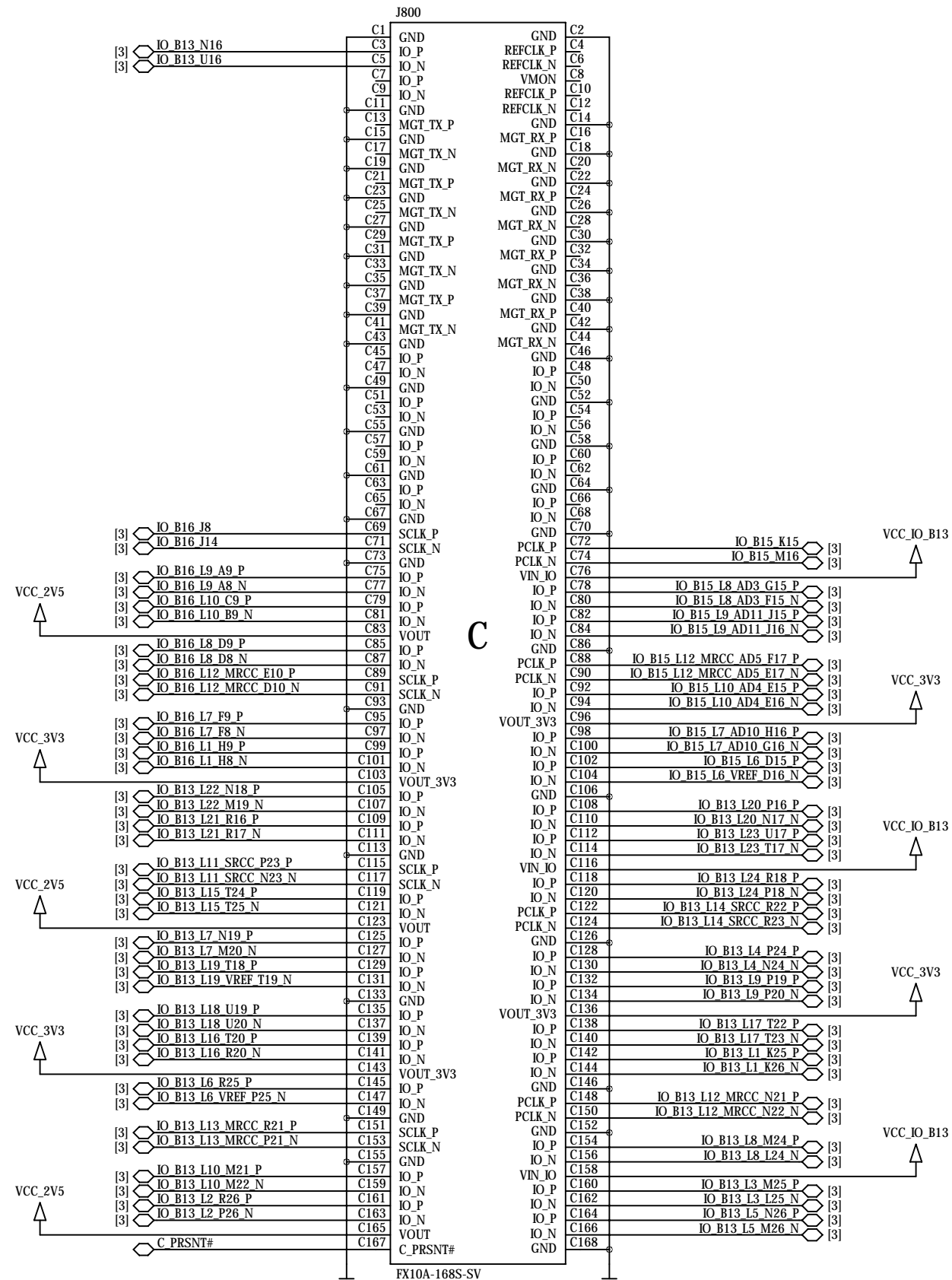
FPGA Battery Voltage



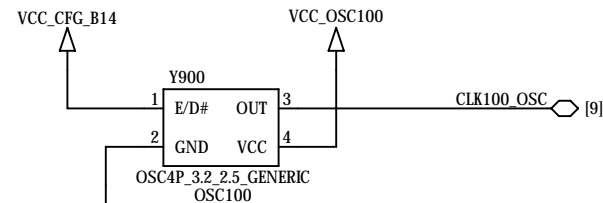
Module Connector B



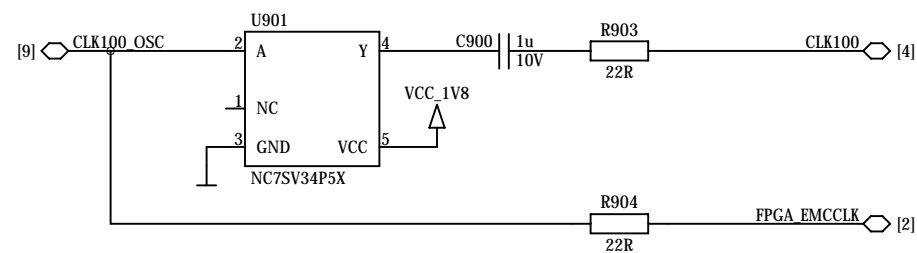
Module Connector C



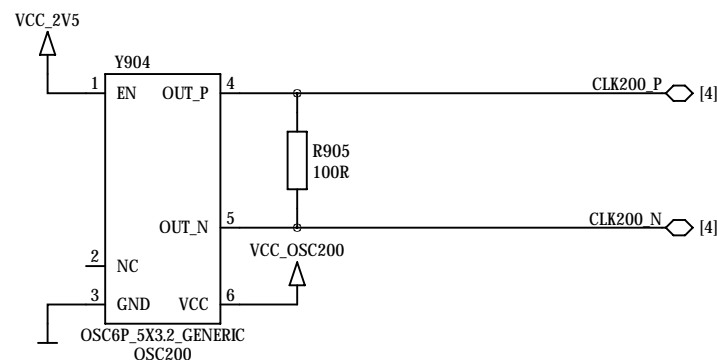
100 MHz Oscillator



Clock Driver



200 MHz Oscillator

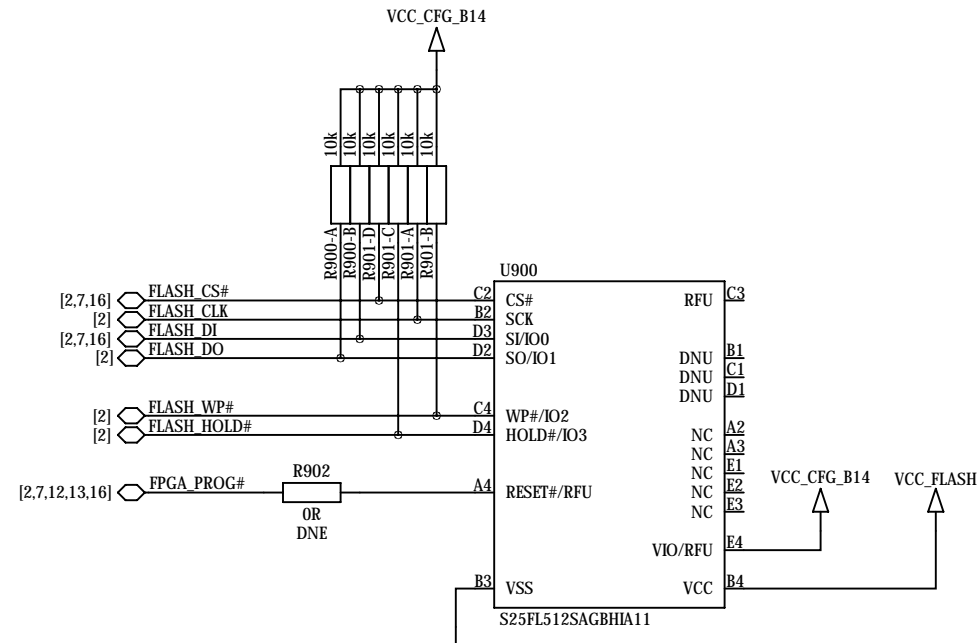


Oscillator Power Filters

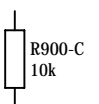
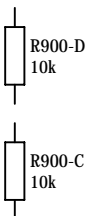
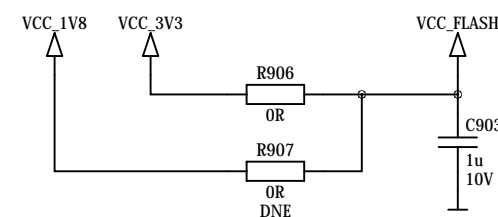
not included in user schematics

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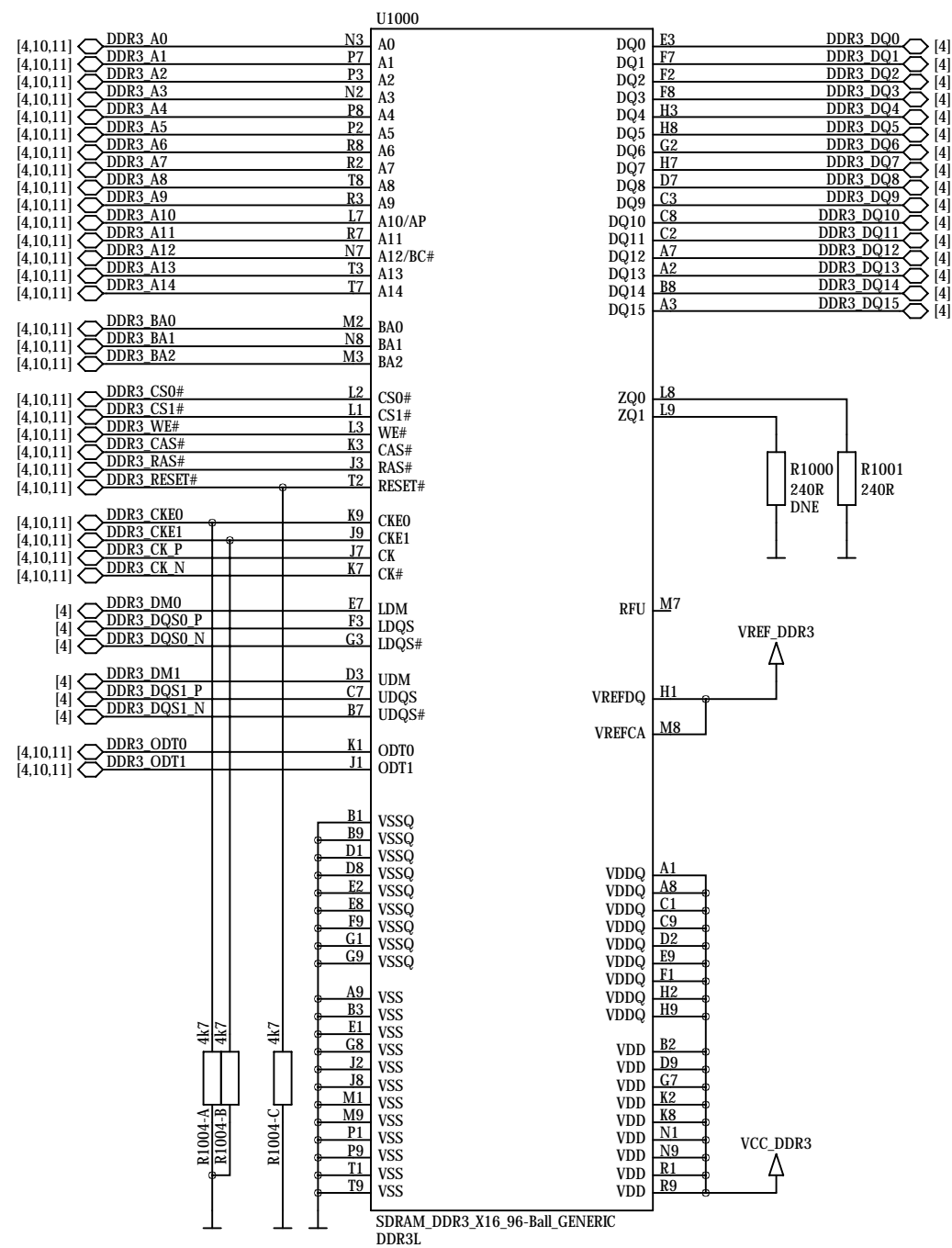
Quad SPI Flash



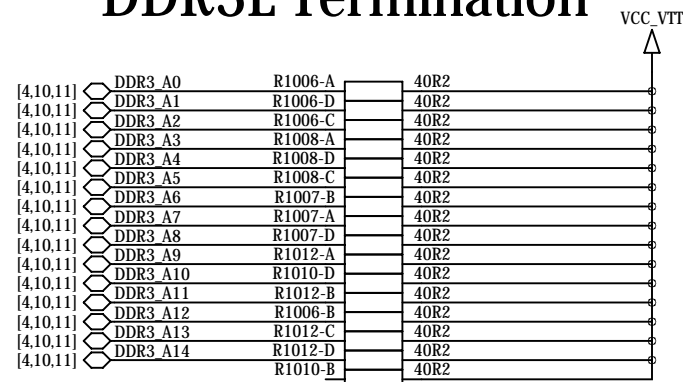
Flash Power



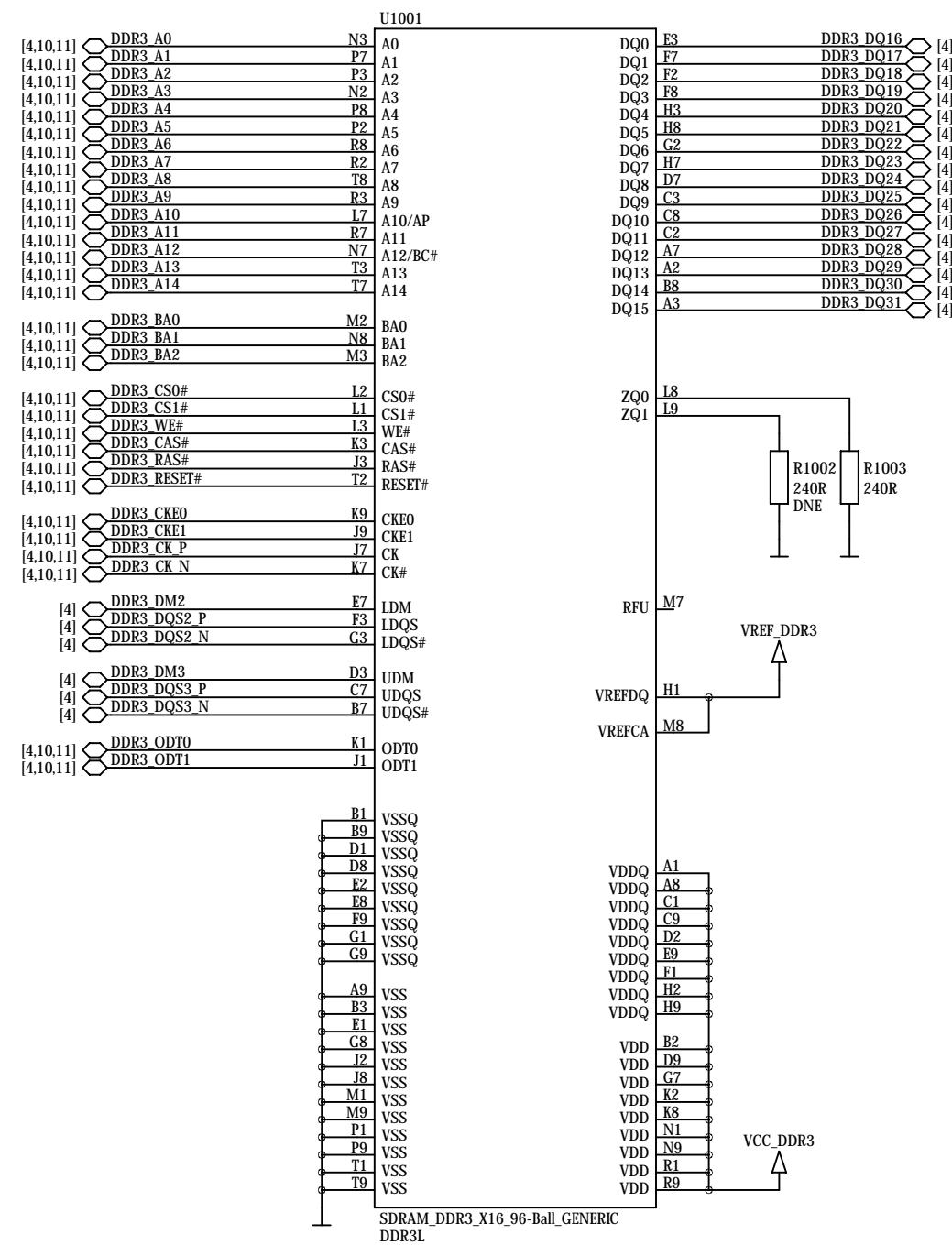
DDR3L SDRAM Bytes 0 - 1



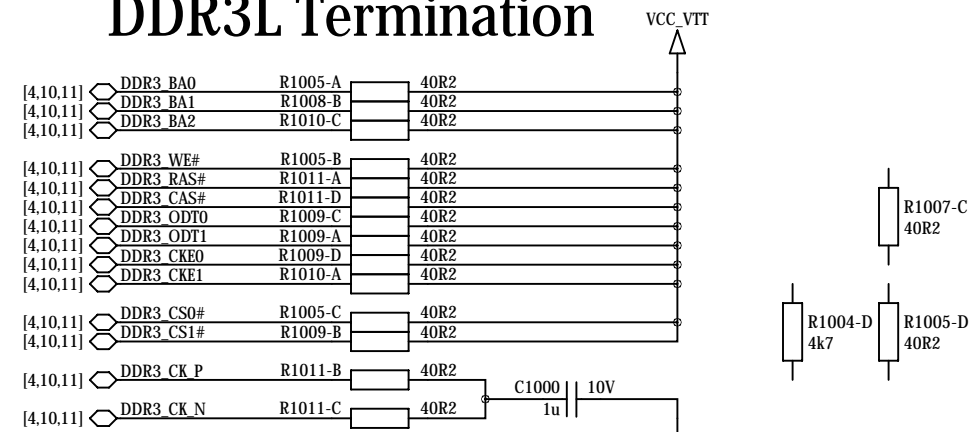
DDR3L Termination



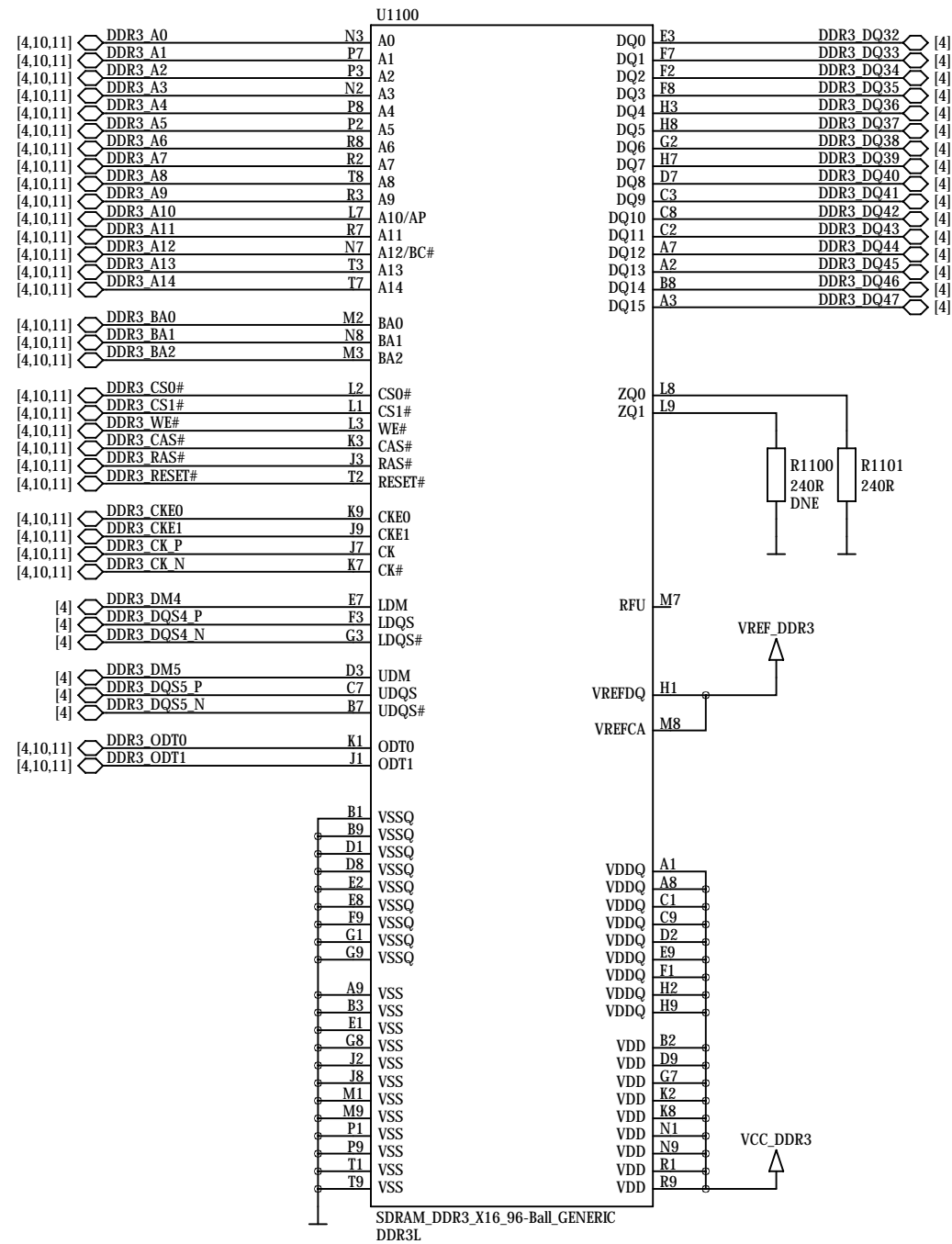
DDR3L SDRAM Bytes 2 - 3



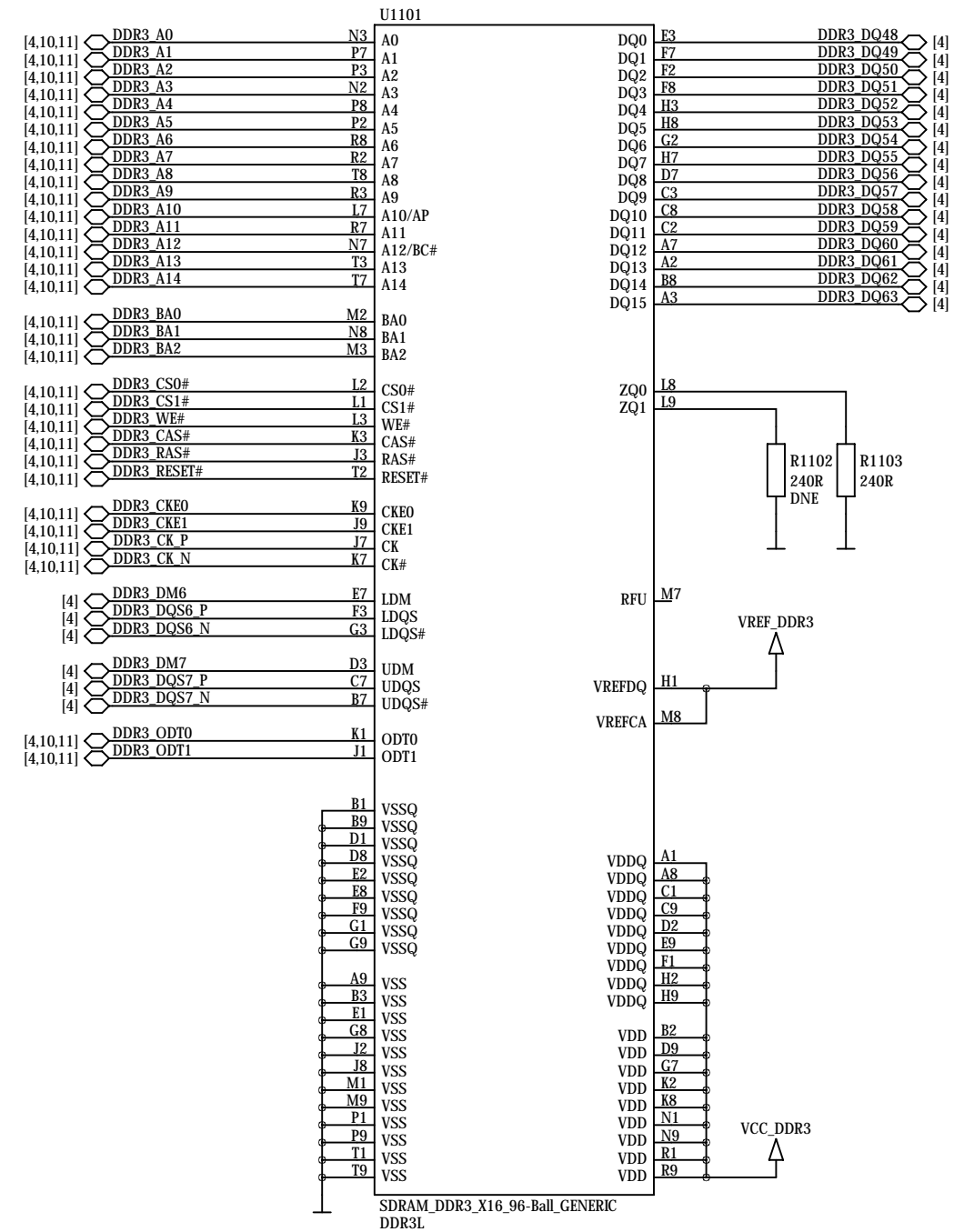
DDR3L Termination



DDR3L SDRAM Bytes 4 - 5



DDR3L SDRAM Bytes 6 - 7



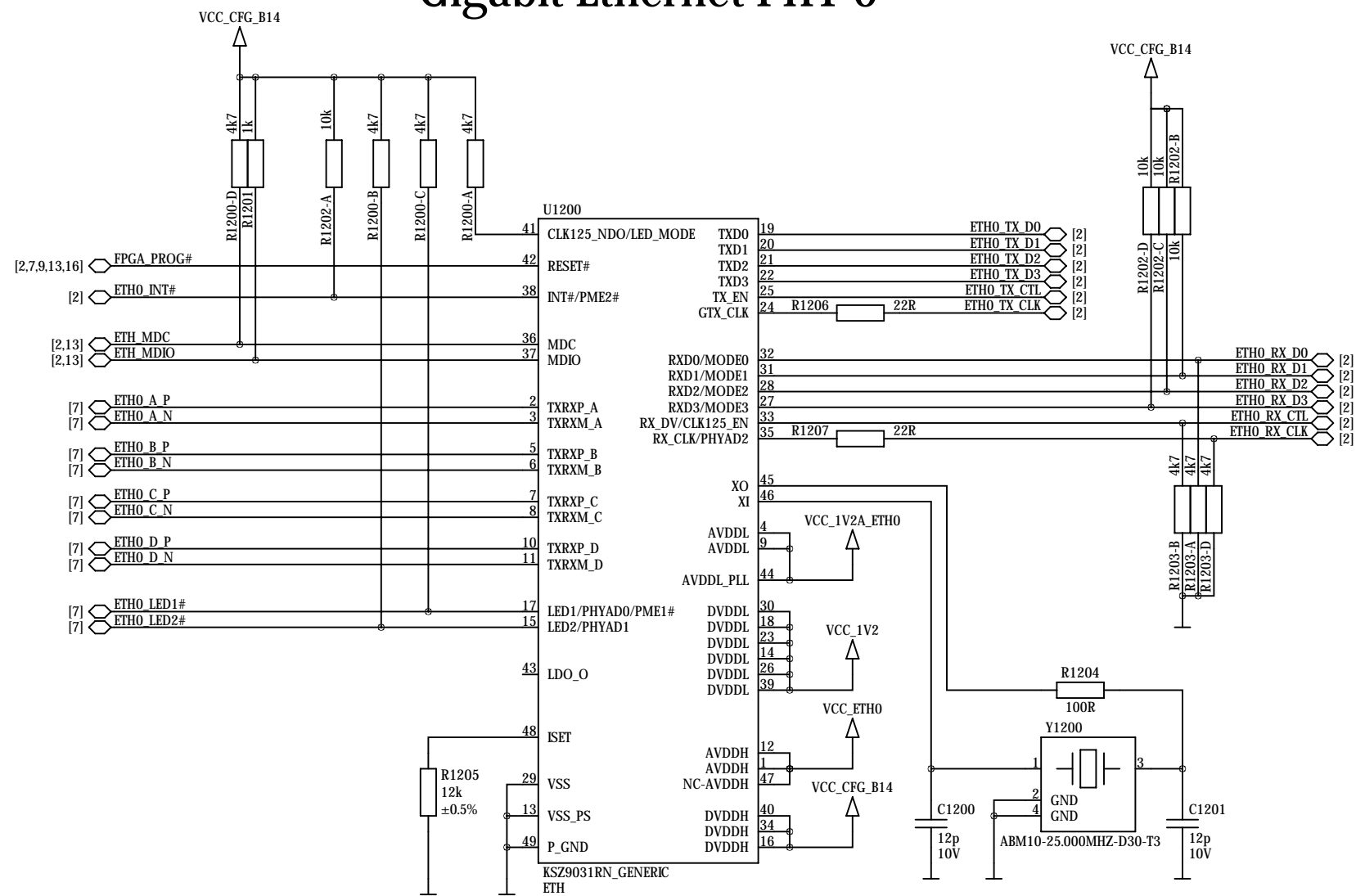
DDR3L Decoupling

not included in user schematics

This part is intentionally left blank.



Gigabit Ethernet PHY 0



MODE<3:0> = 1110 -> RGMII, all capabilities
LED_Mode Pull up = Single LED
PhyAddress <2:0> = 011 -> 3
LED1 and LED2 are active low

Ethernet Power Filter

not included in user schematics

This part is intentionally left blank.



D

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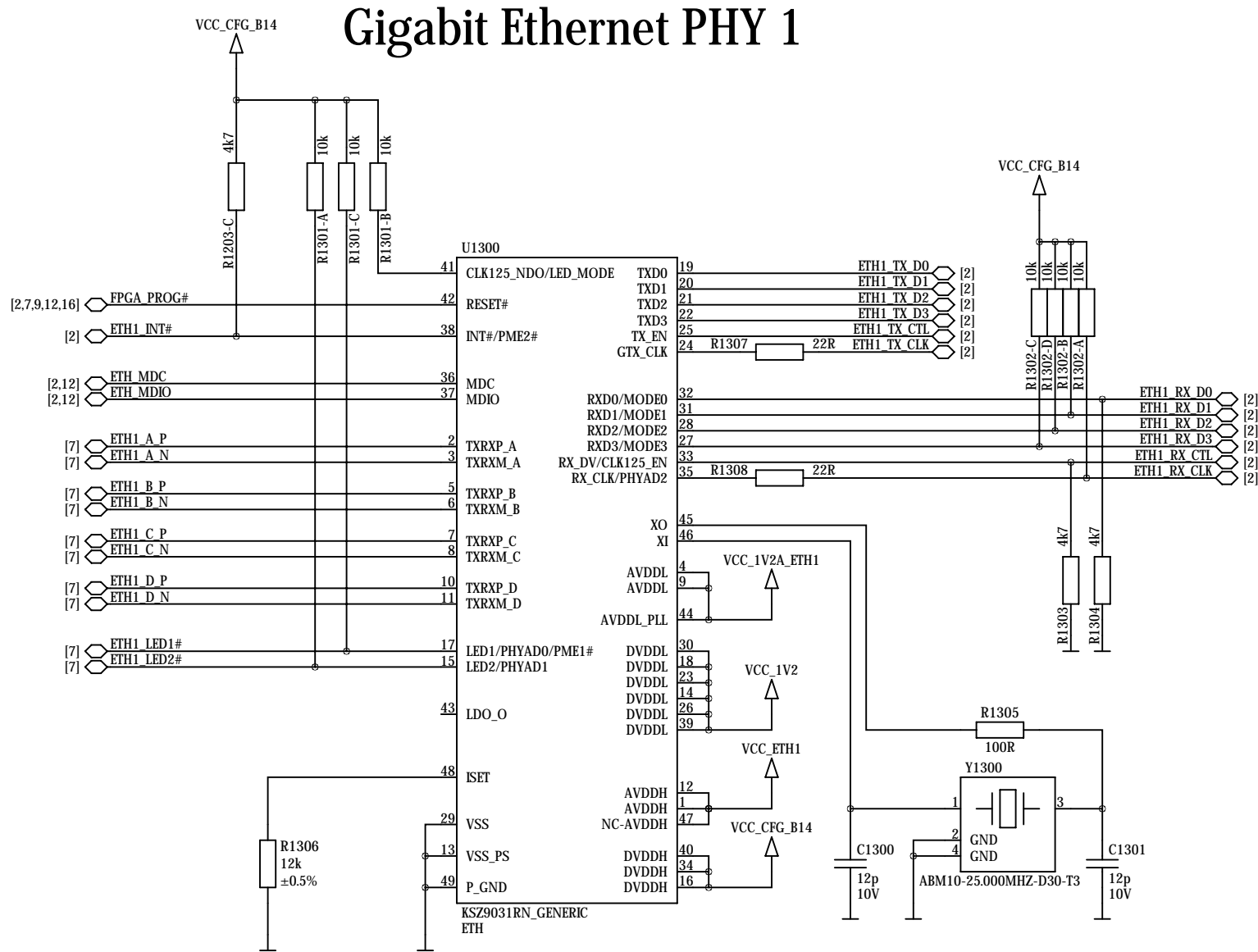
A

D

C

B

A



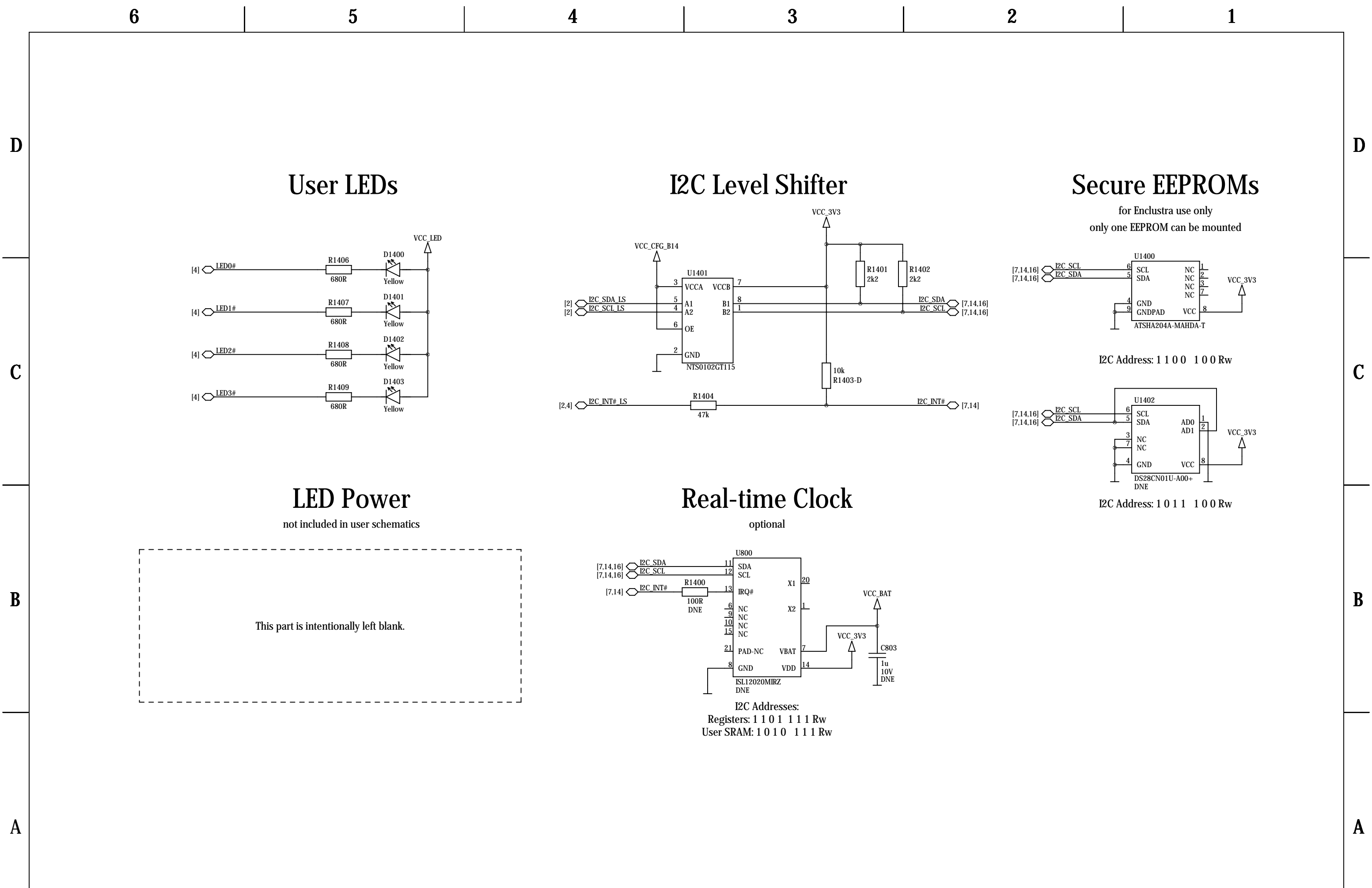
MODE<3:0> = 1110 -> RGMII, all capabilities
LED_Mode Pull up = Single LED
PhyAddress <2:0> = 111 -> 7
LED1 and LED2 are active low

Ethernet Power Filter

not included in user schematics

This part is intentionally left blank.





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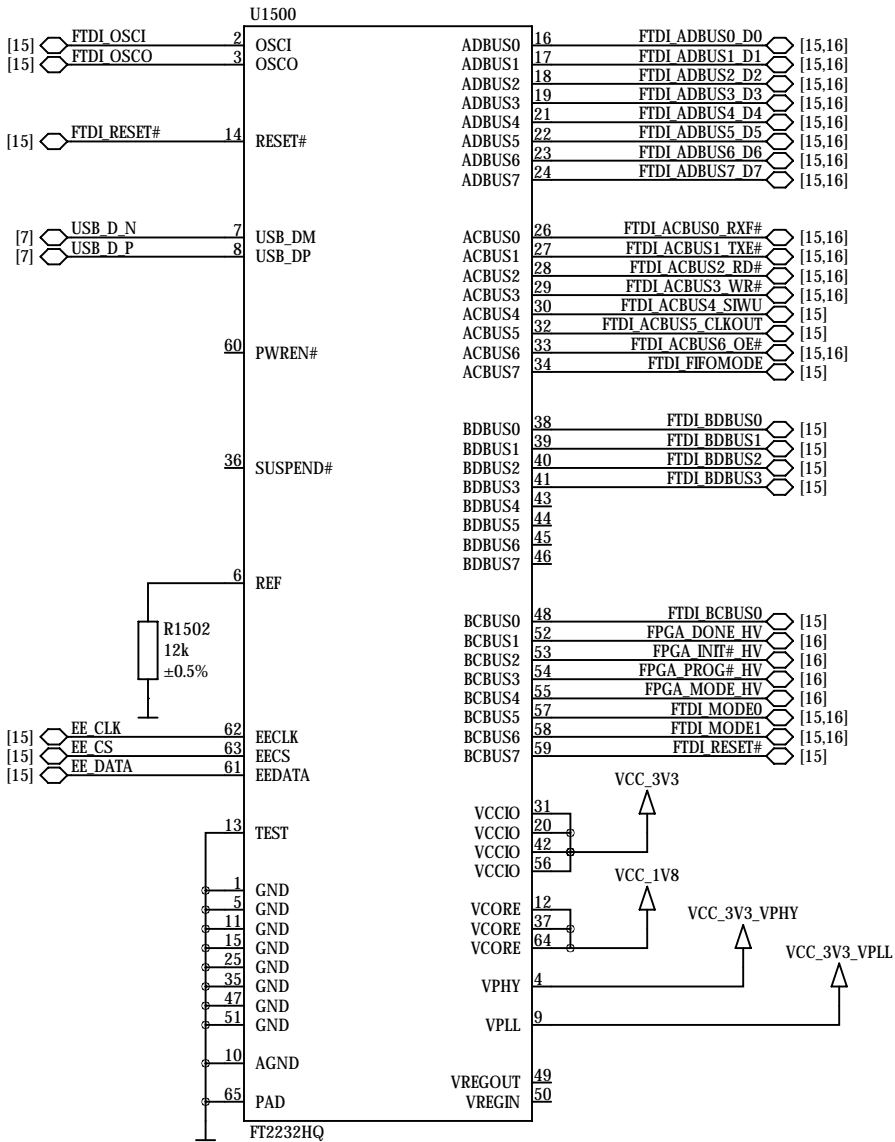
D

C

B

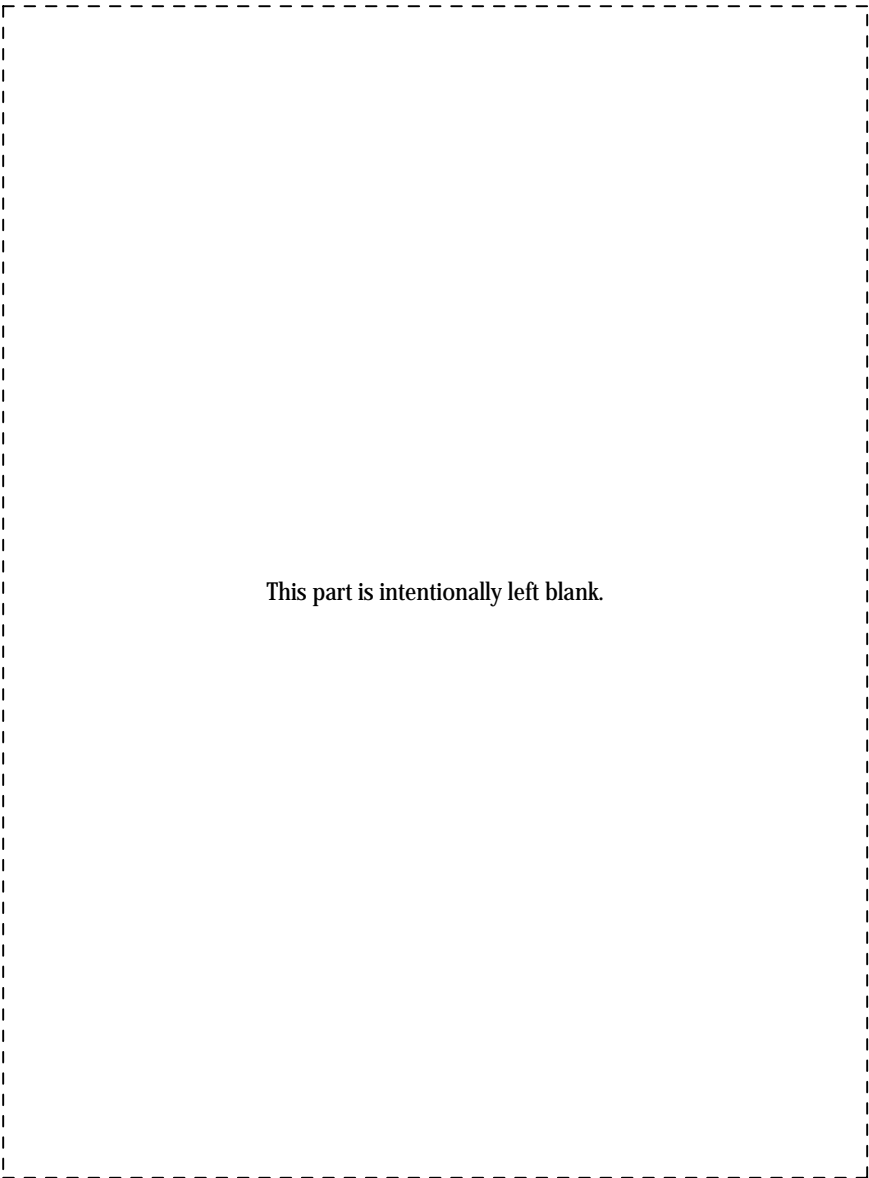
A

FTDI USB 2.0 Device Controller



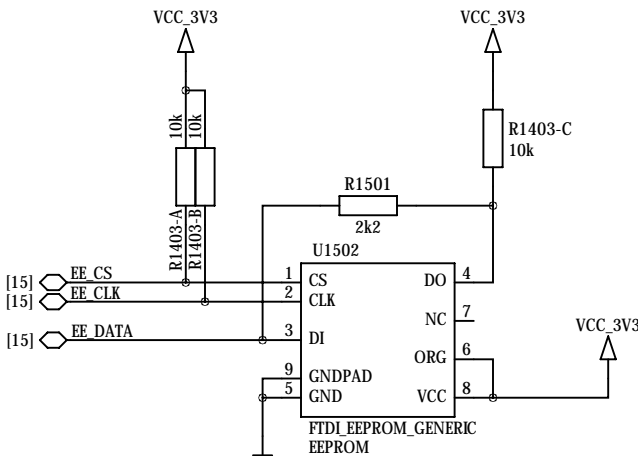
JTAG Adapter

not included in user schematics

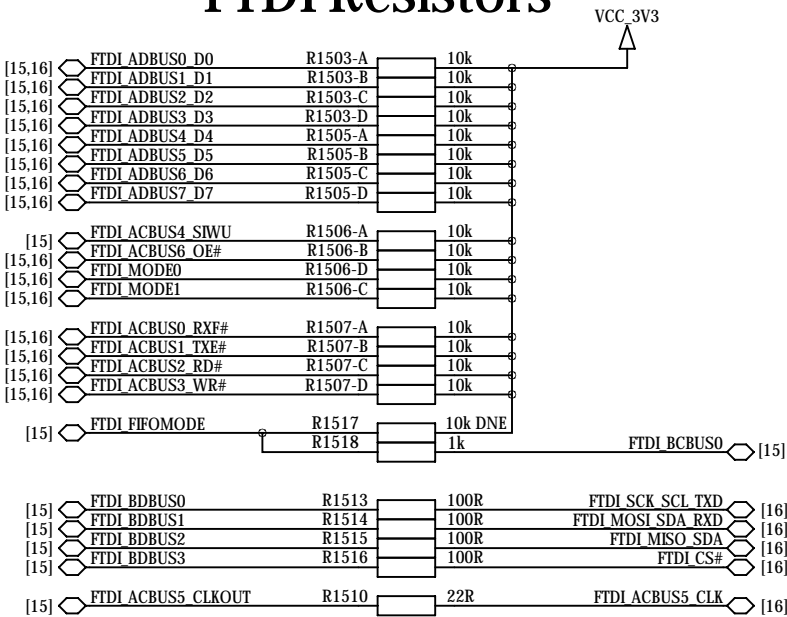


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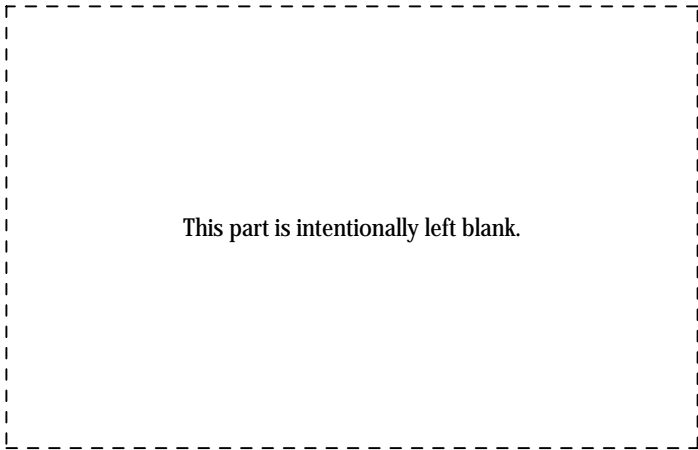
FTDI EEPROM



FTDI Resistors

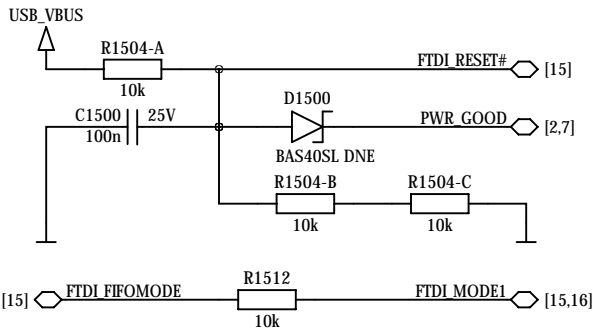


FTDI Power Filters

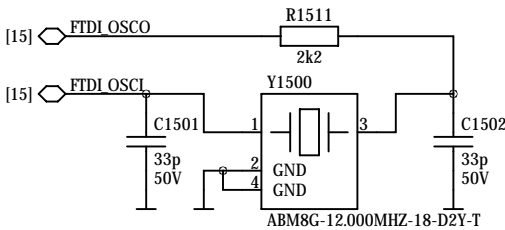


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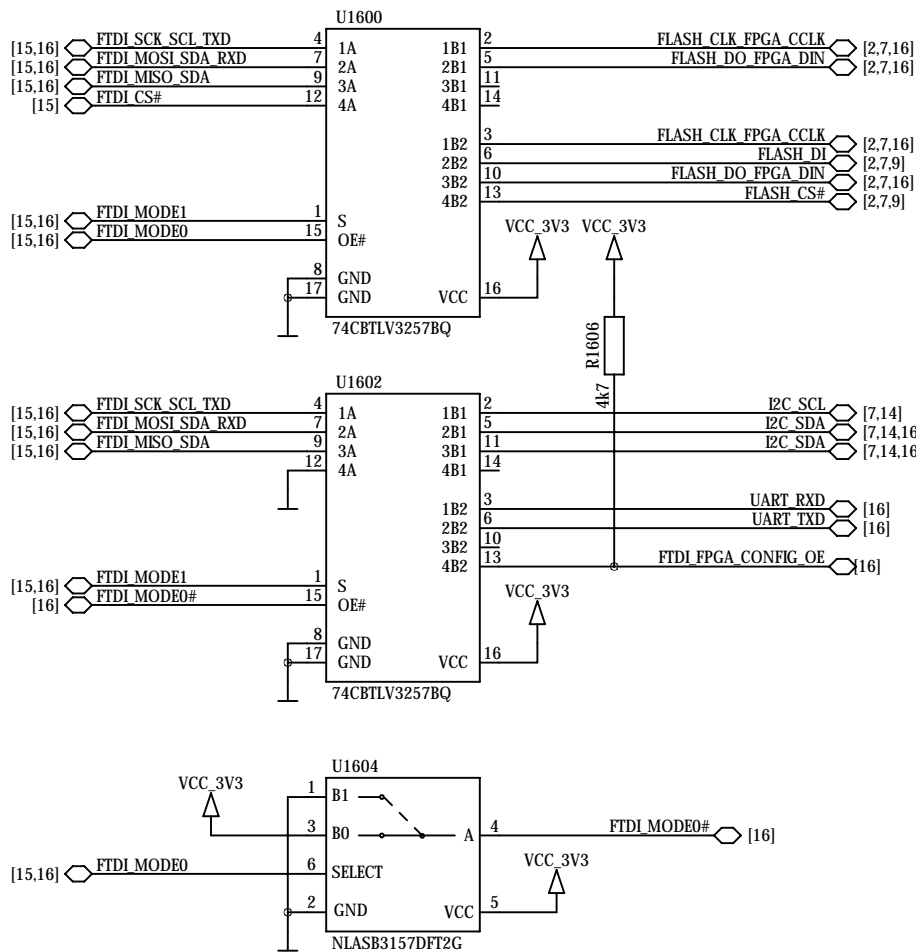
FTDI Reset



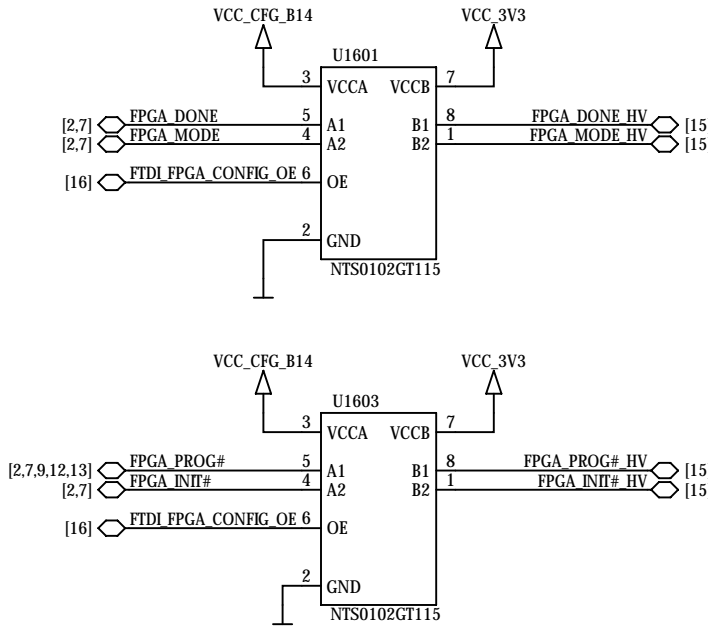
FTDI Clock



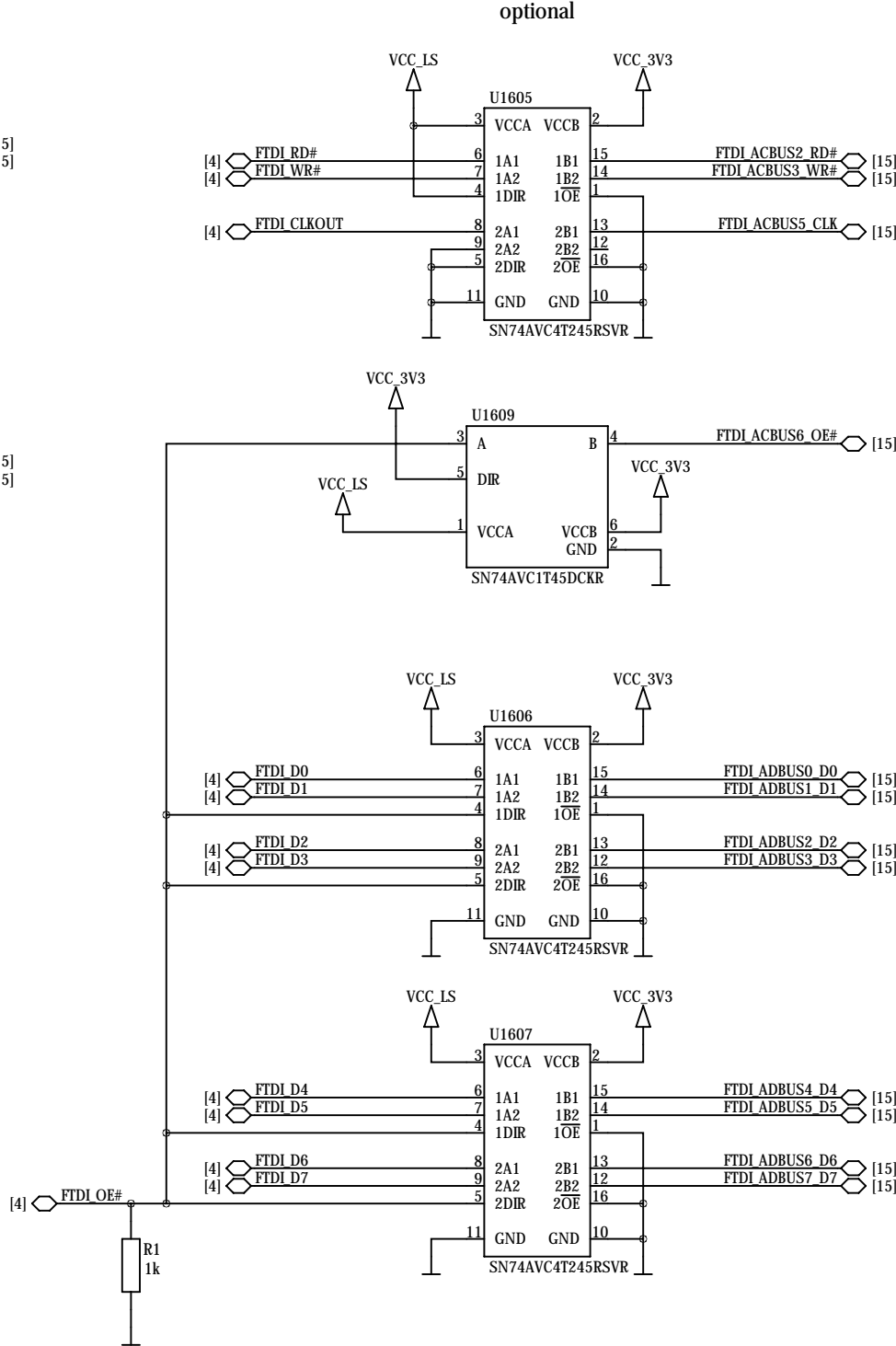
Configuration Multiplexers



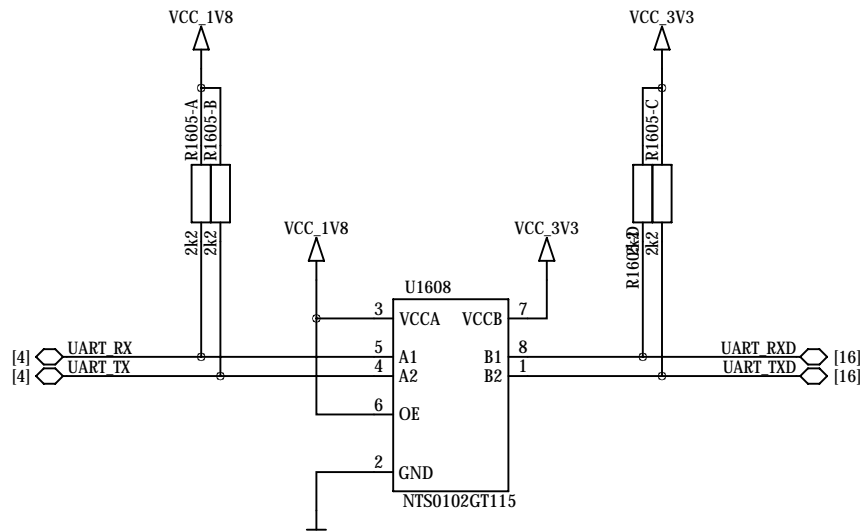
FTDI Status Level Shifters



FTDI FIFO Level Shifters



FTDI UART Level Shifters



Level Shifter Power

not included in user schematics

This part is intentionally left blank.

6

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Dual DC/DC Converter

channel 1: 1.35V/1.5V 2A 5%

channel 2: 2.5V 2A 5%

not included in user schematics

This part is intentionally left blank.

LDO 2.0V 0.5A

only assembled for FPGA in FFG package

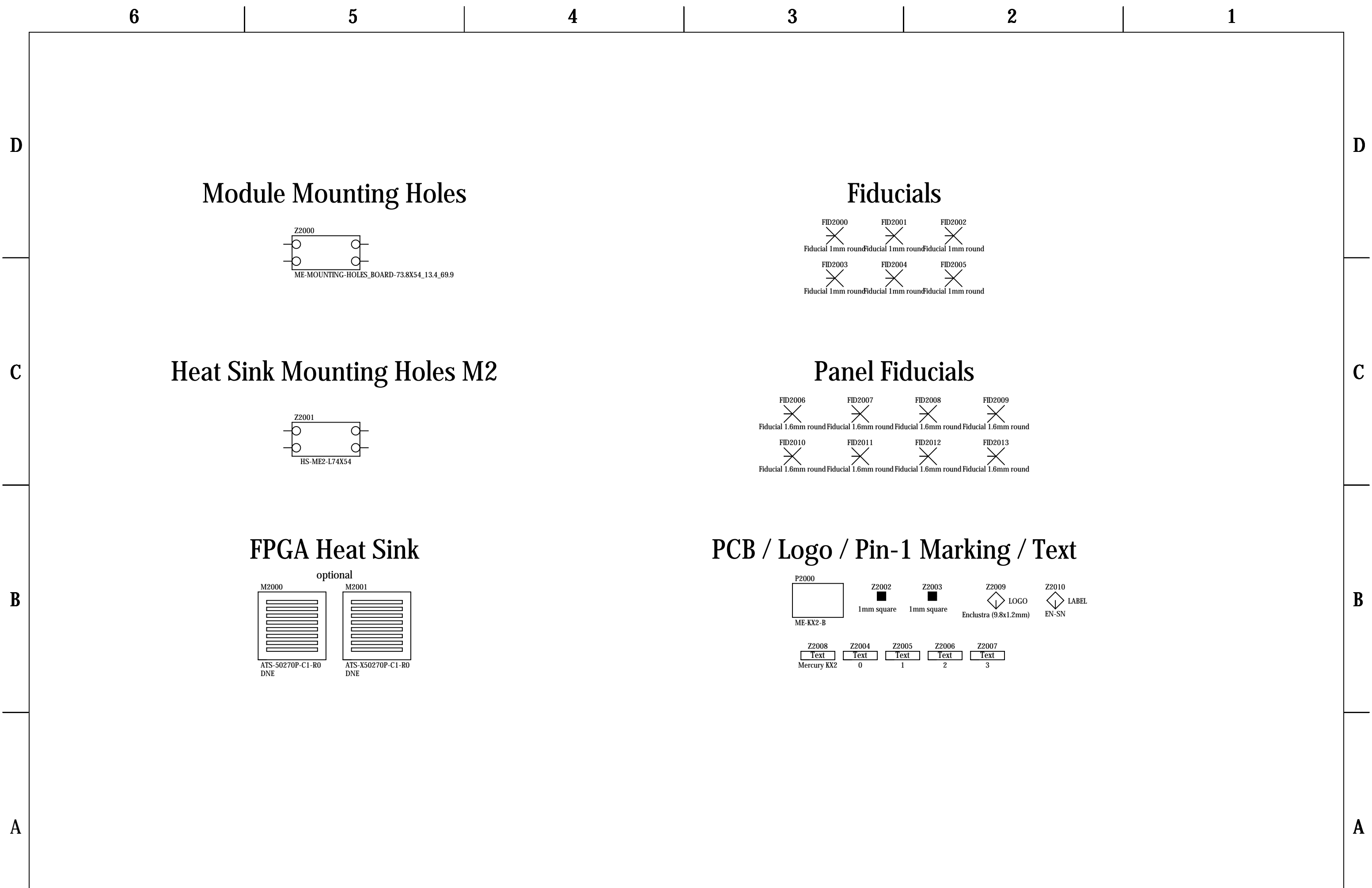
not included in user schematics

This part is intentionally left blank.

DDR3 Voltage Selection

	DDR3_VSEL	VCC_DDR3
Default	"Z"	1.5V
	"0"	1.35V
	"1"	Illegal

6		5		4		3		2		1									
D	<div>Dual DC/DC Converter</div> <div>channel 1: 1.2V 2A 2.8%</div> <div>channel 2: 1.8V 2A 3%</div> <div>not included in user schematics</div>											D							
	<div>This part is intentionally left blank.</div>											C							
C																			
	<div>IO Voltage Generation</div> <div>when C connector is not present on base board</div> <div>not included in user schematics</div>											C							
	<div>This part is intentionally left blank.</div>																		
B	<div>DDR3 Termination Voltage Regulator</div> <div>not included in user schematics</div>											B							
	<div>This part is intentionally left blank.</div>																		
A																			
	<div>VREF DDR3</div> <div>not included in user schematics</div>											A							
	<div>This part is intentionally left blank.</div>																		
<div><div></div><div>ENCLUSTRA</div></div>		Copyright	© 2017 by Enclustra GmbH			Sheet Name	19_POWER_1.2V_1.8V_VTT			Customer No	0000		Revision	R2.2		DNE = do not equip		Confidential	
		Company	Enclustra GmbH			Project	Mercury+ KX2			Project No	430		Designed	MHEI		Date	2 Mar 2017		Sheet/sheets



Component Variants

FPGA	DDR3L	Ethernet PHY	OSC100	OSC200	EEPROM	L0U68	L1U	LDO2V0
<div><div>Part</div><div>U200A XC7K160T-1FBG676C EN100565</div></div> <div><div>Part</div><div>U200B XC7K160T-2FFG676I EN101565</div></div> <div><div>Part</div><div>U200C XC7K325T-2FFG676I EN100566</div></div> <div><div>Part</div><div>U200D XC7K410T-2FFG676I EN100571</div></div>	<div><div>Part</div><div>U1000A NT5CC128M16P-DI EN100912</div></div> <div><div>Part</div><div>U1000B:1 H5TC4G63CFR-RDI EN101580</div></div> <div><div>Part</div><div>U1000B:2 NT5CC256M16DP-EKI EN101581</div></div> <div><div>Part</div><div>U1001A NT5CC128M16P-DI EN100912</div></div> <div><div>Part</div><div>U1001B:1 H5TC4G63CFR-RDI EN101580</div></div> <div><div>Part</div><div>U1001B:2 NT5CC256M16DP-EKI EN101581</div></div> <div><div>Part</div><div>U1100A NT5CC128M16P-DI EN100912</div></div> <div><div>Part</div><div>U1100B:1 H5TC4G63CFR-RDI EN101580</div></div> <div><div>Part</div><div>U1100B:2 NT5CC256M16DP-EKI EN101581</div></div>	<div><div>Part</div><div>U1200A KSZ9031RNXCA EN100202</div></div> <div><div>Part</div><div>U1200B KSZ9031RNXIA EN100203</div></div> <div><div>Part</div><div>U1300A KSZ9031RNXCA EN100202</div></div> <div><div>Part</div><div>U1300B KSZ9031RNXIA EN100203</div></div>	<div><div>Part</div><div>Y900A ASDMB-100.000MHZ-LY-T EN100284</div></div> <div><div>Part</div><div>Y900B ASEMB-100.000MHZ-LY-T EN101056</div></div>	<div><div>Part</div><div>Y904A:1 DSC1123C12-200.0000T EN101130</div></div> <div><div>Part</div><div>Y904A:2 ASDMPLV-200.000MHZ-LR-T EN100881</div></div> <div><div>Part</div><div>Y904B ASEMPLV-200.000MHZ-LR EN100880</div></div>	<div><div>Part</div><div>U1502A CAT93C66VP2I-GT3 EN101255</div></div> <div><div>Part</div><div>U1502B 93AA66C-VMS EN100279</div></div>	<div><div>Part</div><div>L1700A 0u68 EN100848</div></div> <div><div>Part</div><div>L1700B 1u EN100436</div></div>	<div><div>Part</div><div>L1801A 1u EN100784</div></div> <div><div>Part</div><div>L1801B 1u EN100917</div></div> <div><div>Part</div><div>L1803A 1u EN100784</div></div> <div><div>Part</div><div>L1803B 1u EN100917</div></div> <div><div>Part</div><div>L1901A 1u EN100784</div></div> <div><div>Part</div><div>L1901B 1u EN100917</div></div> <div><div>Part</div><div>L1903A 1u EN100784</div></div> <div><div>Part</div><div>L1903B 1u EN100917</div></div>	U1802/R1811

Assembly Variants

Assembly Variant	FPGA	DDR3L	Ethernet PHY	OSC100	OSC200	EEPROM	LOU68	L1U	LDO2V0
<div>Variant</div> EN101775:0 ME-KX2-160-1C-D10-R2	<div>Option</div> EN101775:1 FPGA EN100565	<div>Option</div> EN101775:2 DDR3L EN100912	<div>Option</div> EN101775:3 ETH EN100203	<div>Option</div> EN101775:4 OSC100 EN100284	<div>Option</div> EN101775:5 OSC200 EN101130	<div>Option</div> EN101775:6 EEPROM EN101255	<div>Option</div> EN101775:7 LOU68 EN100848	<div>Option</div> EN101775:8 L1U EN100784	<div>Option</div> EN101775:9 LDO2V0 DNE
<div>Variant</div> EN101776:0 ME-KX2-160-2I-D11-P-R2	<div>Option</div> EN101776:1 FPGA EN101565	<div>Option</div> EN101776:2 DDR3L EN101580	<div>Option</div> EN101776:3 ETH EN100203	<div>Option</div> EN101776:4 OSC100 EN100284	<div>Option</div> EN101776:5 OSC200 EN101130	<div>Option</div> EN101776:6 EEPROM EN101255	<div>Option</div> EN101776:7 LOU68 EN100848	<div>Option</div> EN101776:8 L1U EN100784	<div>Option</div> EN101776:9 LDO2V0
<div>Variant</div> EN101777:0 ME-KX2-325-2I-D11-P-R2	<div>Option</div> EN101777:1 FPGA EN100566	<div>Option</div> EN101777:2 DDR3L EN101580	<div>Option</div> EN101777:3 ETH EN100203	<div>Option</div> EN101777:4 OSC100 EN100284	<div>Option</div> EN101777:5 OSC200 EN101130	<div>Option</div> EN101777:6 EEPROM EN101255	<div>Option</div> EN101777:7 LOU68 EN100848	<div>Option</div> EN101777:8 L1U EN100784	<div>Option</div> EN101777:9 LDO2V0
<div>Variant</div> EN101778:0 ME-KX2-410-2I-D11-P-R2	<div>Option</div> EN101778:1 FPGA EN100571	<div>Option</div> EN101778:2 DDR3L EN101580	<div>Option</div> EN101778:3 ETH EN100203	<div>Option</div> EN101778:4 OSC100 EN100284	<div>Option</div> EN101778:5 OSC200 EN101130	<div>Option</div> EN101778:6 EEPROM EN101255	<div>Option</div> EN101778:7 LOU68 EN100848	<div>Option</div> EN101778:8 L1U EN100784	<div>Option</div> EN101778:9 LDO2V0

