Enclustra User Schematics

Disclaimer

User schematics do not include proprietary Enclustra design elements, such as power supply circuits. These circuits use optimized designs which are extremely compact and remain proprietary to Enclustra. The user manual provides all necessary information to use the module and its interfaces.

User schematics are provided after purchase of Enclustra hardware, and may also be provided in certain cases before purchase, to assist in product evaluation.
No part of the schematics may be copied or modified without written permission from Enclustra.

Full schematics, including a full bill-of-materials, are available through the purchase of a hardware licence for the product in question.
Please contact Enclustra Sales for more information.

Note: DNE = Do Not Equip (parts not equipped by default)

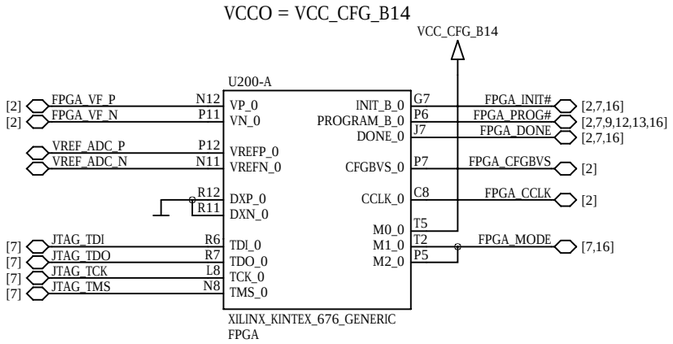
Mercury+ KX2 FPGA Module

Revision 2.2

Sheet Name	1_COVER	Customer No	0000	Revision	R2.2	DNE = do not equip	Confidential
Project	Mercury+ KX2	Project No	430	Designed	MHEI	Date 2 Mar 2017	Sheet/sheets 1 / 21

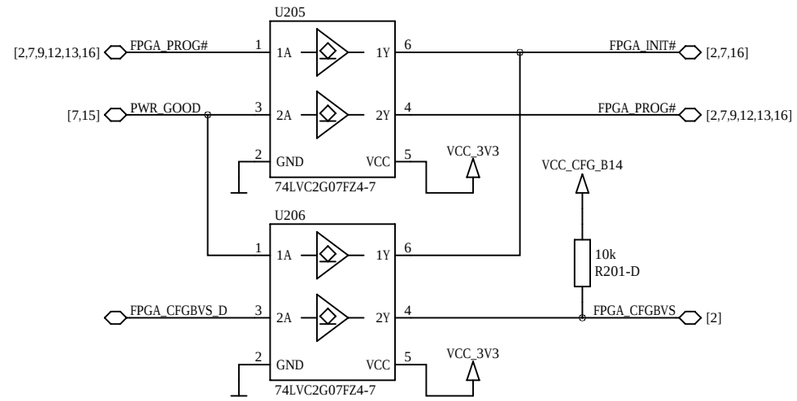
FPGA Bank 0

VCCO = VCC_CFG_B14



TDI and TMS have internal pullups.

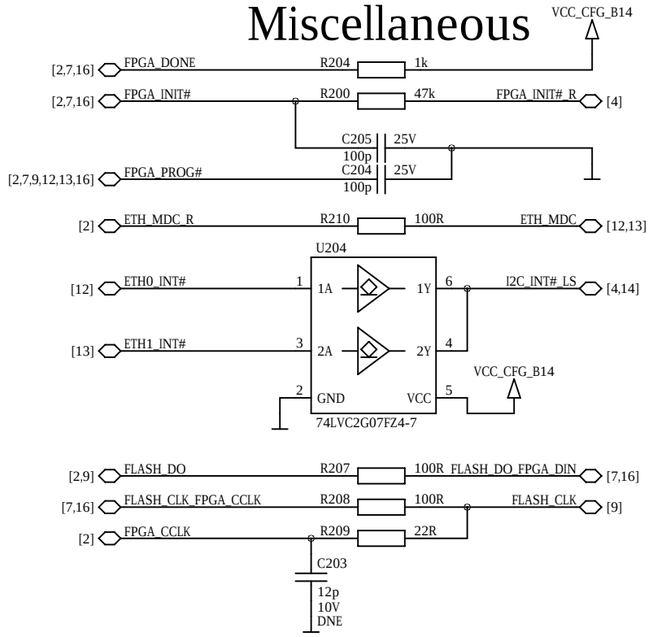
Reset Circuit



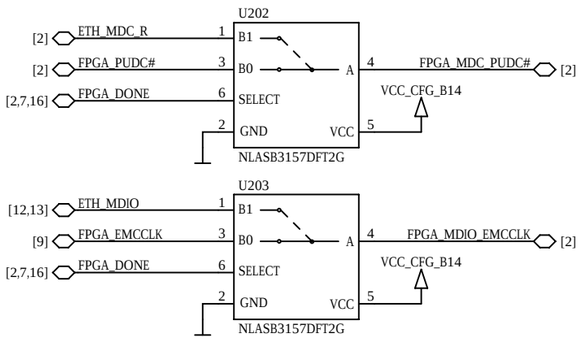
FPGA Mode

		Configuration
Default	0	Active Serial
	1	Passive Serial

Miscellaneous



MDIO Multiplexer



Voltage Select Detection

not included in user schematics

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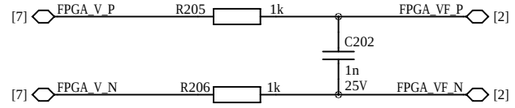
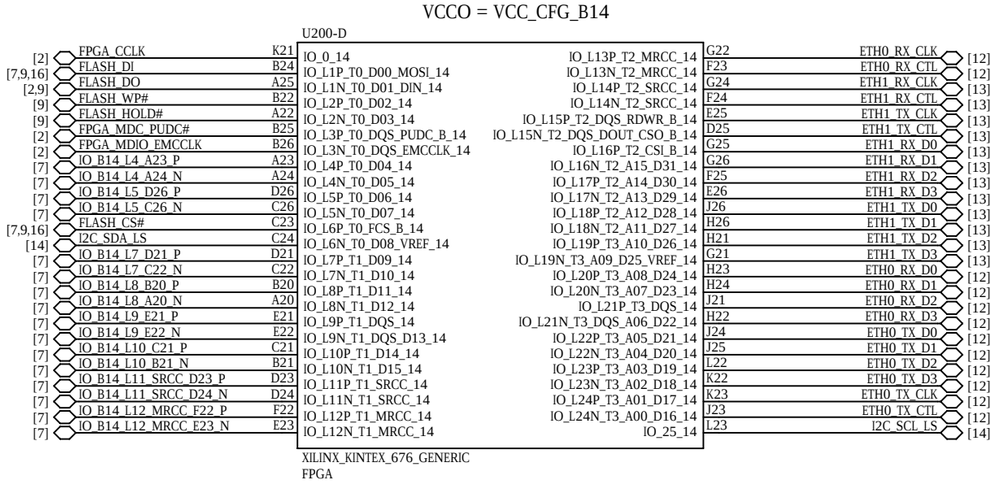
Pull-Up During Configuration

ADC Anti-Alias Filter



FPGA Bank 14

VCCO = VCC_CFG_B14

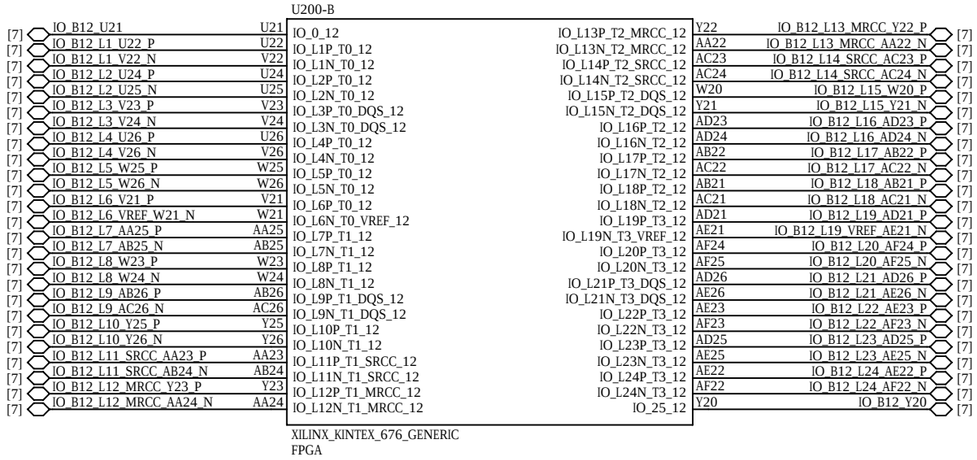


ENCLUSTRA	Copyright	© 2017 by Enclustra GmbH	Sheet Name	2_FPGA_BANKS_0_14_CONFIG	Customer No	0000	Revision	R2.2	DNE = do not equip	Confidential
	Company	Enclustra GmbH	Project	Mercury+ KX2	Project No	430	Designed	MHEI	Date	2 Mar 2017	Sheet/sheets	2 / 21

FPGA Bank 12

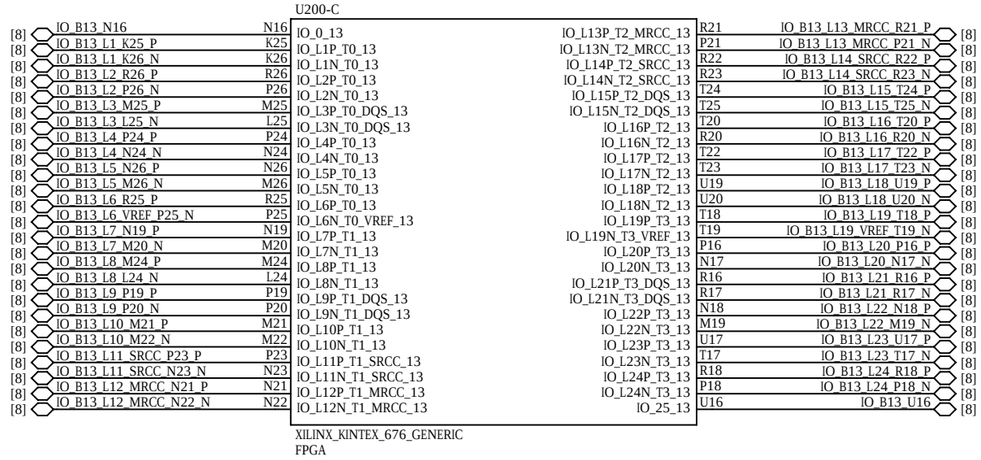
VCCO = VCC_IO_B12

Bank is not available in XC7K70T



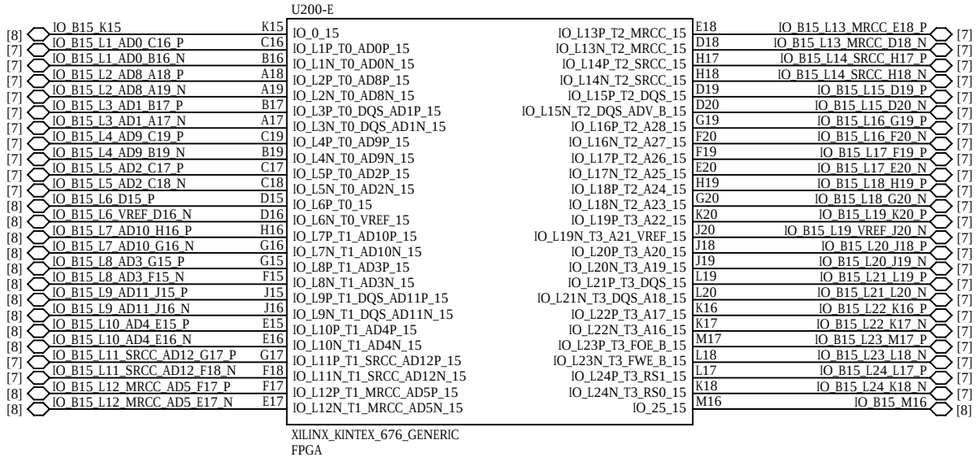
FPGA Bank 13

VCCO = VCC_IO_B13



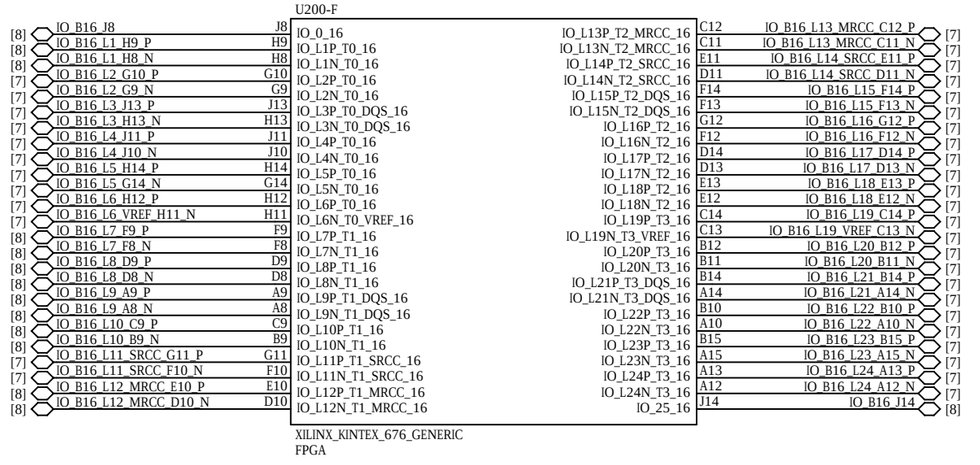
FPGA Bank 15

VCCO = VCC_IO_B15

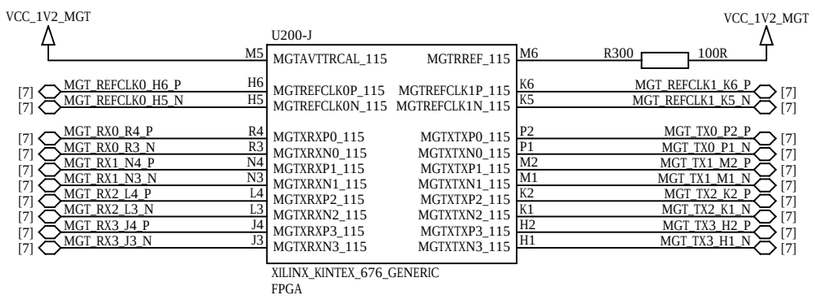


FPGA Bank 16

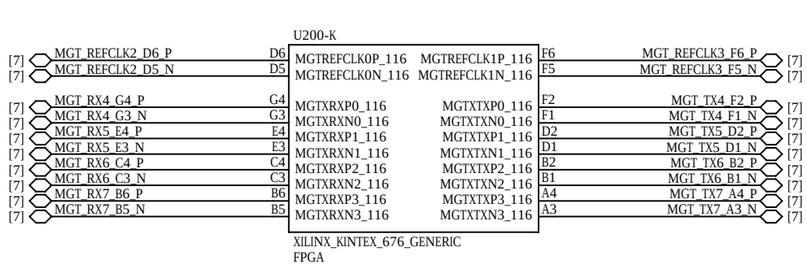
VCCO = VCC_IO_B16



FPGA MGT Bank 115



FPGA MGT Bank 116



ENCLUSTRA	Copyright © 2017 by Enclustra GmbH	Sheet Name 3_FPGA_BANKS_12_13_15_16_MGT	Customer No 0000	Revision R2.2	DNE = do not equip	Confidential
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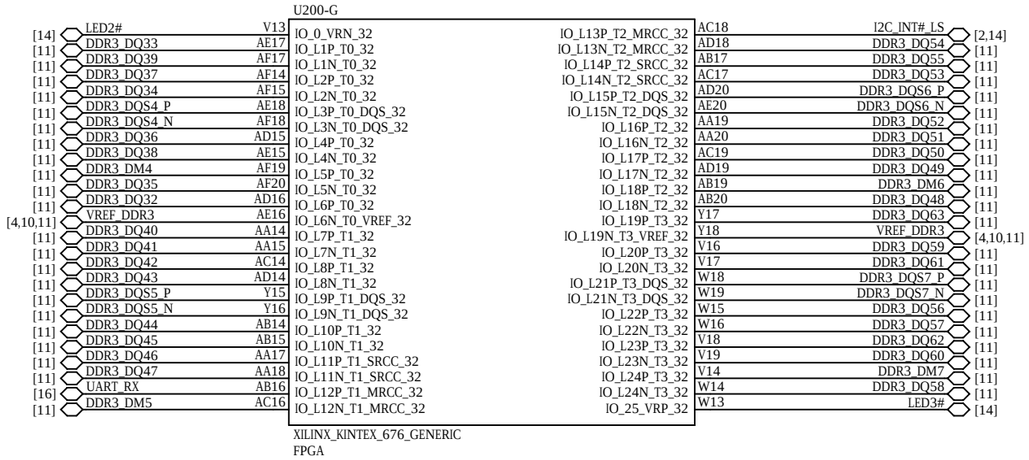
FPGA Bank 32

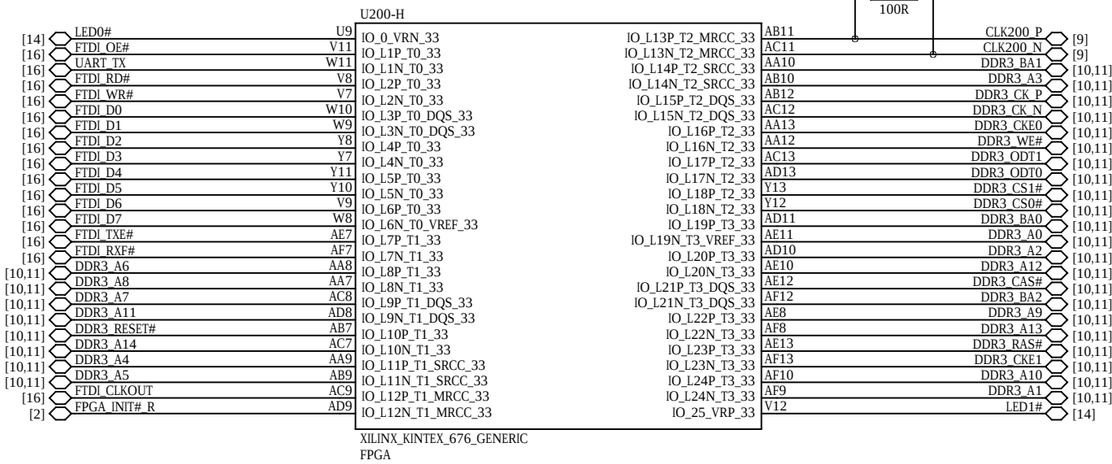
VCCO = VCC_DDR3

Bank is not available in XC7K70T



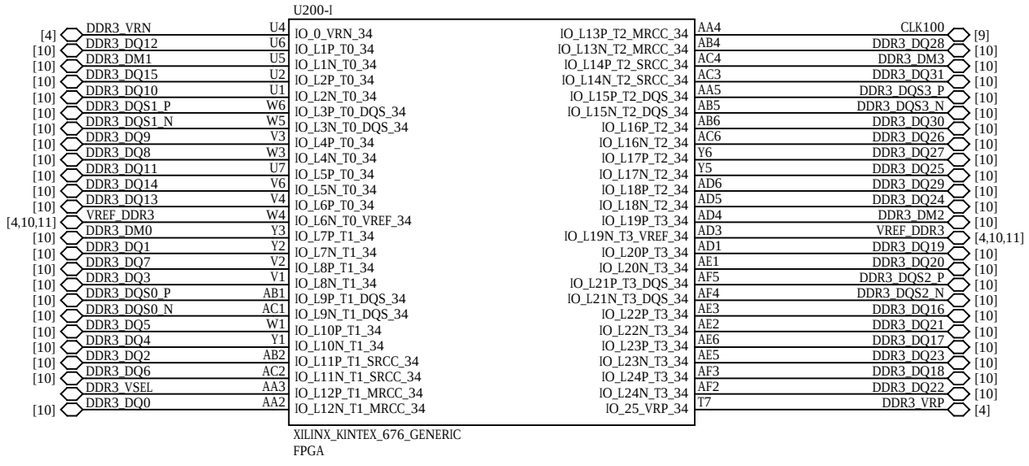
FPGA Bank 33

VCCO = VCC_DDR3

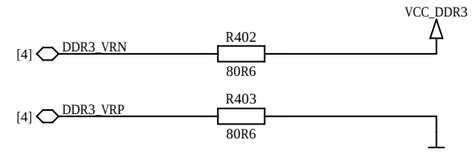


FPGA Bank 34

VCCO = VCC_DDR3



FPGA Driver Calibration



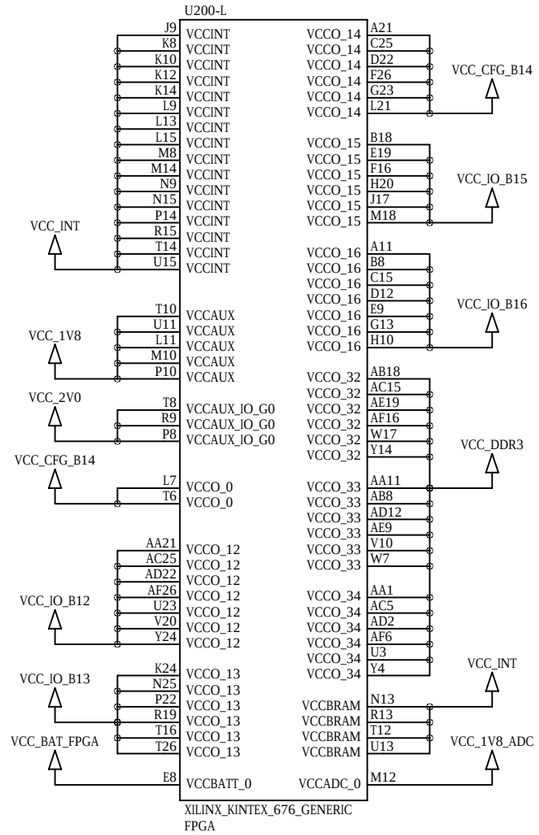
DDR3 VREF Decoupling

not included in user schematics

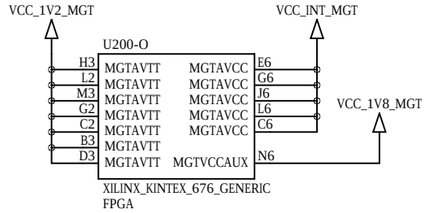
This part is intentionally left blank.

Company	Enclustra GmbH	Sheet Name	4_FPGA_BANKS_32_33_34	Customer No	0000	Revision	R2.2	DNE = do not equip	Confidential
		Project	Mercury+ KX2	Project No	430	Designed	MHEI	Date 2 Mar 2017	Sheet/sheets 4 / 21

FPGA Power



FPGA MGT Power



MGT Power Filters

not included in user schematics

This part is intentionally left blank.

FPGA ADC Supply Filter

not included in user schematics

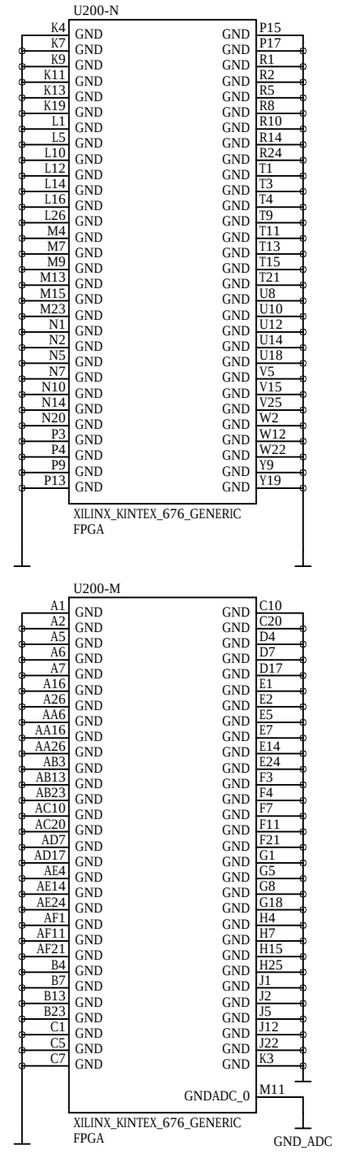
This part is intentionally left blank.

Analog Reference Voltage

not included in user schematics

This part is intentionally left blank.

FPGA Ground



ENCLUSTRA	Copyright	© 2017 by Enclustra GmbH	Sheet Name	5_FPGA_POWER	Customer No	0000	Revision	R2.2	DNE = do not equip	Confidential
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FPGA Decoupling

not included in user schematics

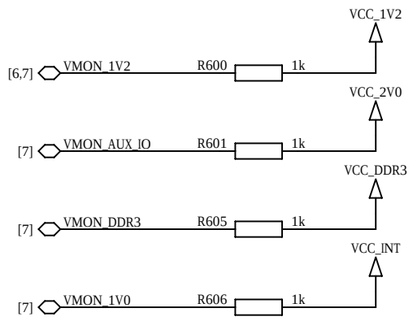
This part is intentionally left blank.

Power Decoupling

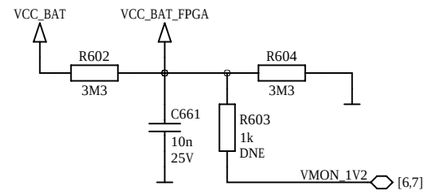
not included in user schematics

This part is intentionally left blank.

Voltage Monitoring

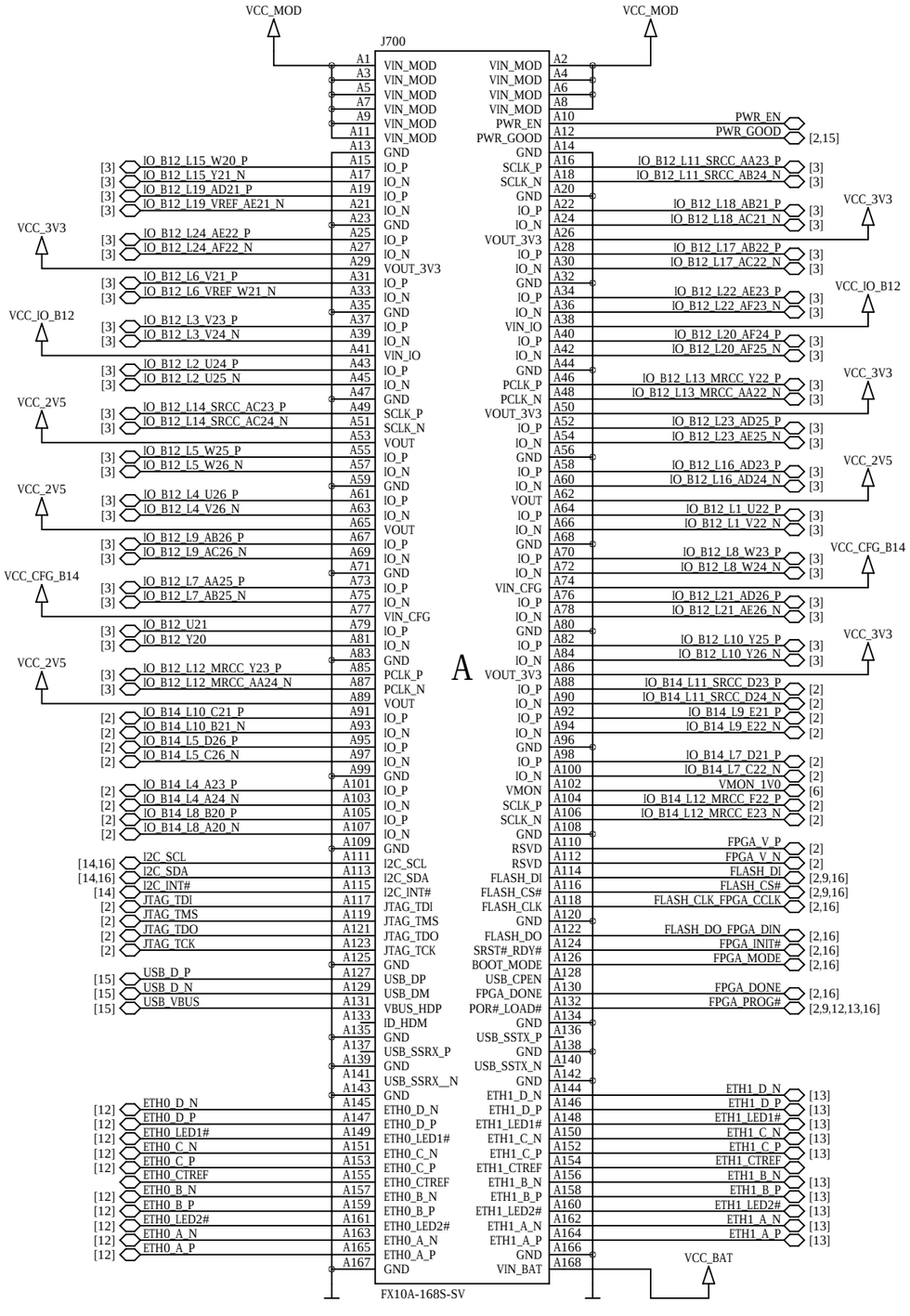


FPGA Battery Voltage

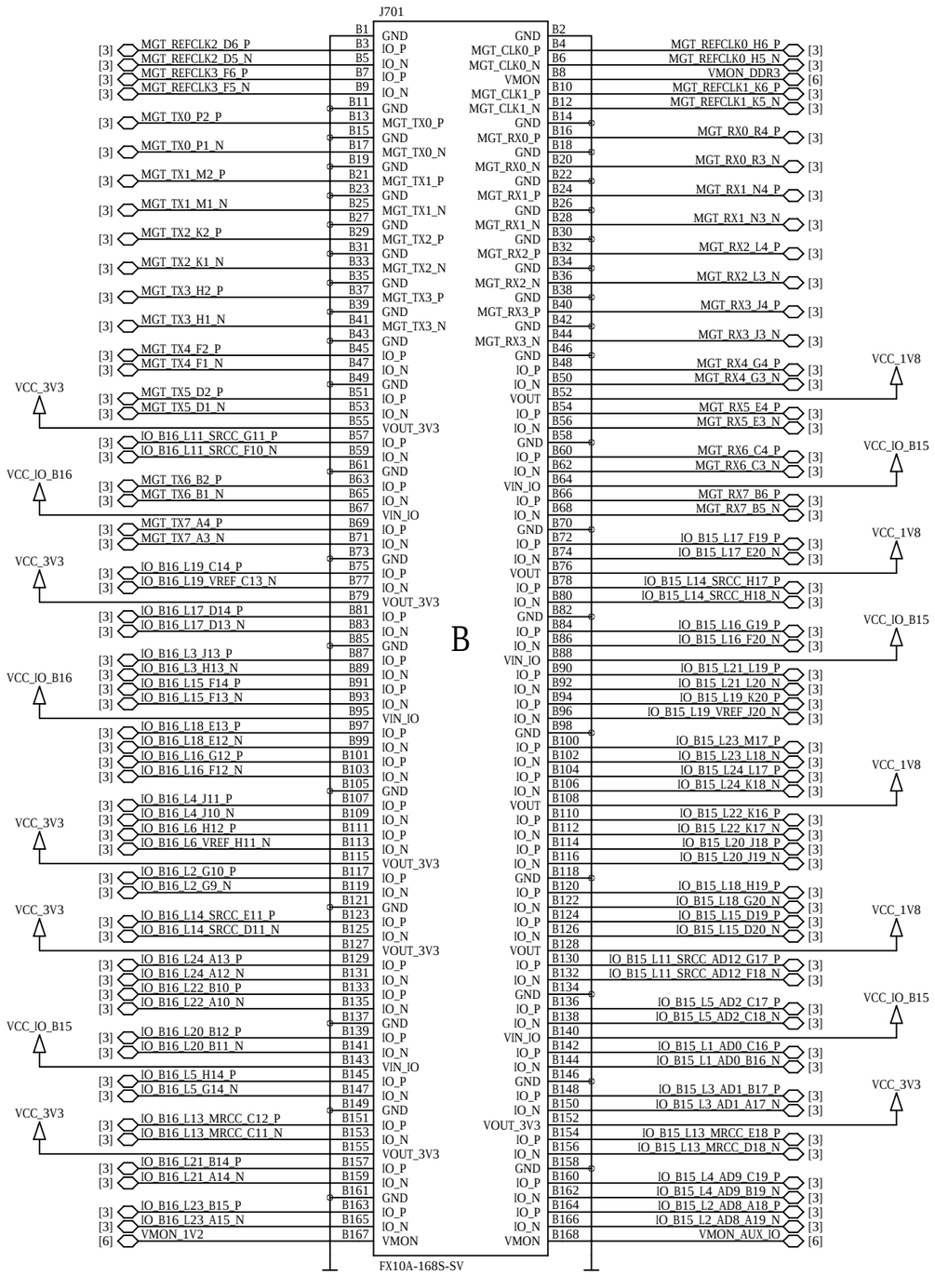


ENCLUSTRA	Copyright © 2017 by Enclustra GmbH	Sheet Name 6_FPGA_DECOUPLING	Customer No 0000	Revision R2.2	DNE = do not equip	Confidential	
	Company Enclustra GmbH	Project Mercury+ KX2	Project No 430	Designed MHEI	Date 2 Mar 2017	Sheet/sheets 6 / 21	

Module Connector A



Module Connector B



ENCLUSTRA	Copyright © 2017 by Enclustra GmbH	Sheet Name 7_MODULE_CONNECTORS_A_B	Customer No 0000	Revision R2.2	DNE = do not equip	Confidential	
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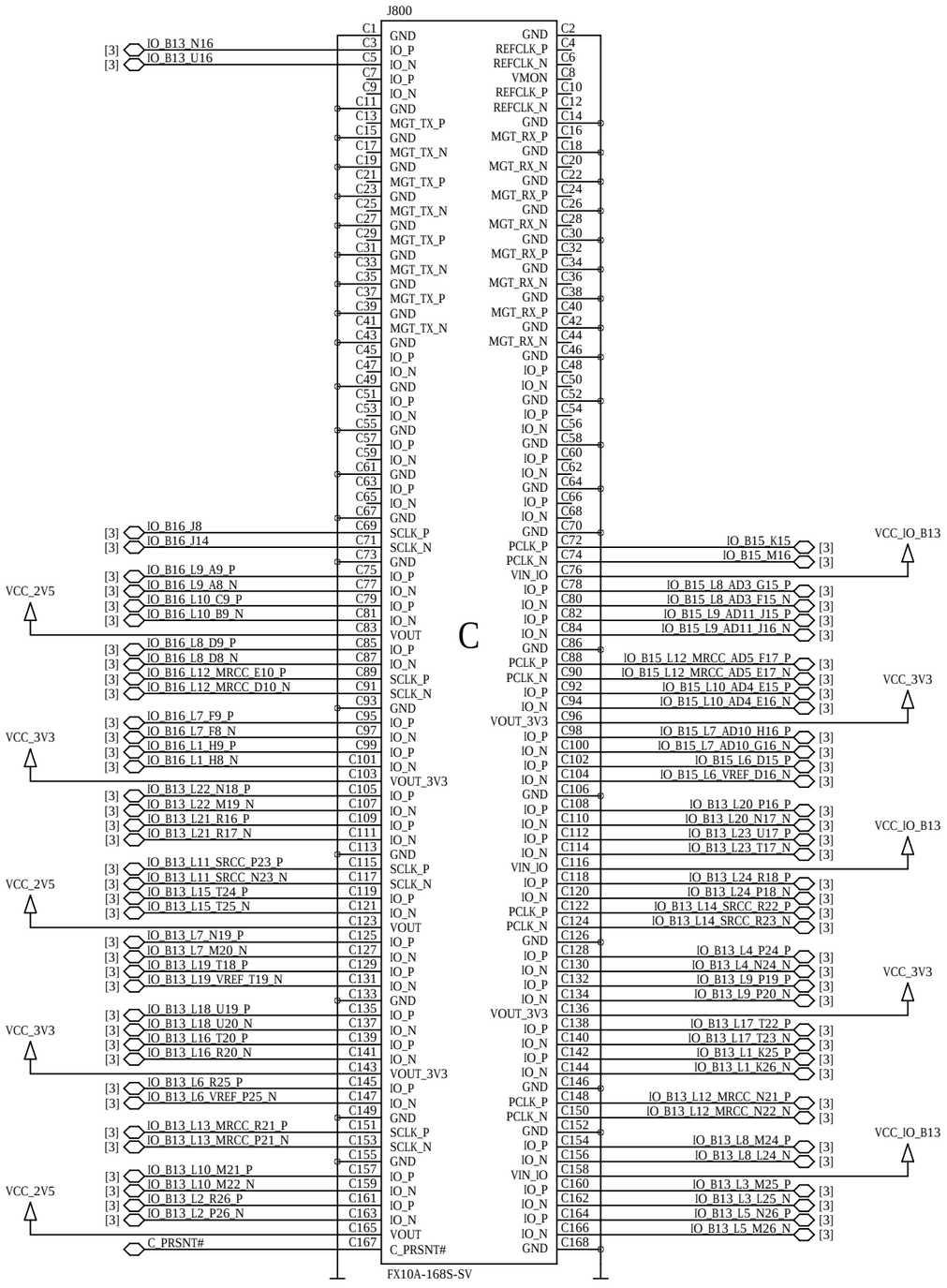
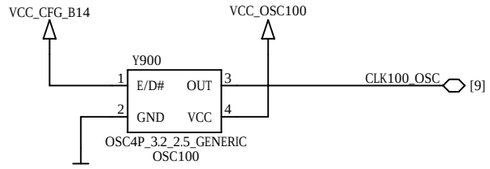
Module Connector C

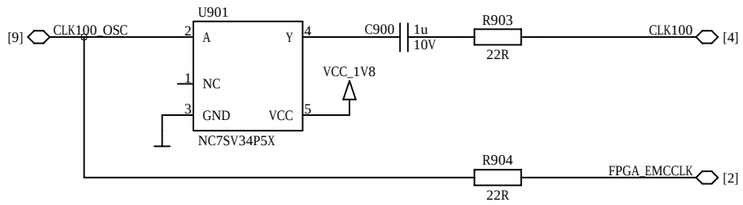


ENCLUSTRA	Copyright © 2017 by Enclustra GmbH	Sheet Name 8_MODULE_CONNECTOR_C	Customer No 0000	Revision R2.2	DNE = do not equip	Confidential	
	Company Enclustra GmbH	Project Mercury+ KX2	Project No 430	Designed MHEI	Date 2 Mar 2017	Sheet/sheets 8 / 21	

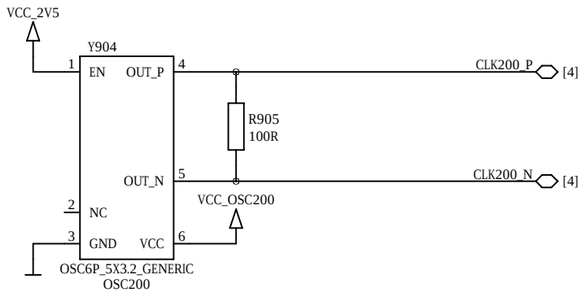
100 MHz Oscillator



Clock Driver



200 MHz Oscillator



Oscillator Power Filters

not included in user schematics

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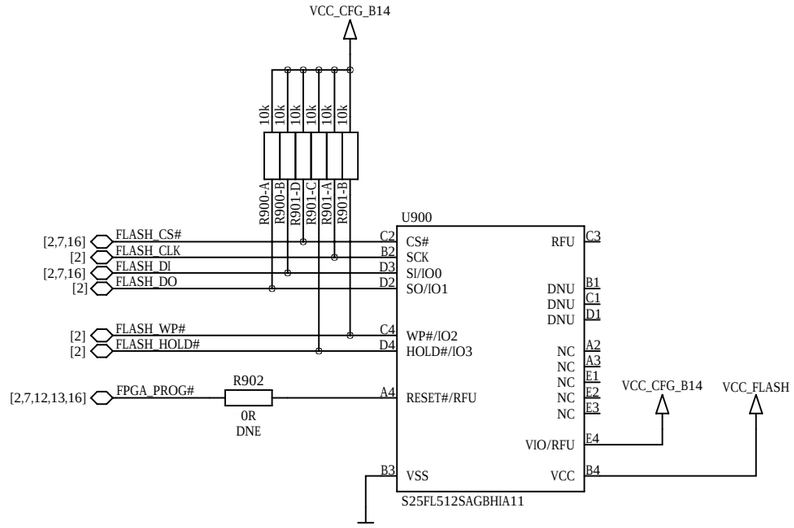
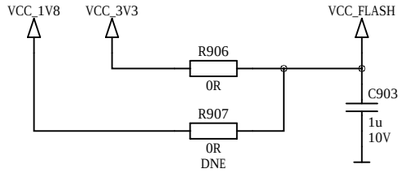
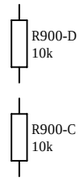
Quad SPI Flash



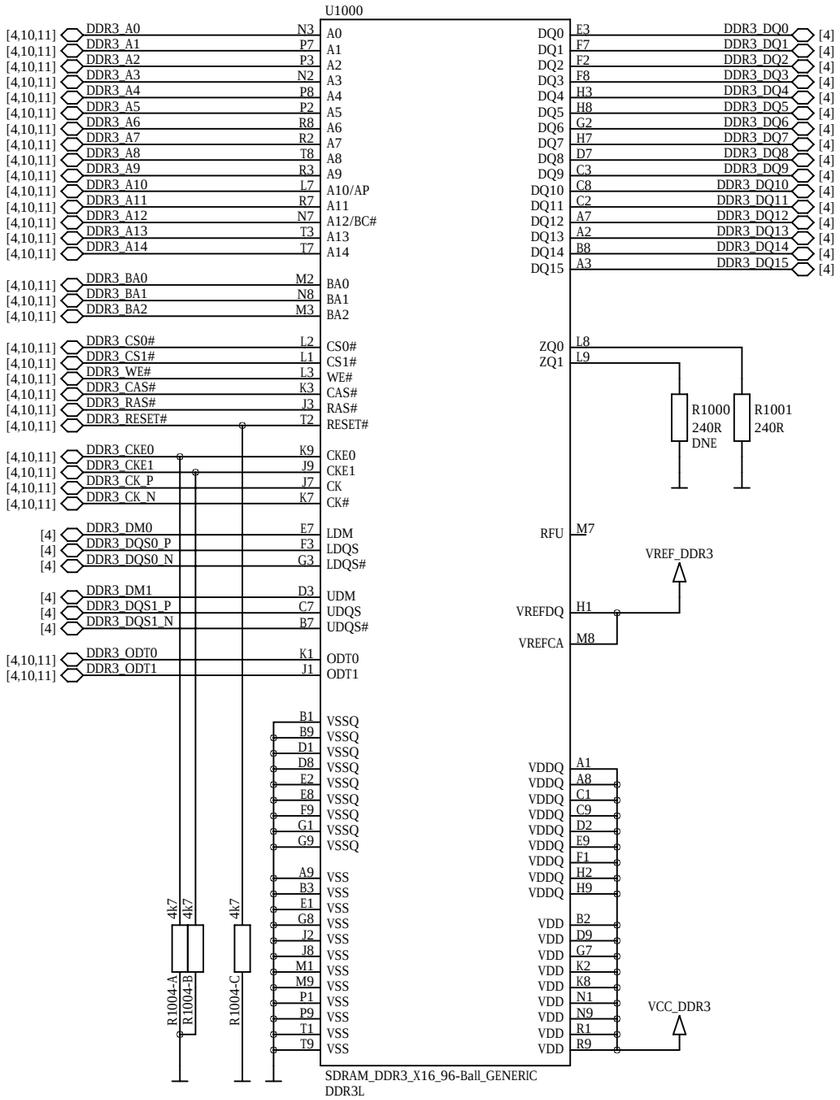
Flash Power



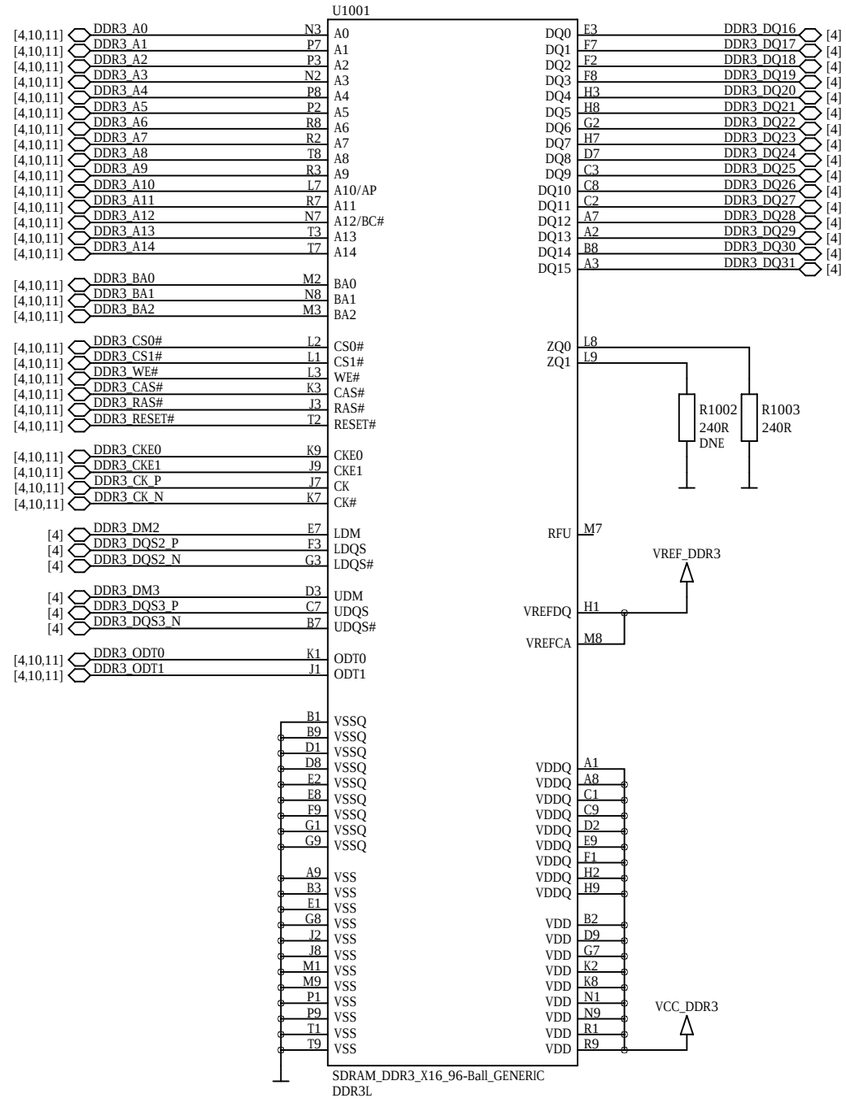


ENCLUSTRA	Copyright	© 2017 by Enclustra GmbH	Sheet Name	9_EEPROM/FLASH/OSCILLATOR	Customer No	0000	Revision	R2.2	DNE = do not equip	Confidential
	Company	Enclustra GmbH	Project	Mercury+ KX2	Project No	430	Designed	MHEI	Date 2 Mar 2017	Sheet/sheets 9 / 21

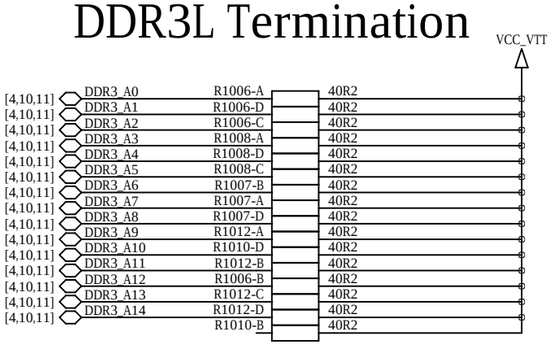
DDR3L SDRAM Bytes 0 - 1



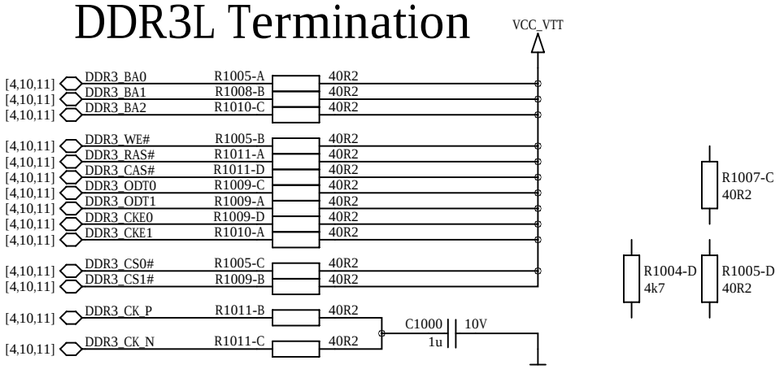
DDR3L SDRAM Bytes 2 - 3



DDR3L Termination

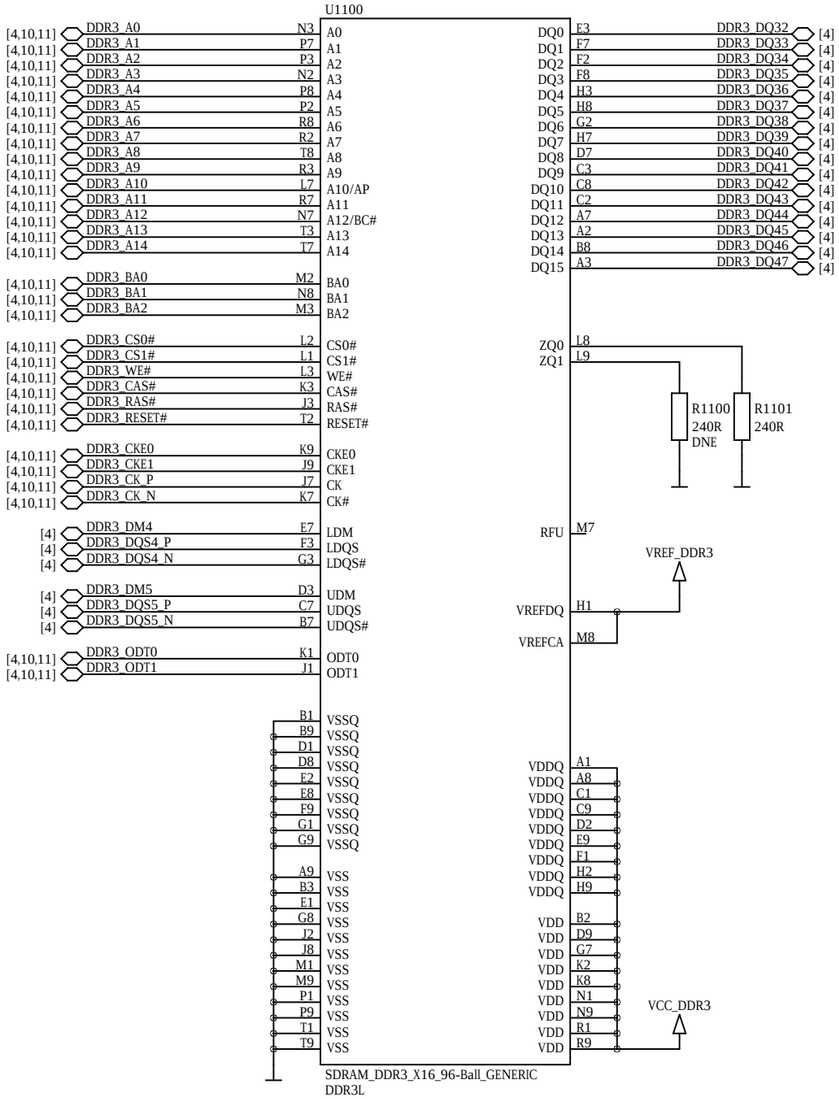


DDR3L Termination

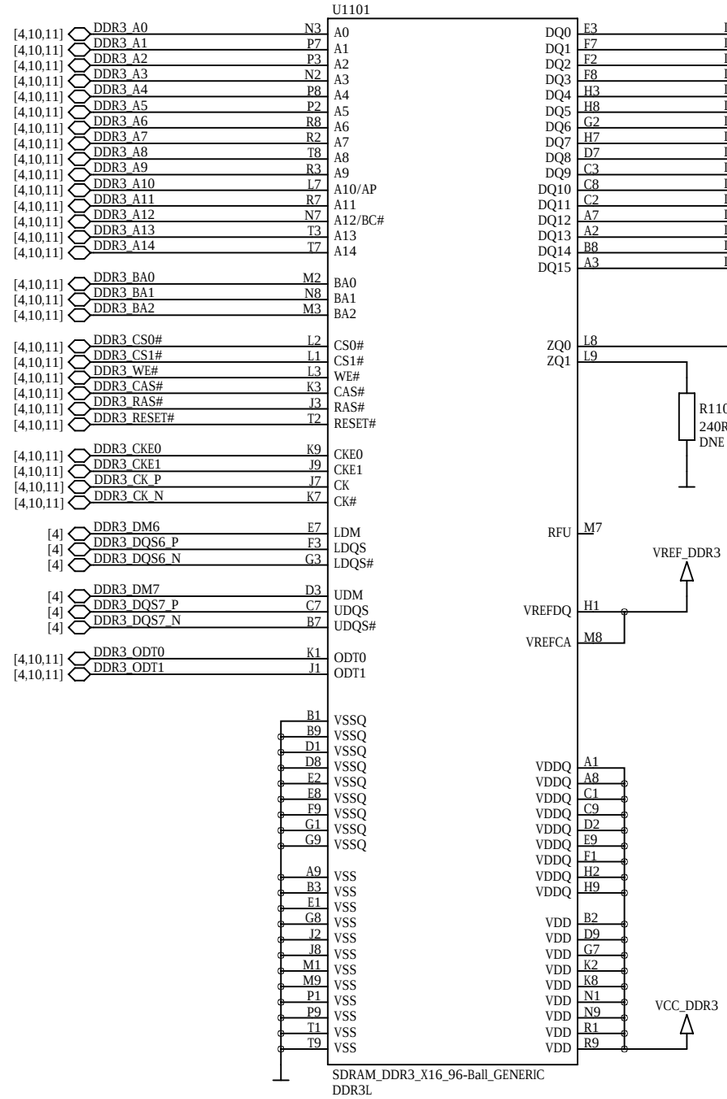


ENCLUSTRA	Copyright	© 2017 by Enclustra GmbH	Sheet Name	10_DDR3L_SDRAM_0_3	Customer No	0000	Revision	R2.2	DNE = do not equip	Confidential
	Company	Enclustra GmbH	Project	Mercury+ KX2	Project No	430	Designed	MHEl	Date 2 Mar 2017	Sheet/sheets 10 / 21

DDR3L SDRAM Bytes 4 - 5



DDR3L SDRAM Bytes 6 - 7



DDR3L Decoupling

not included in user schematics

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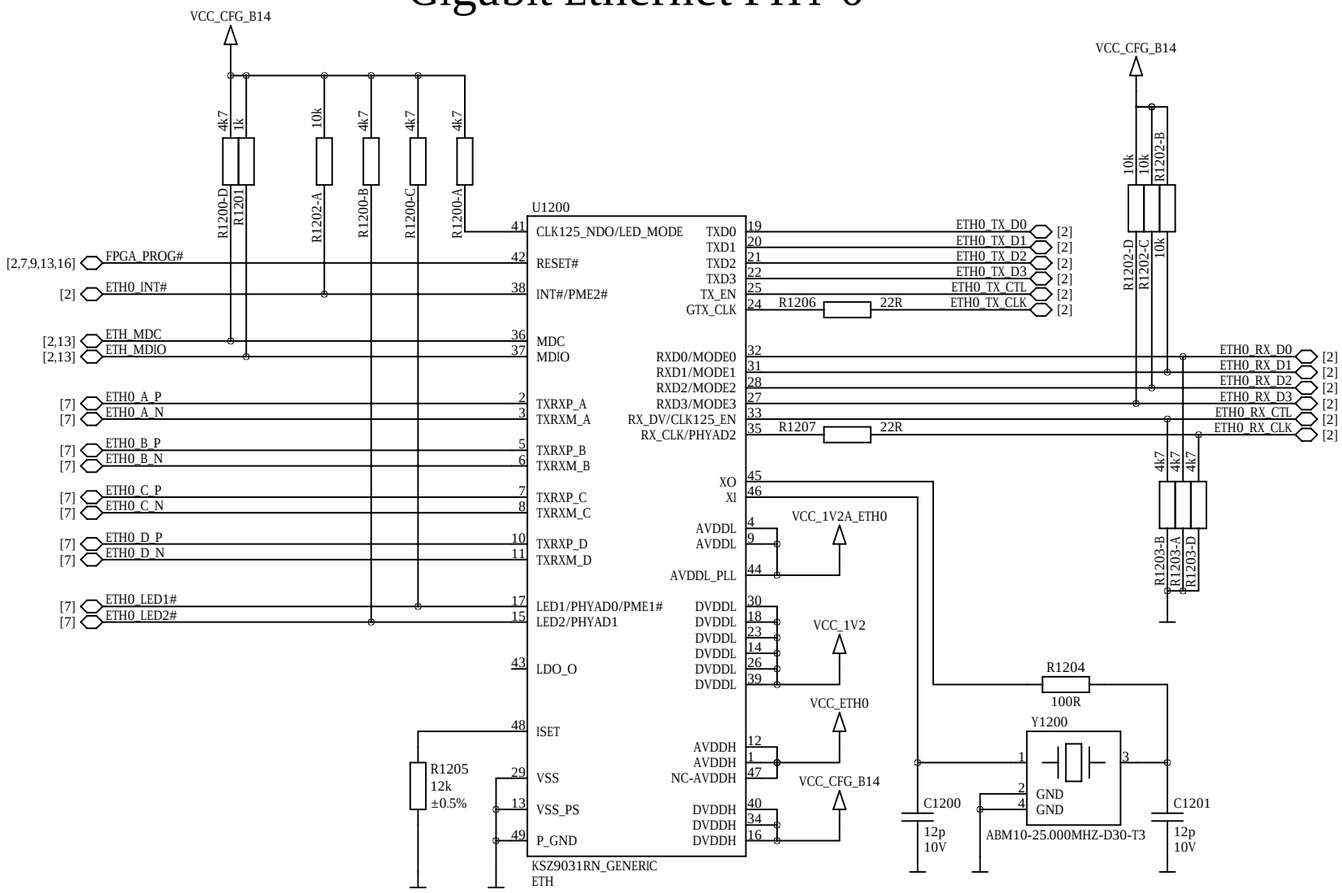
ENCLUSTRA	Copyright	© 2017 by Enclustra GmbH	Sheet Name	11_DDR3L_SDRAM_4_7	Customer No	0000	Revision	R2.2	DNE = do not equip	Confidential
	Company	Enclustra GmbH	Project	Mercury+ KX2	Project No	430	Designed	MHEI	Date 2 Mar 2017	Sheet/sheets 11 / 21

Gigabit Ethernet PHY 0



MODE<3:0> = 1110 -> RGMII, all capabilities
LED_Mode Pull up = Single LED
PhyAddress <2:0> = 011 -> 3
LED1 and LED2 are active low

Ethernet Power Filter

not included in user schematics

This part is intentionally left blank.

ENCLUSTRA	Copyright	© 2017 by Enclustra GmbH	Sheet Name	12_ETHERNET_PHY0	Customer No	0000	Revision	R2.2	DNE = do not equip	Confidential
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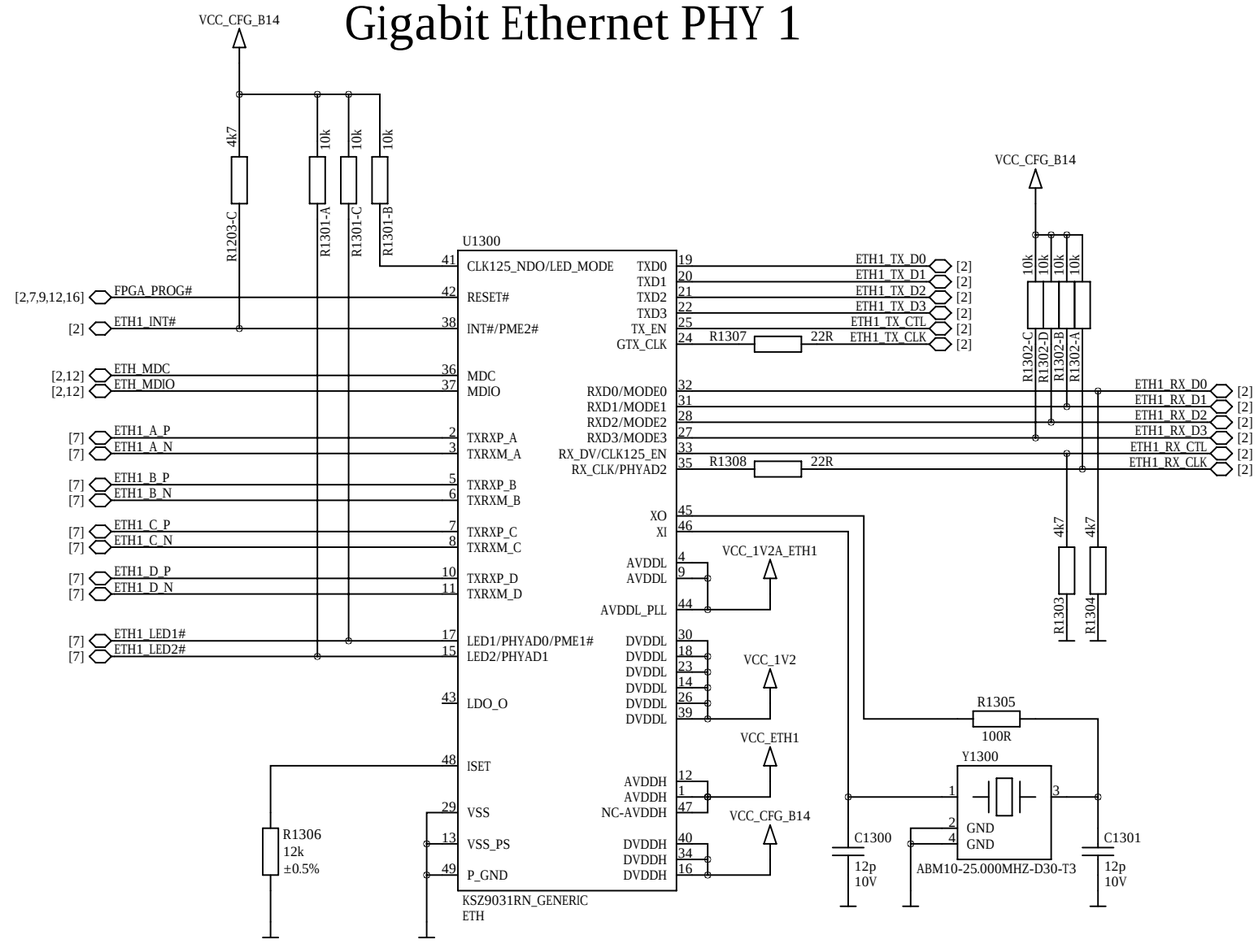
Gigabit Ethernet PHY 1



MODE<3:0> = 1110 -> RGMII, all capabilities
LED_Mode Pull up = Single LED
PhyAddress <2:0> = 111 -> 7
LED1 and LED2 are active low

Ethernet Power Filter

not included in user schematics

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R1301-D
10k

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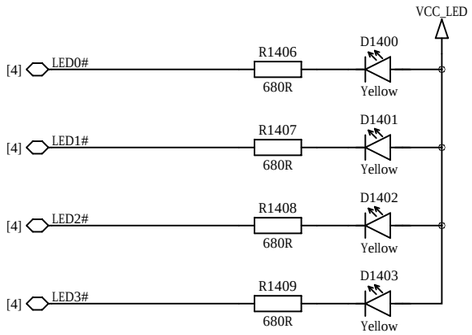
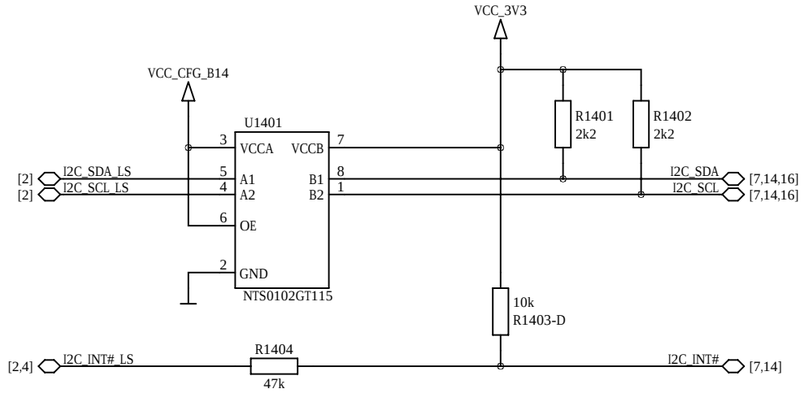
	Company	Enclustra GmbH	Project	Mercury+ KX2	Project No	430	Designed	MHEI	Date 2 Mar 2017	Sheet/sheets 13 / 21

User LEDs



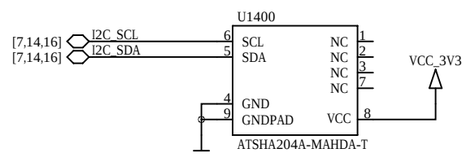
I2C Level Shifter



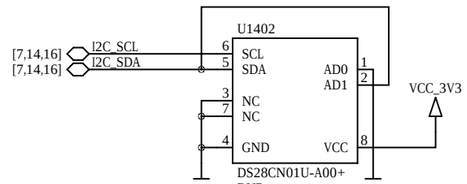
Secure EEPROMs

for Enclustra use only

only one EEPROM can be mounted



I2C Address: 1 1 0 0 1 0 0 Rw



I2C Address: 1 0 1 1 1 0 0 Rw

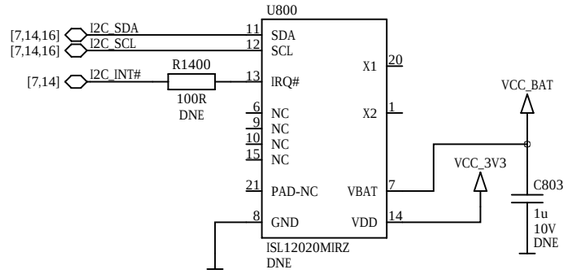
LED Power

not included in user schematics

This part is intentionally left blank.

Real-time Clock

optional



I2C Addresses:
Registers: 1 1 0 1 1 1 1 Rw
User SRAM: 1 0 1 0 1 1 1 Rw

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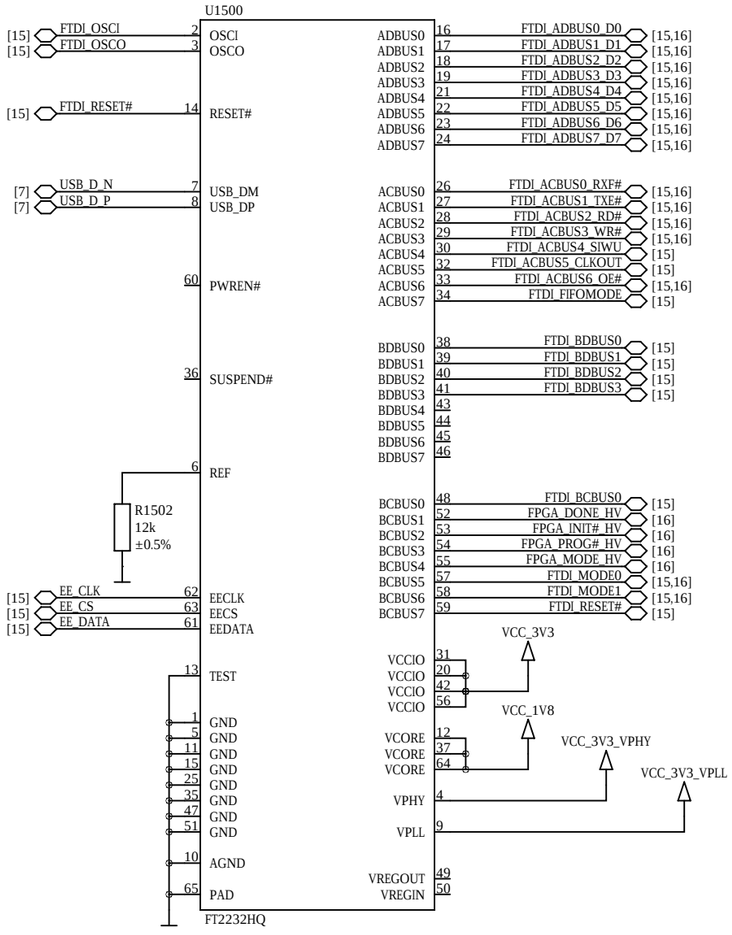
	Company	Enclustra GmbH	Project	Mercury+ KX2	Project No	430	Designed	MHEI	Date 2 Mar 2017	Sheet/sheets 14 / 21

FTDI USB 2.0 Device Controller

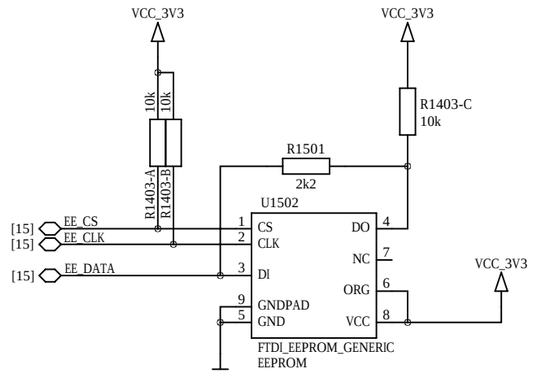


JTAG Adapter

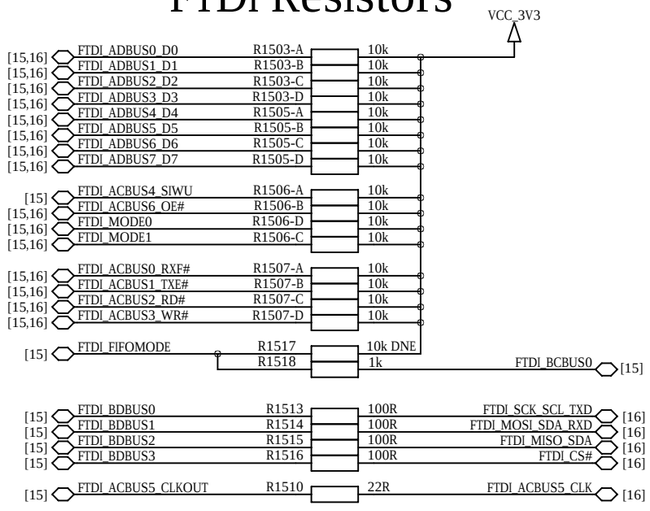
not included in user schematics

This part is intentionally left blank.

FTDI EEPROM



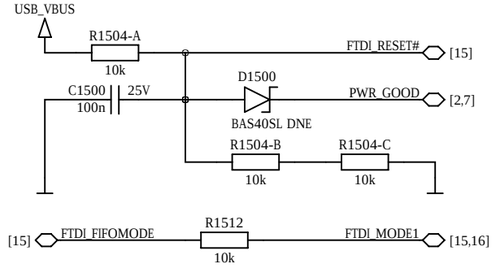
FTDI Resistors



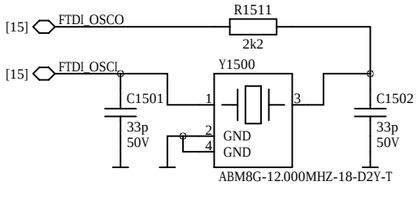
FTDI Power Filters

This part is intentionally left blank.

FTDI Reset



FTDI Clock



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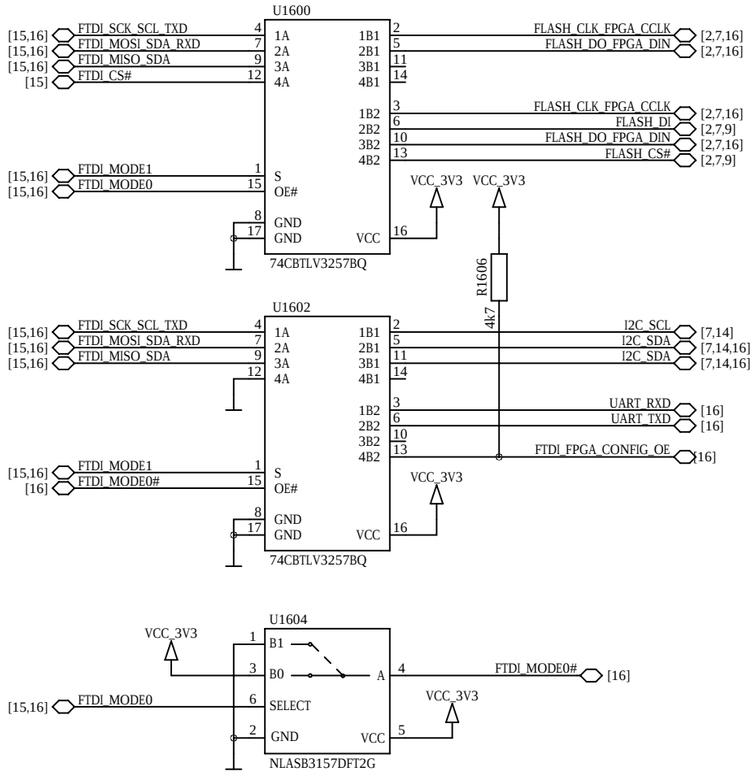
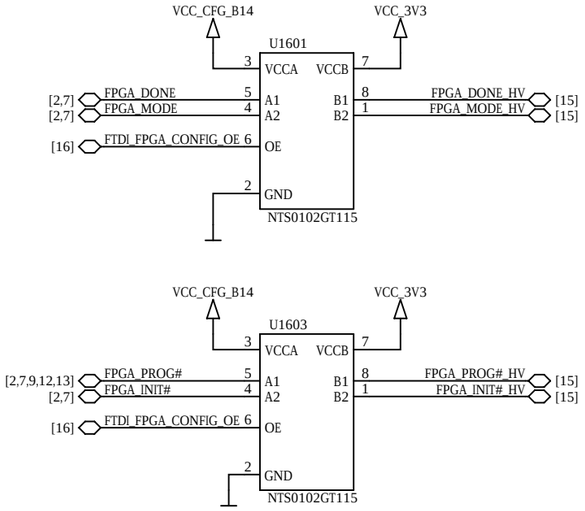
Configuration Multiplexers

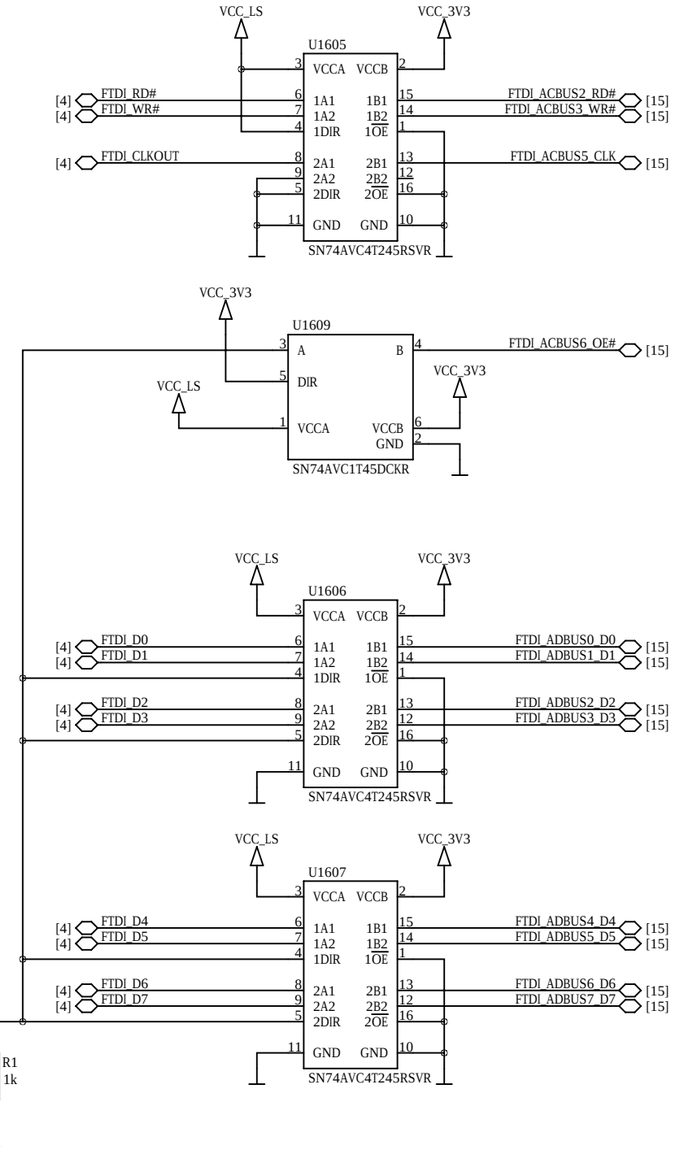


FTDI Status Level Shifters

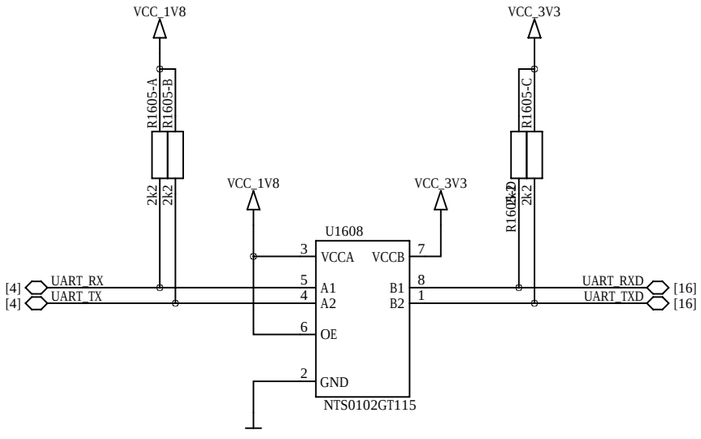


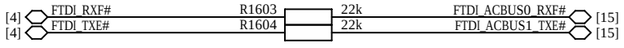
FTDI FIFO Level Shifters

optional



FTDI UART Level Shifters





Level Shifter Power

not included in user schematics

This part is intentionally left blank.

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DC/DC Converter 3.3V 9A 5%

not included in user schematics

This part is intentionally left blank.

Supported Voltage Ranges

Power Rail	Direction	Range	Tolerance
VCC_MOD	input	5.0V - 15V	±5%
VCC_IO_B12	input	1.0V - 3.3V	±5%
VCC_IO_B13	input	1.0V - 3.3V	±5%
VCC_IO_B15	input	1.0V - 3.3V	±5%
VCC_IO_B16	input	1.8V - 3.3V	±5%
VCC_CFG_B14	input	1.8, 2.5V - 3.3V	±5%
VCC_BAT	input	2.0V - 3.6V	-
VCC_1V8	output	1.8V	±5%
VCC_2V5	output	2.5V	±5%
VCC_3V3	output	3.3V	±5%

DC/DC Converter 1.0V 20A 3%

not included in user schematics

This part is intentionally left blank.

Input Power Filter

not included in user schematics

This part is intentionally left blank.

Dual DC/DC Converter

channel 1: 1.35V/1.5V 2A 5%

channel 2: 2.5V 2A 5%

not included in user schematics

This part is intentionally left blank.

LDO 2.0V 0.5A

only assembled for FPGA in FFG package

not included in user schematics

This part is intentionally left blank.

DDR3 Voltage Selection

	DDR3_VSEL	VCC_DDR3
Default	"Z"	1.5V
	"0"	1.35V
	"1"	Illegal

Dual DC/DC Converter

channel 1: 1.2V 2A 2.8%
channel 2: 1.8V 2A 3%
not included in user schematics

This part is intentionally left blank.

IO Voltage Generation

when C connector is not present on base board
not included in user schematics

This part is intentionally left blank.

DDR3 Termination Voltage Regulator

not included in user schematics

This part is intentionally left blank.

VREF DDR3

not included in user schematics

This part is intentionally left blank.

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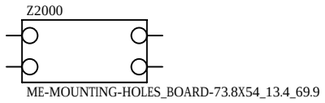
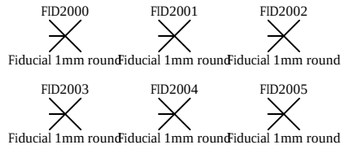
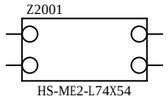
Module Mounting Holes



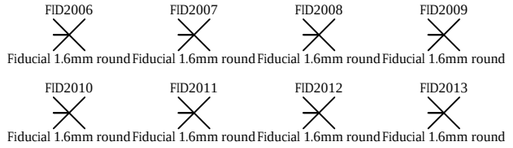
Fiducials



Heat Sink Mounting Holes M2

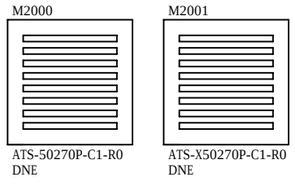


Panel Fiducials

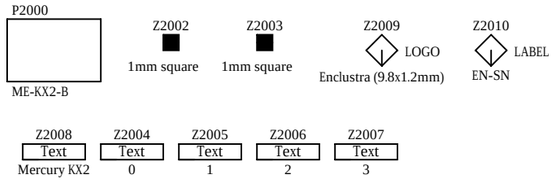


FPGA Heat Sink

optional



PCB / Logo / Pin-1 Marking / Text



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Component Variants

FPGA	DDR3L	Ethernet PHY	OSC100	OSC200	EEPROM	L0U68	L1U	LDO2V0
Part U200A XC7K160T-1FBG676C EN100565 Part U200B XC7K160T-2FFG676I EN101565 Part U200C XC7K325T-2FFG676I EN100566 Part U200D XC7K410T-2FFG676I EN100571	Part U1000A NT5CC128M16IP-DI EN100912 Part Part U1000B:1 H5TC4G63CFR-RDI EN101580 Part U1000B:2 NT5CC256M16DP-EKI EN101581 Part U1001A NT5CC128M16IP-DI EN100912 Part Part U1001B:1 H5TC4G63CFR-RDI EN101580 Part U1001B:2 NT5CC256M16DP-EKI EN101581 Part U1100A NT5CC128M16IP-DI EN100912 Part Part U1100B:1 H5TC4G63CFR-RDI EN101580 Part U1100B:2 NT5CC256M16DP-EKI EN101581 Part U1101A NT5CC128M16IP-DI EN100912 Part Part U1101B:1 H5TC4G63CFR-RDI EN101580 Part U1101B:2 NT5CC256M16DP-EKI EN101581	Part U1200A KSZ9031RNXCA EN100202 Part U1200B KSZ9031RNXIA EN100203 Part U1300A KSZ9031RNXCA EN100202 Part U1300B KSZ9031RNXIA EN100203	Part Y900A ASDMB-100.000MHZ-LY-T EN100284 Part Y900B ASEMB-100.000MHZ-LY-T EN101056	Part Y904A:1 DSC1123CI2-200.0000T EN101130 Part Y904A:2 ASDMPLV-200.000MHZ-LR-T EN100881 Part Y904B ASEMPLV-200.000MHZ-LR EN100880	Part U1502A CAT93C66VP2I-GT3 EN101255 Part U1502B 93AA66C-I/MS EN100279	Part L1700A 0u68 EN100848 Part L1700B 1u EN100436	Part L1801A 1u EN100784 Part L1801B 1u EN100917 Part L1803A 1u EN100784 Part L1803B 1u EN100917 Part L1901A 1u EN100784 Part L1901B 1u EN100917 Part L1903A 1u EN100784 Part L1903B 1u EN100917	U1802/R1811

Assembly Variants

Assembly Variant	FPGA	DDR3L	Ethernet PHY	OSC100	OSC200	EEPROM	L0U68	L1U	LDO2V0
Variant EN101775:0 ME-KX2-160-1C-D10-R2	Option EN101775:1 FPGA EN100565	Option EN101775:2 DDR3L EN100912	Option EN101775:3 ETH EN100203	Option EN101775:4 OSC100 EN100284	Option EN101775:5 OSC200 EN101130	Option EN101775:6 EEPROM EN101255	Option EN101775:7 L0U68 EN100848	Option EN101775:8 L1U EN100784	Option EN101775:9 LDO2V0 DNE
Variant EN101776:0 ME-KX2-160-2I-D11-P-R2	Option EN101776:1 FPGA EN101565	Option EN101776:2 DDR3L EN101580	Option EN101776:3 ETH EN100203	Option EN101776:4 OSC100 EN100284	Option EN101776:5 OSC200 EN101130	Option EN101776:6 EEPROM EN101255	Option EN101776:7 L0U68 EN100848	Option EN101776:8 L1U EN100784	Option EN101776:9 LDO2V0
Variant EN101777:0 ME-KX2-325-2I-D11-P-R2	Option EN101777:1 FPGA EN100566	Option EN101777:2 DDR3L EN101580	Option EN101777:3 ETH EN100203	Option EN101777:4 OSC100 EN100284	Option EN101777:5 OSC200 EN101130	Option EN101777:6 EEPROM EN101255	Option EN101777:7 L0U68 EN100848	Option EN101777:8 L1U EN100784	Option EN101777:9 LDO2V0
Variant EN101778:0 ME-KX2-410-2I-D11-P-R2	Option EN101778:1 FPGA EN100571	Option EN101778:2 DDR3L EN101580	Option EN101778:3 ETH EN100203	Option EN101778:4 OSC100 EN100284	Option EN101778:5 OSC200 EN101130	Option EN101778:6 EEPROM EN101255	Option EN101778:7 L0U68 EN100848	Option EN101778:8 L1U EN100784	Option EN101778:9 LDO2V0