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**Mini Project 2: VGA Report**

For this project, our team created a way for our Xilinx board to communicate through a VGA connection to display a picture on a computer monitor. Our device loads a hex file with pixel data into a ROM upon start up. It then files the data from the ROM into a FIFO which releases the data in time with the internal clock of the monitor. The FIFO gives the data to a timing generator which passes the pixel data to the monitor to display it. The FIFO and ROM units were generator using the CoreGen function in the Xilinx ISE Design Suite, but the timing generator and display plane were coded by hand.

The display plane module (display\_plane.v) reads in the pixel data from the loaded ROM and writes them to the FIFO. It reads in the memory at locations that correspond to the locations of the pixels on the screen. The FIFO is only written to if it is empty and then it is written to until it is full.

The timing generator (timing\_generator.v) takes the pixel data in from the FIFO and give the monitor the timing on which to display the pixel values. It uses a state machine for the vertical and horizontal synchronization and delivers the pixel values only when the monitor is in active time.