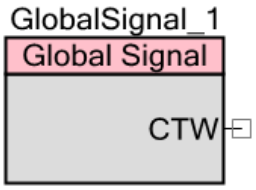
Global Signal Reference (GlobalSignal)
2.0

Features



- Allows access to device level global signals

General Description

This is the GlobalSignal reference component. It allows access to device specific, device level global signals.

When to use Global Signal

The GlobalSignal component can be used for accessing global signals of various types:

- Time period interrupts: CTW, FTW and one pulse per second.
- Error conditions: XMHz Error and Cache Interrupt.
- Status conditions: PLL Lock, LVI/HVI, and PM Interrupt.

Input/Output Connections

This section describes the output connection for the GlobalSignal component.

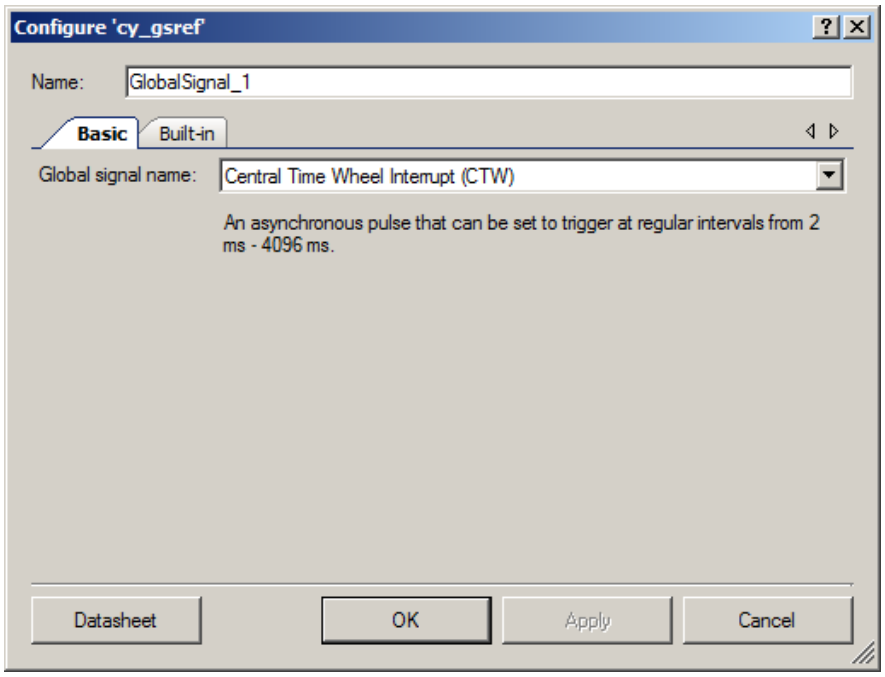
sig_out – Output

This terminal allows you to hook up a global signal to an interrupt or to another digital input.

Component Parameters

Drag the GlobalSignal component onto your design and double-click it to open the **Configure** dialog.

Figure 1 Configure GlobalSignal Dialog



The GlobalSignal component provides the following parameter:

Global Signal Name

For PSoC 3 and PSoC 5 LP, the drop down contains the following list of supported signals. The default value for the Global signal name is **Central Time Wheel Interrupt (CTW)**.

- **Central Time Wheel Interrupt (CTW) –** The central time wheel (CTW) is a 1-kHz, free-running, 13-bit counter clocked by the ILO. It is used to wake up the device from a low-power mode, is used in a Watchdog timer (WDT), and for General timing purposes. The interrupt generated from this counter is an asynchronous pulse that can be set to trigger at regular intervals from 2 ms - 4096 ms.
- **Fast Time Wheel Interrupt (FTW) –** The fast timewheel (FTW) is a 100-kHz, 5-bit counter clocked by the ILO, which can also be used to wake the system. When the terminal count is reached, the timewheel automatically resets and begins counting again. When it reaches terminal count, the FTW interrupt is generated. This interrupt then creates an asynchronous pulse that can be set to trigger at regular intervals from 10 µs - 2560 µs.

- **SPC Idle (SPCIdle) –** The System Performance Controller (SPC) is used in nonvolatile memory programming of Flash memory. The SPC can perform both read and write operations on the flash memory. The SPC Idle signal indicates that SPC left the active mode, which allows writing to certain registers that are dependent on this signal.
- **One Pulse per Second Interrupt (OPPS) –** This is an interrupt that triggers every second. The OPPS requires that the external 32 kHz crystal be enabled. It also requires that the OPPS be properly configured, either by using the RTC component, or by manually configuring bits 4 and 5 in the PM_TW_CFG2 register. In PSoC 5LP, the RTC component must be used.
- **Cache Interrupt (CacheInt) –** Error Correcting Code (ECC) can be used to ensure reliability in flash reads. When the cache reads from Flash, it gets the error status from the ECC block and generates an interrupt if either a single or multi-bit error is detected in the ECC.
- **PLL Lock (PLLLock) –** This signal indicates the status of the PLL frequency lock.
- **XMHz Error (XMHzErr) –** Indicates that an error was detected with the external crystal.
- **Power Management Status Register Interrupt (PwrMS) –** Triggers if the Central Time Wheel, Fast Time Wheel or One Pulse per Second is enabled and the timer expires. Stays high until the status register is read.
- **Low/High Voltage (LVI/HVI) –** Used to detect that the voltage is outside of a settable range. For more information on using the Low/High Voltage signals, see the Voltage Detect APIs section in the System Reference Guide.

For PSoC 4, the drop down contains the following list of supported signals. The default value for the Global signal name is **Watch Dog Timer Interrupt (WDTInt)**.

- **Watch Dog Timer Interrupt (WDTInt) –** The watchdog timer (WDT) circuit automatically resets the microcontroller in the event of an unexpected firmware execution path. This timer is clocked by the 32-kHz ILO. The WDT interrupt triggers when any enabled Watch Dog timer expires.
- **Combined CTBm interrupt (CTBmInt) –** The CTBm block provides continuous time functionality at the entry and exit points of the analog subsystem. The Combined CTBm interrupt triggers when any enabled CTBm block generates an interrupt.
- **System Performance Controller Interface interrupt (SPCIFInt) –** The System Performance Controller (SPC) is the block that generates the properly sequenced high-voltage pulses required for erase and program operations of the flash memory. When a non-blocking function is called from SRAM, the SPCIF timer triggers its interrupt when each of the sub-operations in a write or program operation is complete.

- **Combined low power comparator interrupt –** Triggers when any enabled low power comparator generates an interrupt.
- **Power System interrupt –** Triggers on low voltage detect. For more information on using the Power System interrupt, see the Voltage Detect APIs section in the System Reference Guide.

Silicon Supported Signals

Signal name		Silicon	
		PSoC 3	PSoC 5LP
CTW		Applicable	Applicable
FTW		Applicable	Applicable
SPCIdle		Applicable	Applicable
OPPS		Applicable	Applicable
CacheInt	ECC interrupt	Not Applicable	Applicable
	Cache interrupt	Not Applicable	Applicable
PLLLock		Applicable	Applicable
XMHzErr		Applicable	Applicable
PwrMS		Applicable	Applicable
LVI/HVI		Applicable	Applicable

Signal name	Silicon	
	PSoC 4200/PSoC 4100	PSoC 4000
WDTInt	Applicable	Applicable
CTBmInt	Applicable	Not Applicable
SPCIFInt	Applicable	Applicable
LPCompInt	Applicable	Not Applicable
PWRInt	Applicable	Not Applicable

MISRA Compliance

This section describes the MISRA-C:2004 compliance and deviations for the component. There are two types of deviations defined:

- project deviations – deviations that are applicable for all PSoC Creator components
- specific deviations – deviations that are applicable only for this component

This section provides information on component-specific deviations. Project deviations are described in the MISRA Compliance section of the *System Reference Guide* along with information on the MISRA compliance verification environment.

The Global Signal Reference component does not have any C source code APIs.

Functional Description

This is a hardware component. It produces a single output signal that can be used by other components in the design. The timing of this signal is not guaranteed, so it must be used by components that are not sensitive to timing constraints such as the interrupt component.

Component Changes

Version	Description of Changes	Reason for Changes / Impact
2.0.d	Updated the Global Signal Name inputs information	Inadequate description
	Added PSoC 4000 (CY8C40xx) support	
2.0.c	Enhanced description of One Pulse Per Second Interrupt.	Provide guidance on using OPPS interrupt.
2.0.b	Added PSoC 4 support.	PSoC 4 contains five new selectable global signals.
2.0.a	Added MISRA Compliance section.	The component does not have APIs.
2.0	Initial release.	