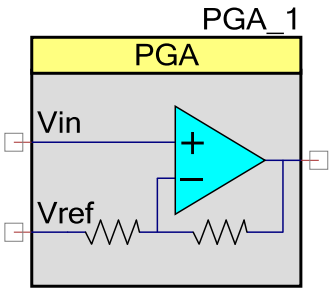
# Programmable Gain Amplifier (PGA)

1.50

## Features

- Gain steps from 1 to 50
- High input impedance
- Selectable input reference
- Adjustable power settings




## General Description

The PGA implements an opamp-based, non-inverting amplifier with user-programmable gain. This amplifier has high input impedance, wide bandwidth, and selectable input voltage reference. It is derived from the SC/CT block.

The gain can be between 1 (0 dB) and 50 (+34 dB). The gain may be selected via configuration or changed at run-time using the provided API. The maximum bandwidth is limited by the gain-bandwidth product of the opamp and is reduced as the gain is increased. The input of the PGA operates from rail to rail, but the maximum input swing (difference between Vin and Vref) is limited to Vdda/Gain. The output of the PGA is class A, and is rail to rail for sufficiently high load resistance.

The PGA is used when an input signal has insufficient amplitude. A PGA may be placed in front of a comparator, ADC, or mixer to increase the amplitude of the signal to these components. The PGA can be used as a unity gain amplifier to buffer the inputs of lower impedance blocks, including Mixers or inverting PGAs. A unity gain PGA can also be used to buffer the output of a VDAC or reference.

## Input/Output Connections

This section describes the various input and output connections for the PGA. An asterisk (*) in the list of I/Os indicates that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.

### Vin – Analog

Vin is the input signal terminal.

### Vref – Analog *

Vref is the input terminal for a reference signal.

The reference input can be connected to an external (to the component) reference or internal (to the component) Vss (ground). When the reference is connected externally the routing resistance is added to the internal resistors slightly decreasing the gain and increasing the gain tolerance.

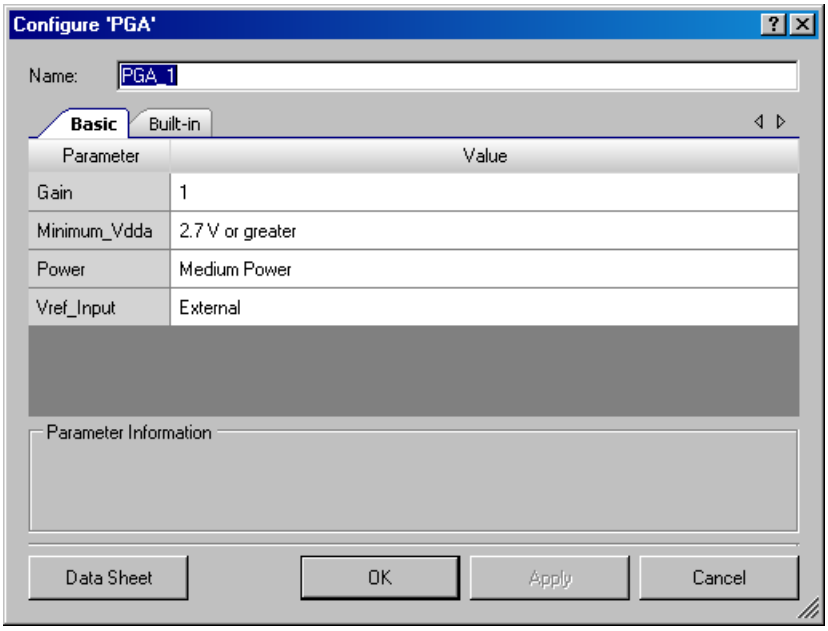
### Vout – Analog

Vout is the output voltage signal terminal. Vout is a function of (Vin - Vref) times the specified Gain:

*Vout = Vref + (Vin - Vref) * Gain*

## Parameters and Setup

Drag a PGA component onto your design and double-click it to open the Configure dialog.




### Gain

This sets the initial gain of the PGA. The gain may be selected from the following set of allowed values: 1 (default), 2, 4, 8, 16, 24, 32, 48, and 50.

### Minimum_Vdda

This parameter is determined by the minimum analog supply voltage expected for the PSoC in the design. The parameter can be set to one of two values:

- 2.7 V or greater (default)
- Less than 2.7 V

For an analog supply voltage below 2.7 V, the amplifier makes use of an internal boost circuit. The component implementation uses an additional 10 MHz clock to drive the boost circuit for the amplifier block.

### Power

This sets the initial drive power of the PGA. The power determines the speed with which the PGA reacts to changes in the input signal. There are four power settings; Minimum, Low, Medium (default), and High. Minimum Power setting results in the slowest response time and a High Power setting results in the fastest response time.

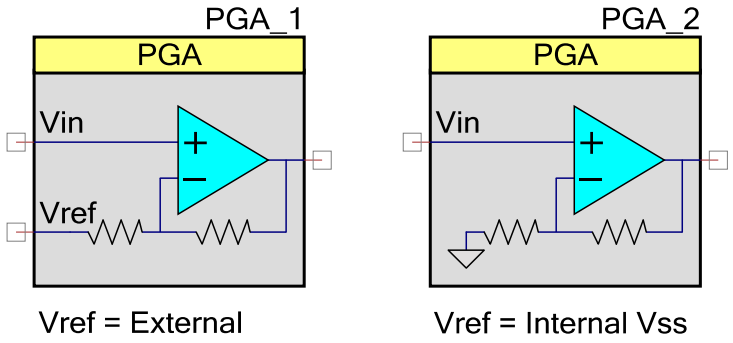
### Vref_Input

This parameter is used to select the input voltage reference. The options include:

- "Internal Vss" – Uses a ground signal internal to the component
- "External" (default) – Signal on the Vref terminal provides the amplifier reference.

The symbol displayed in PSoC Creator changes depending on the reference input selected.

**Figure 1 PGA Configurations**




Vref = External Vref = Internal Vss

# Placement

There are no placement specific options.

# Resources

The PGA uses one SC/CT block. Details on this block can be found in the applicable device data sheet and Technical Reference Manual (TRM). These documents are available on the Cypress web site.

# Application Programming Interface

Application Programming Interface (API) routines allow you to configure the component using software. The following table lists and describes the interface to each function. The subsequent sections cover each function in more detail.

By default, PSoC Creator assigns the instance name "PGA_1" to the first instance of a component in a given design. You can rename it to any unique value that follows the syntactic rules for identifiers. The instance name becomes the prefix of every global function name, variable, and constant symbol. For readability, the instance name used in the following table is "PGA".

| Function | Description |
|---|---|
| void PGA_Init(void) | Initializes or restores default PGA configuration. |
| void PGA_Enable(void) | Enables the PGA. |
| void PGA_Start(void) | Start the PGA. |
| void PGA_Stop(void) | Power down the PGA. |
| void PGA_SetGain(uint8 gain) | Set gain to pre-defined constants. |
| void PGA_SetPower(uint8 power) | Set drive power to one of four settings. |
| void PGA_Sleep(void) | Stops and saves the user configurations. |
| void PGA_Wakeup(void) | Restores and enables the user configurations. |
| void PGA_SaveConfig(void) | Empty function. Provided for future usage. |
| void PGA_RestoreConfig(void) | Empty function. Provided for future usage. |

## Global Variables

| Variable | Description |
|---|---|
| PGA_initVar | Indicates whether the PGA has been initialized. The variable is initialized to 0 and set to 1 the first time PGA_Start() is called. This allows the component to restart without reinitialization after the first call to the PGA_Start() routine.<br>If reinitialization of the component is required, then the PGA_Init() function can be called before the PGA_Start() or PGA_Enable() function. |

## void PGA_Init(void)

**Description:** Initializes or restores default PGA configuration.

**Parameters:** None

**Return Value:** None

**Side Effects:** All registers will be reset to their initial values. This will re-initialize the component.

## void PGA_Enable(void)

**Description:** Enables the PGA.

**Parameters:** None

**Return Value:** None

**Side Effects:** None

## void PGA_Start( void )

**Description:** Turns on the amplifier with the power and gain based on the settings provided during the configuration or the current values after a PGA_Stop() has been called.

**Parameters:** None

**Return Value:** None

**Side Effects:** None

## void PGA_Stop( void )

**Description:** Turn off PGA and enable its lowest power state.

**Note** This API is not recommended for use on PSoC 3 ES2 and PSoC 5 ES1 silicon. These devices have a defect that causes connections to several analog resources to be unreliable when not powered. The unreliability manifests itself in silent failures (e.g. unpredictably bad results from analog components) when the component utilizing that resource is stopped. It is recommended that all analog components in a design should be powered up (by calling the <INSTANCE_NAME>_Start() APIs) at all times. Do not call the <INSTANCE_NAME>_Stop() APIs.

**Parameters:** None

**Return Value:** None

**Side Effects:** None. Does not affect power or gain settings

## void PGA_SetPower( uint8 power )

**Description:** Sets the drive power to one of four settings; minimum, low, medium, or high.

**Parameters:** (uint8) power: See the following table for valid power settings.

| Power Setting | Notes |
|---|---|
| PGA_MINPOWER | Minimum active power and slowest reaction time. |
| PGA_LOWPOWER | Low power and speed. |
| PGA_MEDPOWER | Medium power and speed. |
| PGA_HIGHPOWER | Highest active power and fastest reaction time. |

**Return Value:** None

**Side Effects:** None

## void PGA_SetGain( uint8 gain )

**Description:** Set the amplifier gain to a value between 1 and 50.

**Parameters:** uint8 gain: See table below for valid gain settings.

| Gain Setting | Notes |
|---|---|
| PGA_GAIN_01 | Gain = 1 |
| PGA_GAIN_02 | Gain = 2 |
| PGA_GAIN_04 | Gain = 4 |
| PGA_GAIN_08 | Gain = 8 |
| PGA_GAIN_16 | Gain = 16 |
| PGA_GAIN_24 | Gain = 24 |
| PGA_GAIN_32 | Gain = 32 |
| PGA_GAIN_48 | Gain = 48 |
| PGA_GAIN_50 | Gain = 50 |

**Return Value:** None

**Side Effects:** None

## void PGA_Sleep( void )

**Description:** Stops the operation. Saves the configuration registers and the component enable state. Should be called just prior to entering sleep

**Parameters:** None

**Return Value:** None

**Side Effects:** None

### void PGA_Wakeup( void )

**Description:** Restores the component enable state and configuration registers. Should be called just after awaking from sleep.

**Parameters:** None

**Return Value:** None

**Side Effects:** None

### void PGA_SaveConfig(void)

**Description:** Empty function. Provided for future usage.

**Parameters:** None

**Return Value:** None

**Side Effects:** None

### void PGA_RestoreConfig(void)

**Description:** Empty function. Provided for future usage.

**Parameters:** None

**Return Value:** None

**Side Effects:** None

## Sample Firmware Source Code

The following is a C language example demonstrating the basic functionality of the PGA component. This example assumes the component has been placed in a design with the default name "PGA_1."

**Note** If you rename your component you must also edit the example code as appropriate to match the component name you specify.

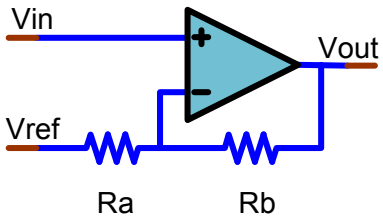
```
#include <device.h>

void main()
{
    PGA_1_Start();
    PGA_1_SetGain(PGA_1_GAIN_24);
    PGA_1_SetPower(PGA_1_MEDPOWER);
    PGA_1_Sleep();
    PGA_1_Wakeup();
}
```

# Functional Description

The PGA is constructed from a generic SC/CT block. Details on this block can be found in the applicable device data sheet and TRM, available on the Cypress web site. The gain is selected by adjusting two resistors, Ra and Rb. (see functional schematic, Figure 3). Ra may be set to either 20K or 40K ohms. Rb is set between 20K and 1000K ohms to generate the gain values selectable in either the parameter dialog or the SetGain function.

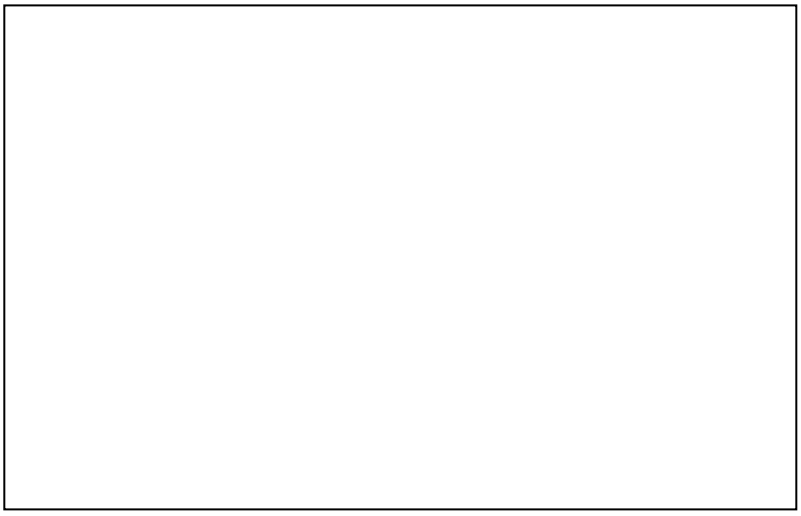
The block has a programmable capacitor in parallel with the feedback resistor, Rb. The value of the capacitor is configured for each gain selection to achieve guaranteed stability. Reassigning Rb values without also selecting the appropriate feedback capacitor value may result in PGA instability. The user is strongly advised to use the provided APIs for gain changes.

**Figure 2 PGA Schematic**




The bandwidth of the PGA is determined by gain and power setting. Because of compensation capacitor and stability requirements, the bandwidth is somewhat reduced from the absolute maximum expected from the opamp's open loop gain-bandwidth.

TBD - Add power vs bandwidth graph



## Registers

The PGA component configuration is implemented in registers SC[0..3]_CR0, SC[0..3]_CR1 and SC[0..3]_CR2. These can be accessed in user code by reference to the instantiated component name, e.g., PGA_1_CR0_REG. The register contents can be reviewed in the PSoC Creator component debug window. Refer to the applicable TRM, available on the Cypress web site, for a detailed description of each register. The following registers are displayed in the PGA component debug window.

**Register:** PGA_1_CR0_REG

**Name:** Switched Capacitor Control Register 0

**Description:** Register bits 3:1 configure the switch capacitor block operating mode. This field is set to 110b for the PGA component.

**Register:** PGA_1_CR1_REG

**Name:** Switched Capacitor Control Register 1

**Description:** Register fields configure drive mode, compensation capacitor values, and gain setting of the switch capacitor block.

**Register:** PGA_1_CR2_REG

**Name:** Switched Capacitor Control Register 2

**Description:** Register fields configure the input impedance, feedback impedance and the reference ground selection for the switch capacitor block.

**Register:** PGA_1_PM_ACT_CFG_REG

**Name:** Active Power Mode Configuration Register 9

**Description:** Register bits 3:0 enable power to each of the four switch capacitor blocks.

# DC and AC Electrical Characteristics

The following values are based on characterization data. Specifications are valid for -40°C ≤ $T_A$ ≤ 85°C and $T_J$ ≤ 100°C except where noted. Unless otherwise specified in the tables below, all Typical values are for $T_A$ = 25°C, Vdda = 5.0V, Power = High, output referenced to analog ground, Vssa .

## 5.0V/3.3V DC Electrical Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input | | | | | | |
| Vos | Input Offset Voltage | Vdda=3.3 V, 25 C, P=Min | na | tbc | tbc | mV |

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | | Vdda=3.3 V, 25 C, P=Low | na | tbc | tbc | mV |
| | | Vdda=3.3 V, 25 C, P=Med | na | tbc | tbc | mV |
| | | Vdda=3.3 V, 25 C, P=High | na | tbc | tbc | mV |
| TCVos | Temp. coeff. input offset voltage, absolute value | P=Min | na | tbc | tbc | uV/°C |
| | | P=Low | na | tbc | tbc | uV/°C |
| | | P=Med | na | tbc | tbc | uV/°C |
| | | P=High | na | tbc | tbc | uV/°C |
| Rin | Input resistance | Positive gain, non-inverting input | | tbc | tbc | Megohms |
| Cin | Input capacitance | Positive gain, non-inverting input, not including routing capacitance | na | tbc | tbc | pF |
| Ge1 | Gain accuracy, deviation from nominal | G=1, Vdda=5.0 V, P=High, Vref internally connected to Vss | tbc | tbc | tbc | % |
| Ge16 | | G=16, Vdda=5.0 V, P=High, Vref internally connected to Vss | tbc | tbc | tbc | % |
| Ge50 | | G=50, Vdda=5.0 V, P=High, Vref internally connected to Vss | tbc | tbc | tbc | % |
| Gd1 | Gain change vs temp | G=1, Vdda=5.0 V, P=High, Vref internally connected to Vss | na | tbc | tbc | ppm/°C |
| Gd16 | | G=16, Vdda=5.0 V, P=High, Vref internally connected to Vss | na | tbc | tbc | ppm/°C |
| Gd50 | | G=50, Vdda=5.0 V, P=High, Vref internally connected to Vss | na | tbc | tbc | ppm/°C |
| Ge_ref_ext | Gain error, routing dependent, ref | Gain = 16, Vref connected to internally routed buffer (add PGA) | tbc | tbc | tbc | % |
| Ge_ref_pin | Gain error, routing dependent, pin | Gain = 16, Vref connected to pin | tbc | tbc | tbc | % |
| Vout_range | Output swing | Gain = 1, Rload = 100k to Vdda/2 | tbc | tbc | tbc | |
| PSRR | Power supply rejection ratio | Gain=1, measured as shift in offset voltage at DC | tbc | tbc | | dB |
| Idda | Operating current | Vdda=1.71 V, P=Low | na | tbc | tbc | uA |
| | | Vdda=5.0 V, P=High | na | tbc | tbc | uA |

## 5.0V/3.3V AC Electrical Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| GBW_L | Gain Bandwidth Product, P=Low | Gain=1, Vdda=2.7 V, 25 C | tbc | tbc | na | MHz |
| GBW_H | Gain Bandwidth Product, P=High | Gain=1, Vdda=5.0 V, 25 C | tbc | tbc | na | MHz |
| SR_PMin | Slew Rate | 20 - 80%, Gain=1, P=Min | tbc | tbc | na | V/us |
| SR_PLow | | 20 - 80%, Gain=1, P=Low | tbc | tbc | na | V/us |
| SR_PMed | | 20 - 80%, Gain=1, P=Med | tbc | tbc | na | V/us |
| SR_PHigh | | 20 - 80%, Gain=1, P=High | tbc | tbc | na | V/us |
| Tsettle_Pmin | Settling time to | 1.0 V step to 0.1%, CLoad= 15 pF Vdda= 5.0 V, G=1, P=min | na | tbc | tbc | nsec |
| Tsettle_Plow | | 1.0V step to 0.1%, CLoad= 15 pF Vdda= 5.0 V, G=1, P=low | na | tbc | tbc | nsec |
| Tsettle_Pmed | | 1.0V step to 0.1%, CLoad= 15 pF Vdda= 5.0 V, G=1, P=med | na | tbc | tbc | nsec |
| Tsettle_Phigh | | 1.0V step to 0.1%, CLoad= 15 pF Vdda= 5.0 V, G=1, P=high | na | tbc | tbc | nsec |
| Vn_Pmin | Noise | f=10 kHz, P=min | na | tbc | na | nV/rtHz |
| Vn_Plow | | f=10 kHz, P=Low | na | tbc | na | nV/rtHz |
| Vn_Pmed | | f=10 kHz, P=Med | na | tbc | na | nV/rtHz |
| Vn_Phigh | | f=10 kHz, P=High | na | tbc | na | nV/rtHz |
| | | | | | | |

## Figures

**Typical Gain vs freq, 3.3V, P=min**
X axis 10 kHz to 10 MHz
Y axis Gain, dB
1 G=1
2 G=2
3 G=4
4 G=8
5 G=16
6 G=24
7 G=32
8 G=48
9 G=50

**Typical Gain vs freq, 3.3V, P=low**
X axis 10 kHz to 10 MHz
Y axis Gain, dB
1 G=1
2 G=2
3 G=4
4 G=8
5 G=16
6 G=24
7 G=32
8 G=48
9 G=50

**Typical Gain vs freq, 3.3V, P=med**
X axis 10 kHz to 10 MHz
Y axis Gain, dB
1 G=1
2 G=2
3 G=4
4 G=8
5 G=16
6 G=24
7 G=32
8 G=48
9 G=50

**Typical Gain vs freq, 3.3V, P=high**
X axis 10 kHz to 10 MHz
Y axis Gain, dB
1 G=1
2 G=2
3 G=4
4 G=8
5 G=16
6 G=24
7 G=32
8 G=48
9 G=50

**Gain deviation vs freq, Vdda=2.7V, P=low G=50, Difference from nominal**
X axis 10 kHz to 10 MHz
Y axis Gain error (dB or %, tbd)
1 Min at -40
2 Mean at -40
3 Max at -40
4 Min at 85
5 Mean at 85
6 Max at 85

**Gain deviation vs freq, Vdda=2.7V, P=high G=50, Difference from nominal**
X axis 10 kHz to 10 MHz
Y axis Gain error (dB or %, tbd)
1 Min at -40
2 Mean at -40
3 Max at -40
4 Min at 85
5 Mean at 85
6 Max at 85

**Gain deviation vs freq, Vdda=5V, P=low G=50, Difference from nominal**
X axis 10 kHz to 10 MHz
Y axis Gain error (dB or %, tbd)
1 Min at -40
2 Mean at -40
3 Max at -40
4 Min at 85
5 Mean at 85
6 Max at 85

**Gain deviation vs freq, Vdda=5V, P=high G=50, Difference from nominal**
X axis 10 kHz to 10 MHz
Y axis Gain error (dB or %, tbd)
1 Min at -40
2 Mean at -40
3 Max at -40
4 Min at 85
5 Mean at 85
6 Max at 85

**-3dB BW (Typ, max) vs Vdda**
X axis Vdda 1,7, 2.7, 3.3, 5.0
Y axis BW kHz
1 P=min, typ
2 P=min, min
3 P=low, typ
4 P=low, min
5 P=med, typ
6 P=med, min
7 P=high, typ
8 P=high, min

**-3dB BW (Typ) vs Temp, P=min**
X axis Temp deg C
Y axis -3dB BW kHz
1 G=1
2 G=2
3 G=4
4 G=8
5 G=16
6 G=24
7 G=32
8 G=48
9 G=50

**-3dB BW (Typ) vs Temp, P=low**
X axis Temp deg C
Y axis -3dB BW kHz
1 G=1
2 G=2
3 G=4
4 G=8
5 G=16
6 G=24
7 G=32
8 G=48
9 G=50

**-3dB BW (Typ) vs Temp, P=med**
X axis Temp deg C
Y axis -3dB BW kHz
1 G=1
2 G=2
3 G=4
4 G=8
5 G=16
6 G=24
7 G=32
8 G=48
9 G=50

**-3dB BW (Typ) vs Temp, P=high**
X axis Temp deg C
Y axis -3dB BW kHz
1 G=1
2 G=2
3 G=4
4 G=8
5 G=16
6 G=24
7 G=32
8 G=48
9 G=50

**Voltage noise, Vdda = 5.0V, P=high**
Xaxis freq kHz .01 to 1000 kHz
Yaxis voltage noise nV/rtHz

**PSRR vs freq, Vdda = 5.0V, P=high**
X axis freq 100 Hz to 1.0 MHz
Y axis dB

**Note** More specifications at other voltages and graphs may be added after characterization.

# Component Changes

This section lists the major changes in the component from the previous version.

| Version | Description of Changes | Reason for Changes / Impact |
|---|---|---|
| 1.50 | Added Sleep/Wakeup and Init/Enable APIs. | To support low power modes, as well as to provide common interfaces to separate control of initialization and enabling of most components. |
| | Removed Gain setting of 25. | The gain of 25 was too close to other values and therefore offered no value. |
| | Updated the symbol image and Configure dialog. | These were updated to comply with corporate standards. |
| | Changed the names of the registers by adding "_REG." | Updated to comply with coding guidelines. |

| Version | Description of Changes | Reason for Changes / Impact |
|---|---|---|
| | Added specification table and graphic placeholders | Data to be provided when characterization is complete. |



**PRELIMINARY**