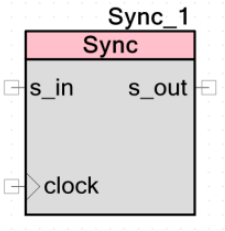
Sync
1.0



Features

- Synchronizes 1 to 32 input signals

General Description

The Sync component resynchronizes a set of input signals to the rising edge of the clock signal.

When to Use a Sync

When you need to use a signal from one clock domain in another clock domain, you can use the Sync component to line up that signal's transitions to the clock domain of the destination. In this case the Sync component is clocked using the same clock as the destination.

Input/Output Connections

This section describes the various input and output connections for the Sync component.

s_in – Input

Signal to be resynchronized. The signal must have a pulse width of at least one clock period plus 2 ns.

clock – Input

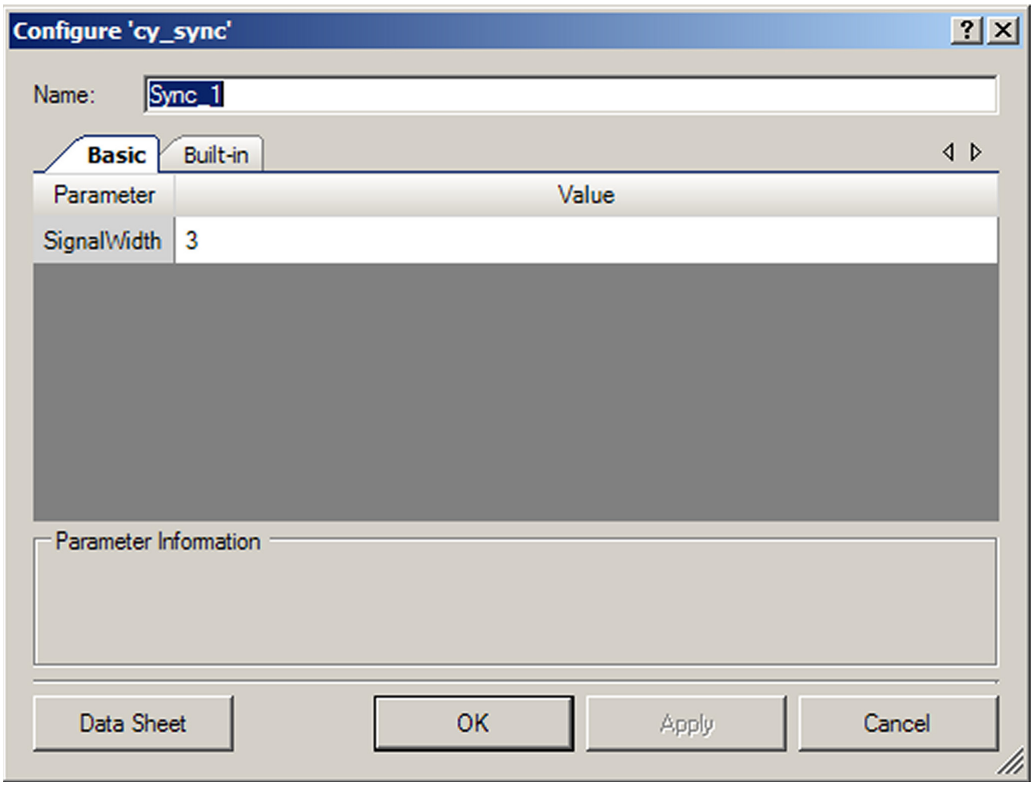
Signal that s_in is to be resynchronized against.

s_out – Output

Resulting resynchronized signal.

Component Parameters

Drag a Sync component onto your design and double-click it to open the **Configure** dialog.



The Sync component provides the following parameter.

SignalWidth

This parameter configures the number of signals that will be synchronized to the associated clock.

Placement

The Sync component has no placement controls. PSoC Creator packs these signals into groups to be placed in the UDB array.

Resources

This circuit is implemented using a status register in synchronizer mode. A single status register can synchronize four signals that are synchronized by the same clock.

Functional Description

The Sync component is implemented using a double synchronizer. A double synchronizer clocks the input signal through two registers in series. The second register is used to resolve a metastable value that could occur if the incoming signal violates setup or hold on the first register.

Component Changes

This section lists the major changes in the component from the previous version.

Version	Description of Changes
1.0.b	Minor datasheet edits and updates
1.0.a	Minor datasheet edits and updates