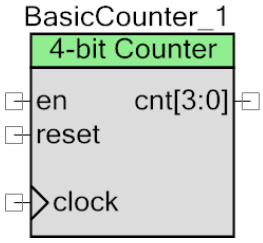
Basic Counter
1.0



Features

- 2 to 32 bit Counter.
- Direct access to count value.
- Enable and reset inputs for easily customizable counter circuit.

General Description

The Basic Counter component provides a selectable-width up-counter, implemented in PLD macrocells.

When to Use a Basic Counter

Use the Basic Counter when the bussed counter value needs to be routed, or when small, basic counter functionality is all that is necessary:

- Mux Sequencer: Connect the cnt output to the input of a mux to easily sequence signals.
- Small Counter: Count level events on the en input without consuming any datapath resources.
- Small Timer: Measure the number of clocks between events without consuming any datapath resources.

Input/Output Connections

This section describes the various input and output connections for the Basic Counter.

en – Input

This input is a level-sensitive enable, determining whether the count value will be incremented.

reset – Input

This input resets the counter value to zero.

clock – Input

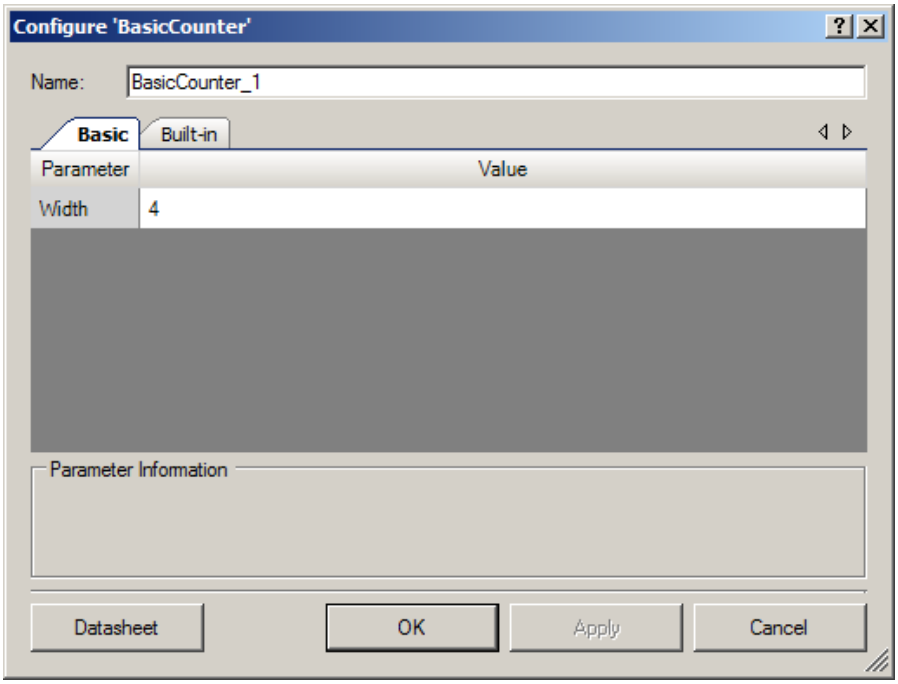
The clock signal determines when to increment the internal counter value. The internal counter value changes when a rising edge of the clock is detected.

cnt – Output

The current value of the counter.

Component Parameters

Drag a Basic Counter onto your design and double-click it to open the **Configure** dialog.



The Basic Counter provides the following parameters.

Width

This parameter defines the size of the internal counter register, and the bus width of the cnt terminal. The value must be between 2 and 32. The default is **4**.

Clock Selection

The Clock input of the Basic Counter determines when the counter value changes, or how often the enable is sampled. The frequency of the clock signal is limited to the frequency range defined in the DC and AC Electrical Characteristics section in this datasheet.

Functional Description

The Basic Counter component is an up-counter with input connections for enable and reset.

- Counter value initializes to 0, and resets to 0 when the reset input is asserted for a rising edge of the clock.
- Counter value increments by 1 on every clock cycle when the enable input is high.
- Counter value rolls over from max-value to 0 (eg. an 8-bit counter will “increment” from 0xFF to 0x00).

Figure 1. Simple Up-Counter w/ Rollover

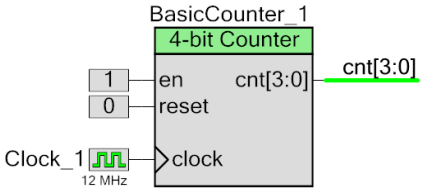
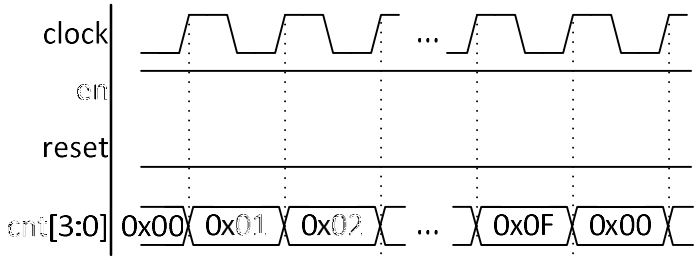


Figure 1 shows the Basic Counter being used to implement a simple up-counter with rollover. This is useful for sequencing inputs to a mux, or if the required period for a counter is a power of 2. Figure 2 shows the resulting waveform from this setup.

Figure 2. Simple Up-Counter w/ Rollover: Waveform



With only the clock input connected, the Basic Counter will count from 0 to 2^{Width} and then roll over back to 0.

Figure 3. Event Counting Using Enable

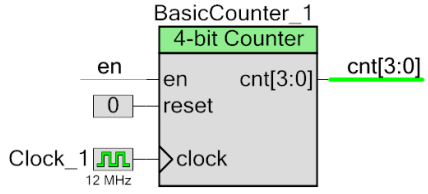
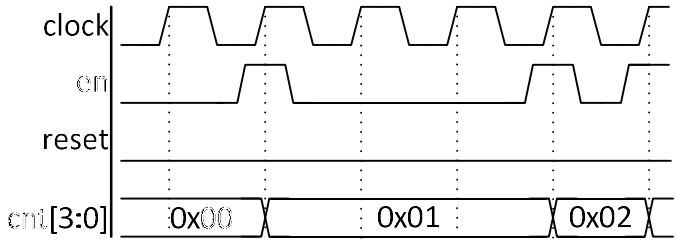


Figure 3 shows the Basic Counter being used to count events using the enable input. Figure 4 shows the resulting waveform from this setup.

Figure 4. Event Counting Using Enable: Waveform



When the enable input is used to count events, the counter value only increments when the enable is high for a rising edge of the clock.

Figure 5. Counter with Period

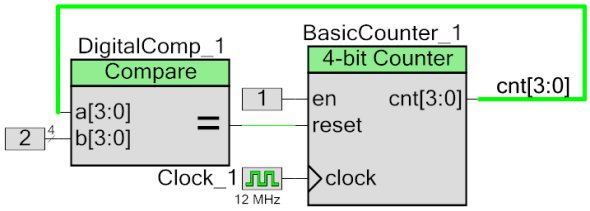
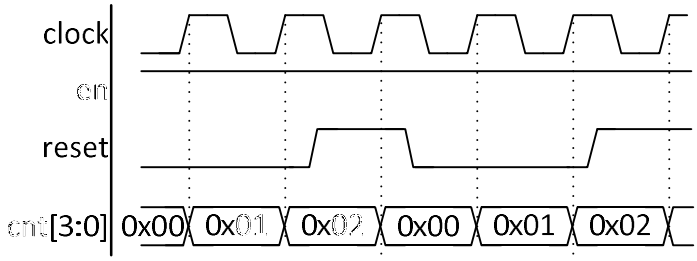


Figure 5 shows the Basic Counter connected to the Digital Comparator to create a counter with a period of 3 (maximum value of 2). Figure 6 shows the resulting waveform from this setup.

Figure 6. Counter with Period: Waveform



When the count value is equal to 2, the reset signal goes high, causing the counter to reset to 0 on the next rising edge of the clock.

Resources

The Basic Counter is synthesized to macrocells in the UDB array. Macrocell usage is dependent on optimizations performed during synthesis. Table 1 provides an estimate of the resource usage for different sizes of the Basic Counter.

Table 1. Resource Usage

Configuration	Resource Type					
	Datapath Cells	Macrocells	Status Cells	Control Cells	DMA Channels	Interrupts
4-bit Basic Counter	–	4	–	–	–	–
8-bit Basic Counter	–	8	–	–	–	–
16-bit Basic Counter	–	17	–	–	–	–
24-bit Basic Counter	–	26	–	–	–	–
32-bit Basic Counter	–	35	–	–	–	–

MISRA Compliance

This section describes the MISRA-C:2004 compliance and deviations for the component. There are two types of deviations defined: project deviations – deviations that are applicable for all PSoC Creator components and specific deviations – deviations that are applicable only for this component. This section provides information on component specific deviations. The project deviations are described in the MISRA Compliance section of the *System Reference Guide* along with information on the MISRA compliance verification environment.

The Basic Counter component does not have any C source code APIs.

DC and AC Electrical Characteristics

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 2. AC Characteristics

Parameter	Description	Min	Typ	Max[1]	Units
f_{CLOCK}	Component clock frequency				
	4-bit Basic Counter	–	–	67	MHz
	8-bit Basic Counter	–	–	67	MHz
	16-bit Basic Counter	–	–	59	MHz
	24-bit Basic Counter	–	–	41	MHz
	32-bit Basic Counter	–	–	30	MHz

1 The values provide a maximum safe operating frequency of the component. The component may run at higher clock frequencies, at which point validation of the timing requirements with STA results is necessary.

Component Changes

Version	Description of Changes	Reason for Changes / Impact
1.0.a	Removed duplicated sections below Clock Selection section.	Formatting clean-up.