Voltage Reference (Vref)
1.50

Features

- Voltage references and supplies
- Multiple options
- Bandgap principle to achieve temperature, and voltage stability

General Description

This component works with both PSoC 3 and PSoC 5 devices. The Voltage Reference (Vref) component provides one of several voltage reference outputs. The 1.024-V and 0.256-V outputs are temperature compensated using the bandgap principle to achieve excellent stability.

Note The Vref component is not intended to source or sink current. It has low drive strength. If high drive strength is needed, buffer the Vref with an Opamp or PGA component.

Every Vref is associated with some analog resource. To enable a Vref, the associated resource must be enabled. All Vrefs default their **AutoEnable** parameter to **true**. Since auto-enable Vrefs automatically enable the associated analog resource, all Vrefs are automatically enabled by default.

When to Use a Vref

Use Vref components for threshold detectors, reference inputs to analog-to-digital converters, comparators, and programmable gain amplifiers. They can also be used whenever you need a known voltage.

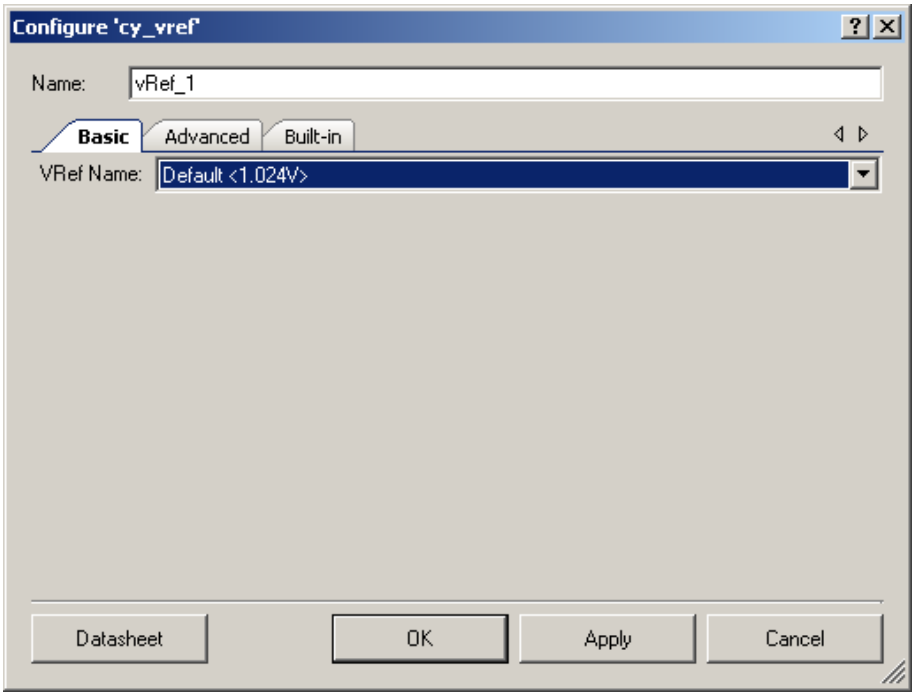
Input/Output Connections

The Vref component has a single output terminal that provides access to the selected voltage reference.

Component Parameters

Drag a Vref onto your design and double click it to open the **Configure** dialog.

Basic Tab



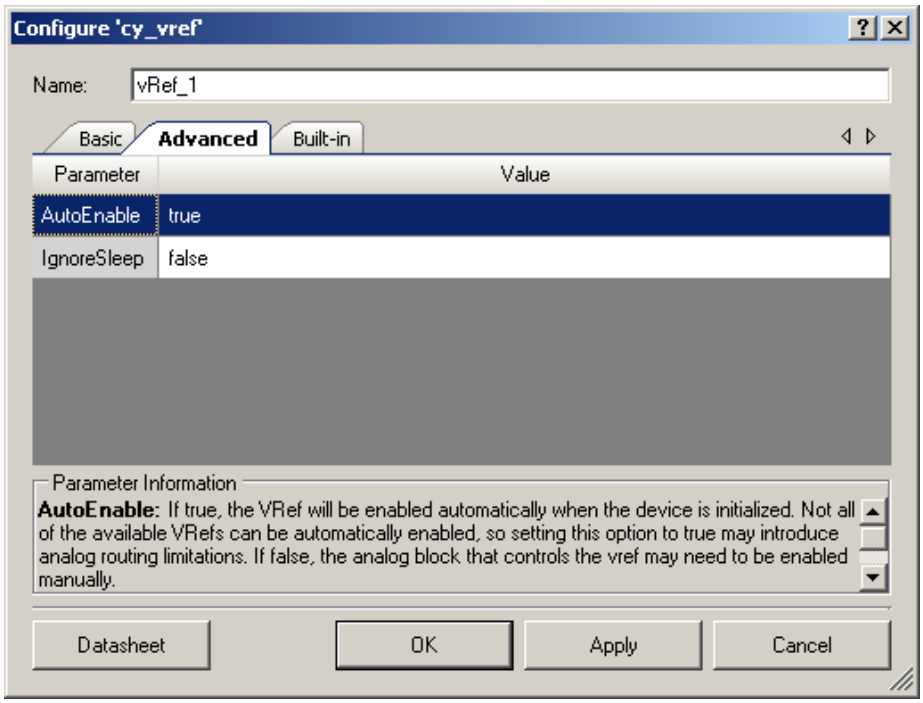
VRef Name

This is the Vref value. Options include:

- 1.024 V (default) – Based on bandgap; see DC and AC Electrical Characteristics section for more information.
- Vssa(GND) – Internal Vssa voltage.
- 0.256 V – Derived from the 1.024 bandgap with a resistive divider; see DC and AC Electrical Characteristics section for more information.
- Vdda/2 – Derived from Vdda with a resistive divider; see DC and AC Electrical Characteristics section for more information.
- Vdda(HiZ) – The Vdda voltage reference is provided with a resistive divider and so has high impedance. Vdda(HiZ) cannot be used if Vdda/2 is used elsewhere. See the Precision Reference chapter of the chip Technical Reference Manual (TRM) for details.
- Vccd – Special 1.8-V reference that is only available for SIO pins. Available in Production PSoC 3 or later only.

- Vddd – Internal Vddd voltage. Available in Production PSoC 3 or later only.
- Vbat – Internal Vbat voltage. Available in Production PSoC 3 or later only.
- Vdda – Internal Vdda voltage. Available in Production PSoC 3 or later only.

Advanced Tab



AutoEnable

The **AutoEnable** parameter applies to the 1.024-V and 0.256 V-Vref components.

When **AutoEnable** is set to **true** (default), the Vref is enabled automatically when the device is initialized and the static analog routes are established. The 1.024-V and 0.256-V Vref components may need to consume a comparator when **AutoEnable** is **true**.

When a 1.024-V or 0.256-V Vref is connected to intended analog block connections such as the comparator, the device automatically enables the Vref when the connected components are enabled. AutoEnable is not necessary in these cases. See the Precision Reference chapter of the chip Technical Reference Manual (TRM) for details.

Note Vref components that require **AutoEnable** set to **true** have reduced routing capability because specific analog routing resources are required to supply the auto-enable Vref.

When **AutoEnable** is set to **false**, the 1.024-V and 0.256-V Vref components are only powered up when the associated analog block is powered up. See the TRM for details.

IgnoreSleep

The **IgnoreSleep** parameter applies to 1.024-V and 0.256-V Vref components.

When **IgnoreSleep** is set to **true**, the Vref remains active when the device goes into a sleep state. This increases the power consumption of the device in the sleep state. The default **IgnoreSleep** value is **false**.

The affected Vrefs consume a comparator when **IgnoreSleep** is **true**. Also, if **IgnoreSleep** is true, **AutoEnable** is automatically set to **true**.

IgnoreSleep cannot be **true** for PSoC 5 devices.

Placement

For a design project, the list of available voltage references is determined by what is available from the selected family or device.

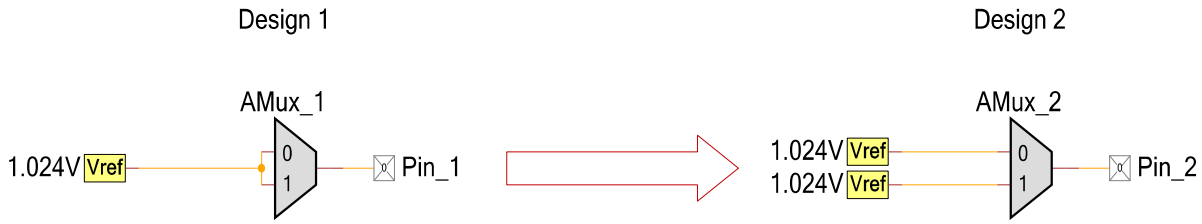
If you place a Vref component in a library project schematic at the generic level, you do not see any references available. In this case, you need to specify a family or device when creating the schematic.

AutoEnable Vref Connecting to an Amux Switchable Connection

The auto-enable 1.024-V or 0.256-V Vref component must be all by itself when connected to an Amux switchable connection. This restriction is introduced so the software can handle the auto-enable Vref feature without ambiguities.

In general, the software must split up signals connected to auto-enable Vrefs, but that is not possible for Amux switchable connections.

In the following example, in order for Design 1 to work, it must be converted to Design2.



If you choose to set the AutoEnable parameter of the Vref component to false, this restriction does not apply.

Resources

When AutoEnable is enabled for an unintended analog block, the 1.024-V Vref consumes a comparator, which will be automatically removed from available comparator resources. A comparator is required to satisfy device requirements of having the analog block associated with the Vref powered up. So, a comparator is allocated to be able to control the power settings and use that Vref.

Functional Description

The Vref component provides one of the available voltage references. Connection is through a single terminal. The Vref component may be shared among several components.

DC and AC Electrical Characteristics

The following values indicate expected performance and are based on initial characterization data. Note that the 1.024-V voltage reference calibration occurs for the buffered ADC_DelSig reference. All of the other 1.024-V references (about 7 or 8 different ones) can be off by several millivolts.

Vref Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{ref}	Precision reference voltage	Initial trimming	1.023 (–0.1%)	1.024	1.025 (+0.1%)	V
	Temperature drift[1]		–	–	20	ppm/°C
	Long term drift		–	100	–	ppm/Khr
	Thermal cycling drift (stability)[1]		–	100	–	ppm

[1] Based on device characterization (Not production tested).

Component Changes

This section lists the major changes in the component from the previous version.

Version	Description of Changes	Reason for Changes / Impact
1.50.c	Minor datasheet edits and updates	
1.50.b	Updated description of Vdda(HiZ)	Description was unclear.
	Updated AutoEnable section to include quarter volt Vref	0.256-V Vref has the same AutoEnable properties as the 1.024-V Vref.
1.50.a	Added characterization data to datasheet	
	Datasheet edits	
1.50	Added AutoEnable and IgnoreSleep parameters to the customizer.	The AutoEnable and IgnoreSleep parameters provide additional functionality and a more intuitive user experience.
	Added the special purpose Vccd Vref for use with SIO pins.	The Vccd reference is used with SIO pins.
	Added Vbat, Vddd, and Vdda references.	The Vbat, Vddd, and Vdda references were added to provide additional functionality.