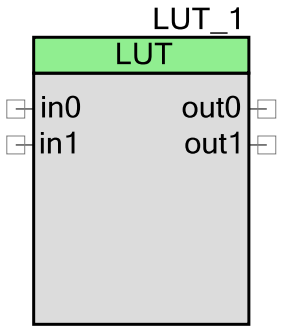
Lookup Table (LUT)
1.0

Features

- 1 to 5 Inputs
- 1 to 8 Outputs
- Configuration Tool
- Optionally Registered Outputs



General Description

The Lookup Table (LUT) component can be set up to perform any logic function with up to five inputs and eight outputs. This is done by generating logic equations that are realized in the UDB PLDs. Optionally, the outputs can be registered.

When to use a digital LUT

The LUT should be used any time that a particular input combination should generate a specific set of outputs. The LUT allows an easy method of specifying the input to output relationship without having to generate specific gate level combinatorial logic. Use of the optional registered output mode allows the generation of sequential logic. State machines may also be created by registering the outputs and routing some of the outputs back to the LUT inputs.

Input/Output Connections

This section describes the various input and output connections for the LUT. An asterisk (*) in the list of I/O's states that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.

in0 to in4 – Input

At least one input is required for this component. Add up to four additional inputs, as desired.

clock – Input *

Select "Register Outputs" option to enable Clock input.

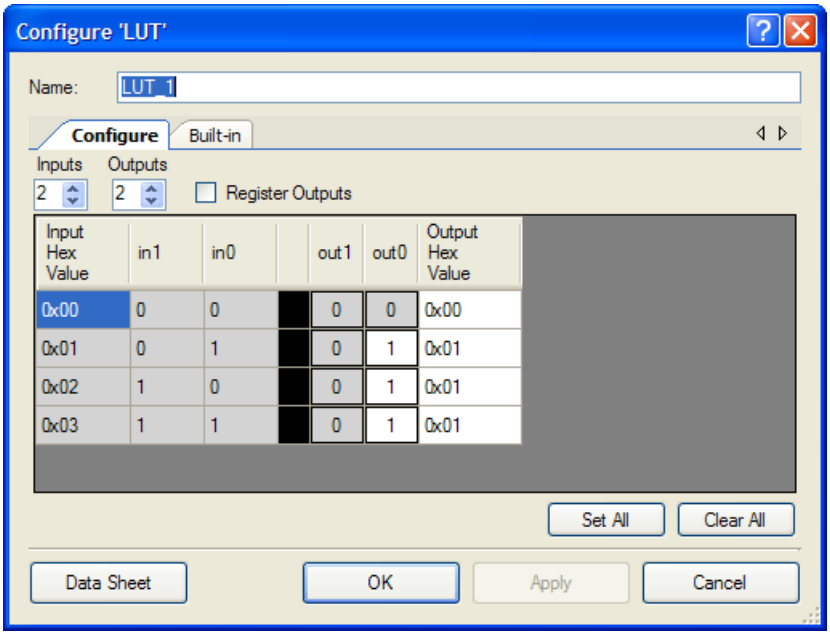
out0 to out7– output

At least one output is required for this component. Add up to seven additional outputs, as desired.

Parameters and Setup

Drag a LUT component onto your design and double-click it to open the Configure dialog.

Figure 1 Configure LUT Dialog



The LUT provides the following parameters.

Hardware Configuration Options

The LUT can configure all of its outputs for all of the possible input combinations. Additionally it can be configured to register the output data on the rising edge of an input clock.

Software Configuration Options

The LUT is a hardware-only block and therefore does not have any software configuration options.

Default Configuration

When first instantiated, the default LUT is configured with two inputs and two outputs, and the "Register Outputs" option is not selected.

Clock Selection

The Clock input of the LUT is only available if the "Register Outputs" option is selected. All outputs will be registered on the rising-edge of this clock. You may select any clock in the system with the single restraint that if any of the outputs go to an I/O they will not work correctly if the LUT is operating faster than 33MHz (the fastest I/O operating speed).

Placement

The LUT is implemented in 0 or more macrocells. Its placement is indeterminate until build time where each piece will be placed for the best fit that meets the timing requirements. If no clock is used for registered outputs, the macrocells can be placed anywhere in the UDB array.

Resources

Resolution	Digital Blocks					API Memory (Bytes)		Pins (per External I/O)
	Datapaths	Macro cells	Status Registers	Control Registers	Counter7	Flash	RAM	
N Outputs	0	N *	0	0	0	0	0	0

* Assumes no two outputs are the same equation because the build will optimize this to a single output and use less macrocells, p-Terms and routing.

Application Programming Interface

The LUT does not have any API interface because it is a hardware only design.

Sample Firmware Source Code

No firmware is necessary for operation of the LUT.

Interrupt Service Routine

There is no Interrupt Service Routine for the LUT.

Functional Description

Not applicable

References

Not applicable

DC and AC Electrical Characteristics

5.0V/3.3V DC and AC Electrical Characteristics

Parameter	Typical	Min	Max	Units	Conditions and Notes
Input					
Input Voltage Range	---		Vss to Vdd	V	
Input Capacitance	---		---	pF	
Input Impedance	---		---	Ω	
Maximum Clock Rate	---		67	MHz	