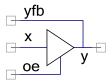


Tri-State Buffer (Bufoe)

1.0

Features

- Buffer with Output Enable signal
- Feedback signal



General Description

The Tri-State Buffer (Bufoe) component is a non-inverting buffer with an active low output enable signal. When the output enable signal is true, the buffer functions as a standard buffer. When the output enable signal is false, the buffer turns off.

When to use a Tri-State Buffer

The Tri-State Buffer should be used to interface to a shared bus such as I²C. Tri-State Buffers should not be used for internal logic. Tri-State Buffers can only be used with an I/O pin.

Input/Output Connections

This section describes the various input and output connections for the Tri-State Buffer.

x - Input

Input to the buffer.

oe – Input

This is the output enable connection. When oe is true ('0'), the buffer will be on. When oe is false ('1'), the buffer output is in a high-impedance state.

y – Inout

This connection is connected to the output of the buffer. When oe is true ('0'), this connection is an output, and y has the same value as x. When oe is false ('1'), this connection may be used as an input.

yfb – Output

This is the feedback signal from the y connection. When oe is true ('0') the yfb and y have the same value as x. When oe is false ('1'), yfb has the same value seen at y irrespective of x.

Component Parameters

Not Applicable

Placement

Each I/O port is limited to four unique output enable signals.

Resources

Not Applicable

Application Programming Interface

Not Applicable

Sample Firmware Source Code

Not Applicable

Interrupt Service Routine

Not Applicable

Functional Description



DC and AC Electrical Characteristics

The following values are indicative of expected performance and based on initial characterization data.

5.0V/3.3V DC and AC Electrical Characteristics

Parameter	Typical	Min	Max	Units	Conditions and Notes
Input					
Input Voltage Range			Vssd to Vddio	V	
Input Capacitance				pF	
Input Impedance				Ω	
Maximum Clock Rate			33	MHz	

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