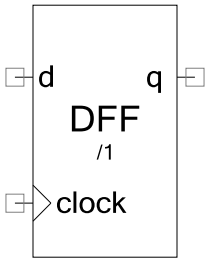
D Flip Flop
1.0

Features

- Stores a digital value
- Asynchronous Reset or Preset
- Optional array of D Flip Flops



General Description

The D Flip Flop stores a digital value.

When to use a D Flip Flop

The D Flip Flop should be used to implement sequential logic.

Input/Output Connections

This section describes the various input and output connections for the D Flip Flip. An asterisk (*) in the list of I/O's states that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.

d – Input

This input determines the next value of the output. The output does not change until the next rising edge of the clock.

clock – Input

The clock signal determines when the output will change. The output changes when a rising edge of the clock is detected.

ar – Input *

Asynchronous reset. When this input is true, the output will immediately change to false. This input only appears if the needAR parameter is true.

ap – Input *

Asynchronous preset. When this input is true, the output will immediately change to true. This input is only available if the needAP parameter is true.

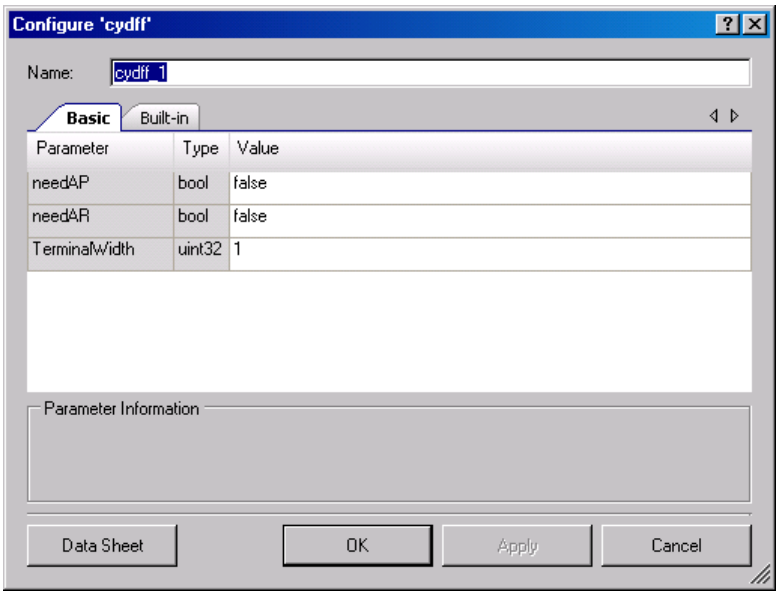
q – Output

The stored value of the D Flip Flop.

Component Parameters

Drag a D Flip Flop onto your design and double-click it to open the Configure dialog.

Figure 1 Configure D Flip Flop Dialog



The D Flip Flop provides the following parameters.

needAP

This parameter controls whether the asynchronous preset (AP) input is visible. The asynchronous reset and asynchronous preset may not be used simultaneously. The default is false.

needAR

The parameter controls whether the asynchronous reset (AR) input is visible. The asynchronous reset and asynchronous preset may not be used simultaneously. The default is false.

TerminalWidth

An array of the D Flip Flop can be created which may be useful if the input or output is a bus. This parameter defines the bus width of the d and q terminals. The default is 1.

Placement

All D Flip Flop components in the same UDB must have the same ar or ap input. All D Flip Flop components in the same PLD must have the same clock signal.

Resources

The D Flip Flop uses one macrocell. If the TerminalWidth parameter is greater than 1, the D Flip Flop uses a number of macrocells equal to TerminalWidth.

Application Programming Interface

Not applicable

Sample Firmware Source Code

Not applicable

Interrupt Service Routine

Not applicable

Functional Description

Not applicable

DC and AC Electrical Characteristics

The following values are indicative of expected performance and based on initial characterization data.

5.0V/3.3V DC and AC Electrical Characteristics

Parameter	Typical	Min	Max	Units	Conditions and Notes
Input					
Maximum Clock Rate	---		80	MHz	