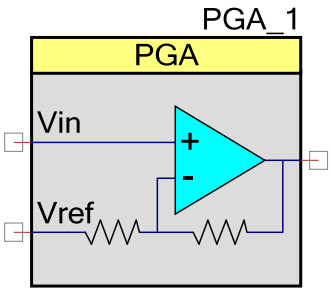
Programmable Gain Amplifier (PGA)

1.20

Features

- Gain steps from 1 to 50
- High input impedance
- Selectable input reference
- Adjustable power settings



General Description

The PGA component implements an Opamp-based non-inverting amplifier with user-programmable gain. This amplifier has high input impedance, wide bandwidth, and selectable input voltage reference.

When to use a PGA

The PGA is used anytime a signal does not have sufficient amplitude. A PGA may be placed in front of a comparator, ADC, or mixer to increase the signal amplitude.

Another use for the PGA is to provide a high input impedance to the next stage. Components that are implemented in switched capacitor blocks may have a lower than desired input impedance, or an input impedance that is a function of the switch frequency. In either case, the PGA can be used as a unity gain amplifier to buffer the input and drive the next stage.

Input/Output Connections

This section describes the various input and output connections for the PGA. An asterisk (*) in the list of I/O's states that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.

Vin – Analog

Vin is the input signal terminal.

Vref – Analog *

Vref is the input terminal for a reference signal. You can choose between an external reference (to the component) or an internal Vss (ground).

Vout – Analog

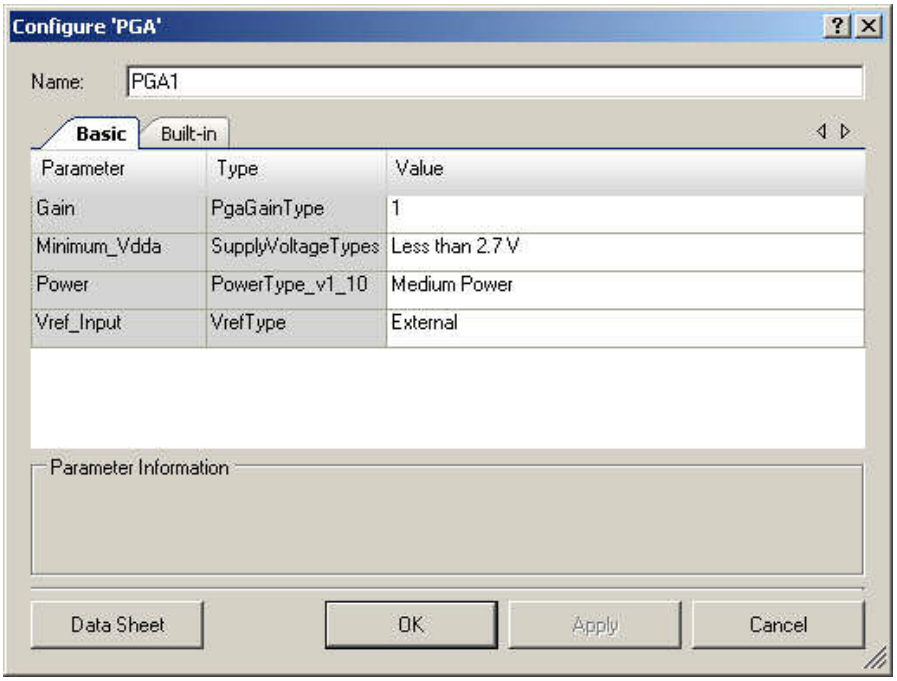
Vout is the output voltage signal terminal. Vout is a function of (Vin - Vref) times the specified Gain:

*Vout = Vref + (Vin - Vref) * Gain*

Parameters and Setup

Drag a PGA component onto your design and double-click it to open the Configure dialog.

Figure 1 Configure PGA Dialog



Gain

This sets the initial gain of the PGA. The gain may be selected from the following set of allowed values: 1 (default), 2, 4, 8, 16, 24, 25, 32, 48, and 50.

Power

This sets the initial drive power of the PGA. The power determines the speed with which the PGA reacts to changes in the input signal. There are four power settings; Minimum, Low, Medium (default), and High. A Low Power setting results in the slowest response time and a High Power setting results in the fastest response time. The power can be set at run time using the SetPower() API.

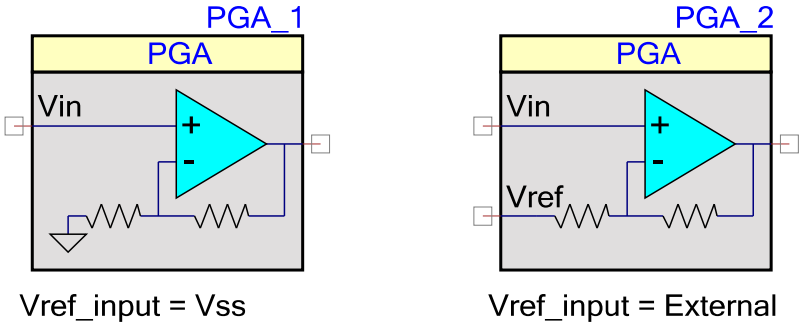
Vref_Input

This parameter is used to select the input voltage reference. The options include:

- "Internal Vss" – Uses a ground signal internal to the component
- "External" (default) – Signal on the Vref terminal provides the amplifier reference.

The following diagram illustrates how the symbol changes based on the selection of this parameter.

Figure 2 PGA Configurations



Placement

There are no placement specific options.

Resources

The PGA uses one SC/CT block.

Application Programming Interface

Application Programming Interface (API) routines allow you to configure the component using software. The following table lists and describes the interface to each function. The subsequent sections cover each function in more detail.

By default, PSoC Creator assigns the instance name "PGA_1" to the first instance of a component in a given design. You can rename it to any unique value that follows the syntactic rules for identifiers. The instance name becomes the prefix of every global function name, variable, and constant symbol. For readability, the instance name used in the following table is "PGA".

Function	Description
void PGA_Start(void)	Start the PGA.

Function	Description
void PGA_Stop(void)	Power down the PGA.
void PGA_SetGain(uint8 gain)	Set gain to pre-defined constants.
void PGA_SetPower(uint8 power)	Set drive power to one of four settings.

void PGA_Start(void)

Description: Turns on the amplifier with the power and gain based on the settings provided during the configuration or the current values after a PGA_Stop() has been called.

Parameters: None

Return Value: None

Side Effects: None

void PGA_Stop(void)

Description: Turn off PGA and enable its lowest power state.

Parameters: None

Return Value: None

Side Effects: None. Does not affect power or gain settings

void PGA_SetPower(uint8 power)

Description: Sets the drive power to one of four settings; minimum, low, medium, or high.

Parameters: (uint8) power: See the following table for valid power settings.

Power Setting	Notes
PGA_MINPOWER	Minimum active power and slowest reaction time.
PGA_LOWPOWER	Low power and speed.
PGA_MEDPOWER	Medium power and speed.
PGA_HIGHPOWER	Highest active power and fastest reaction time.

Return Value: None

Side Effects: None

void PGA_SetGain(uint8 gain)

Description: Set the amplifier gain to a value between 1 and 50.

Parameters: uint8 gain: See table below for valid gain settings.

Gain Setting	Notes
PGA_GAIN_01	Gain = 1
PGA_GAIN_02	Gain = 2
PGA_GAIN_04	Gain = 4
PGA_GAIN_08	Gain = 8
PGA_GAIN_16	Gain = 16
PGA_GAIN_24	Gain = 24
PGA_GAIN_25	Gain = 25
PGA_GAIN_32	Gain = 32
PGA_GAIN_48	Gain = 48
PGA_GAIN_50	Gain = 50

Return Value: None

Side Effects: None

Sample Firmware Source Code

The following is a C language example demonstrating the basic functionality of the PGA component. This example assumes the component has been placed in a design with the default name "PGA_1."

Note If you rename your component you must also edit the example code as appropriate to match the component name you specify.

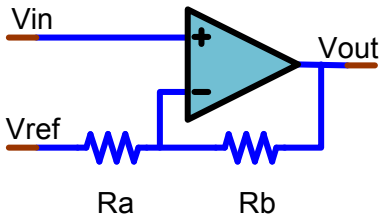
```
#include <device.h>

void main()
{
    PGA_1_Start();
    PGA_1_SetGain(PGA_1_GAIN_24);
    PGA_1_SetPower(PGA_1_MEDPOWER);
}
```

Functional Description

The PGA is constructed from a generic SC/CT block. The gain is selected by adjusting two resistors, Ra and Rb. (See Figure 2). Ra may be set to either 20K or 40K ohms. Rb may be set between 20K and 1000K ohms, to generate the possible gain values selectable in either the parameter dialog or the SetGain function. You are not required to select the resistance values, but instead the parameter dialog and SetGain function select the proper resistor values for the selected gain.

Figure 3 PGA Schematic



TBD - Add power vs bandwidth graph

Registers

TBD

Component Debug Window

The PGA component supports the PSoC Creator component debug window. Refer to the appropriate device data sheet for a detailed description of each register. The following registers are displayed in the PGA component debug window.

Register:	PGA_1_CR0
Name:	Switched Capacitor Control Register 0
Description:	Register bits 3:1 configure the switch capacitor block operating mode. This field is set to 110b for the PGA component.
Register:	PGA_1_CR1
Name:	Switched Capacitor Control Register 1
Description:	Register fields configure drive mode, compensation capacitor values, and gain setting of the switch capacitor block.
Register:	PGA_1_CR2
Name:	Switched Capacitor Control Register 2
Description:	Register fields configure the input impedance, feedback impedance and the reference ground selection for the switch capacitor block.

Register: PGA_1_PWRMGR

Name: Active Power Mode Configuration Register 9

Description: Register bits 3:0 enable power to the four switch capacitor blocks.

DC and AC Electrical Characteristics

The following values are indicative of expected performance and based on initial characterization data. Unless otherwise specified in the tables below, all T_A = 25°C, V_{dd} = 5.0V, Power HIGH, Op-Amp bias LOW, output referenced to Analog Ground = V_{ssa} .

5.0V/3.3V DC Electrical Characteristics

Parameter	Typical	Min	Max	Units	Conditions and Notes
Gain Deviation from Nominal					
G = 1				%	
G = 2				%	
G = 4				%	
G = 8				%	
G = 16				%	
G = 24				%	
G = 25				%	
G = 32				%	
G = 48				%	
G = 50				%	
Input					
Input Offset Voltage				mV	
Input Voltage Range				V	
Leakage				nA	
Input Capacitance				pF	
Output Swing				V	
PSRR				dB	
Operating Current					

Parameter	Typical	Min	Max	Units	Conditions and Notes
Minimum Power				uA	
Low Power				uA	
Medium Power				uA	
High Power				uA	

5.0V/3.3V AC Electrical Characteristics

Parameter	Typical	Min	Max	Units	Conditions and Notes
AC Electrical Characteristics					
Slew Rate (20% to 80%)					
Minimum Power				V/uS	
Low Power				V/uS	
Medium Power				V/uS	
High Power				V/uS	
Settling Time					
Minimum Power				uS	
Low Power				uS	
Medium Power				uS	
High Power				uS	
Noise					
Minimum Power				nV/√Hz	
Low Power				nV/√Hz	
Medium Power				nV/√Hz	
High Power				nV/√Hz	

Note More specifications at other voltages and graphs will be added after characterization.