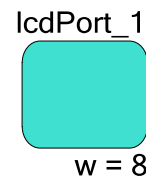


LCD Port

1.10

Features

- Common and segment selection
- Variable widths



General Description

The LCD port provides configuration as either common or segment for the appropriate I/O(s). The port allows for the creation of per-pin aliases, which may be viewed in the PSoC Creator Pin Editor and used in the generated port APIs.

When to use a Port

Use a port when a design needs to generate or access an off-device signal. Use an appropriate port for the type of signal being accessed. LCD ports are optimized for their specific application.

Input/Output Connections

The LCD port does not have any connections.

PRELIMINARY

Component Parameters

Drag a Port onto your design and double-click it to open the Configure dialog.

Basic Tab

Configure 'cy_lcd_port'

Name:

Basic | Pins | Built-in

Parameter	Type	Value
LCDDrive	PortLCDDrive	PortLCDDrive_Common
PowerOnResetState	PortPORState	PortPORState_InDisabledOutHiZ
SWControl	bool	true
Width	uint8	8

Parameter Information

Data Sheet OK Apply Cancel

LCDDrive

This parameter configures all pins in the port as either common or segment drive pins.

PowerOnResetState

This parameter specifies the power on reset state of the port. Legal values include:

- **InDisabledOutHiZ** (default) – the input disabled the output is Hi-Z
- InEnabledOut1 – input enabled and the output is a logic one
- InEnabledOut0 – input enabled and the output is a logic zero
- InEnabledOutHiZ – input enabled and the output is Hi-Z

SWControl

Specifies whether the LCD Port will be controlled via software or the built-in hardware of the device.

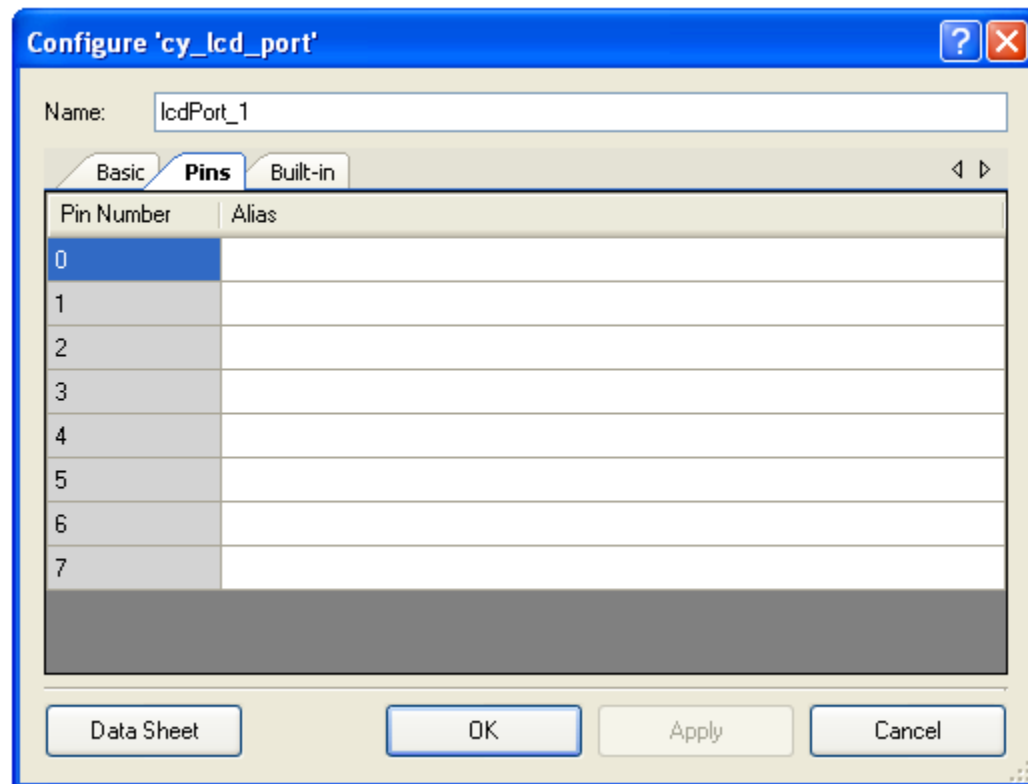
PRELIMINARY



Width

Specifies the width in bits of the logical port (default is 8).

Pins Tab



Alias

This parameter assigns an alias for each pin in the port. The alias is presented in the pin editor and in the generated APIs for the port.

Resources

All ports consume one physical pin, per bit of their width parameter.

Application Programming Interface

Not applicable.

DC and AC Electrical Characteristics

The following values are indicative of expected performance and based on initial characterization data.

5.0V/3.3V DC and AC Electrical Characteristics

Parameter	Typical	Min	Max	Units	Conditions and Notes
Input					
Input Voltage Range	---		Vss to Vdd	V	
Input Capacitance	---		---	pF	
Input Impedance	---		---	Ω	
Maximum Clock Rate	---		67	MHz	

© Cypress Semiconductor Corporation, 2009. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

PSoC® Creator™, Programmable System-on-Chip™, and PSoC Express™ are trademarks and PSoC® is a registered trademark of Cypress Semiconductor Corp. All other trademarks or registered trademarks referenced herein are property of the respective corporations.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

PRELIMINARY

