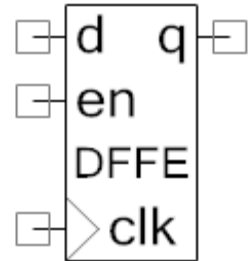


D Flip Flop w/ Enable

1.0

Features

- Enable input allows d input to be selectively captured.
- Configurable width for array of D Flip Flops with a single enable.



General Description

The D Flip Flop w/ Enable selectively captures a digital value.

When to Use a D Flip Flop w/ Enable

Use the D Flip Flop w/ Enable to implement sequential logic.

Input/Output Connections

This section describes the various input and output connections for the D Flip Flop w/ Enable.

d – Input

This input determines the next value of the output. The output does not change until the next rising edge of the clock.

en – Input

This input determines whether the current value on the d input will be stored and propagated to the output.

clock – Input

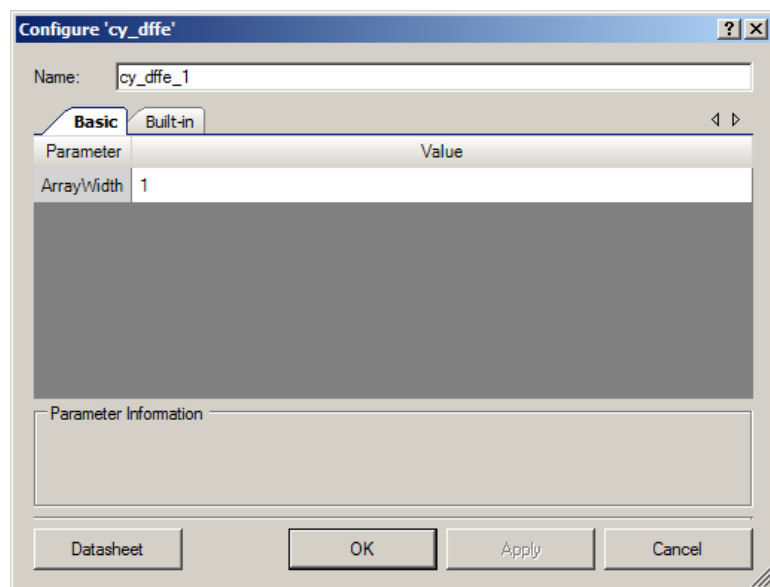
The clock signal determines when the output will change. The output changes when a rising edge of the clock is detected.

q – Output

The stored value.

Component Parameters

Drag a D Flip Flop w/ Enable onto your design and double-click it to open the **Configure** dialog.



The D Flip Flop w/ Enable provides the following parameters.

ArrayWidth

You can create an array of D Flip Flops with a single Enable, which is useful if the input or output is a bus. This parameter defines the bus width of the d and q terminals. The value must be between 1 and 32. The default is **1**.

Functional Description

The D Flip Flop w/ Enable is implemented in PLD macrocells. All macrocell flip-flops are initialized to a 0 value at power up and after any reset of the device. The enable functionality is implemented in product terms in the PLD using the following logical equation:

$$Q = \text{En} ? D : Q_{\text{PREV}}$$

Table 1. 1-ArrayWidth D Flip Flop w/ Enable Truth Table

Q _{PREV}	Enable	D	Q
0	0	X	0
1	0	X	1
X	1	0	0
X	1	1	1

A letter 'X' in the truth table indicates that the input does not affect the output.



Resources

The D Flip Flop w/ Enable uses one macrocell. If the ArrayWidth parameter is greater than 1, the D Flip Flop w/ Enable uses a number of macrocells equal to ArrayWidth. All D Flip Flop w/ Enable components in the same PLD must have the same clock signal for clocking.

MISRA Compliance

This section describes the MISRA-C:2004 compliance and deviations for the component. There are two types of deviations defined: project deviations – deviations that are applicable for all PSoC Creator components and specific deviations – deviations that are applicable only for this component. This section provides information on component specific deviations. The project deviations are described in the MISRA Compliance section of the *System Reference Guide* along with information on the MISRA compliance verification environment.

The D Flip Flop w/ Enable component does not have any C source code APIs.

DC and AC Electrical Characteristics

The D Flip Flop w/ Enable component supports the maximum device frequency.

Component Changes

Version 1.0 is the first release of the D Flip Flop w/ Enable Component

© Cypress Semiconductor Corporation, 2010-2012. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

PSoC® Creator™, Programmable System-on-Chip™, and PSoC Express™ are trademarks and PSoC® is a registered trademark of Cypress Semiconductor Corp. All other trademarks or registered trademarks referenced herein are property of the respective corporations.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

