Minutes from team meeting held on 8/6/2012:

ARs:

- **Driver-side team**: test our multi-queue support on drivers suggested by sponsors.

Team meeting 8/6

- Questions for sponsors:
- “Iperf” tools?
- How do we get register contents?
- Are we finished with requirement 2.2.3?
- Sponsor meeting will be at 7:05 p.m.
- We will go over the requirements list with the sponsors.

Sponsor meeting 8/6

- Registers are represented by macros to read in and write out to PCI device.
- hdw_addr - take address and offset that you want.
- There are some clear-on-read registers, so be careful!
- Dumping the entire bar is ok just to get register access working.
- Error injection: there are injectable errors that are correctable.
- PJ and Shannon will come up with some error injection tests.
- Writing to the tail register and moving it will induce an error.
- Use the mmap utility and write to an address.
- Ethwrite is another useful utility.
- Multi-queue devices use an array of tx and rx rings.
- ‘IGB’ driver supports multi-queue?
- e1000e driver supports some multi-queueing.
- AR: test our multi-queue support on these drivers.
- 10 gb Intel NIC driver - supports multi-queue.
- ‘Big P’ used for load testing?
- Simulate multiple CPUs on the virtual machine.
- NetPerf utility - used for intensive load testing.
- 10 gb cards - PJ has extra cards for testing.
- We will have another meeting with PJ and Shannon 2 weeks from 8/6.