Computer Architecture
Computer Engineering Track
Optional Tutorial 6

# The Revision of Selected Topics:
# SRAM and DRAM
# Latches

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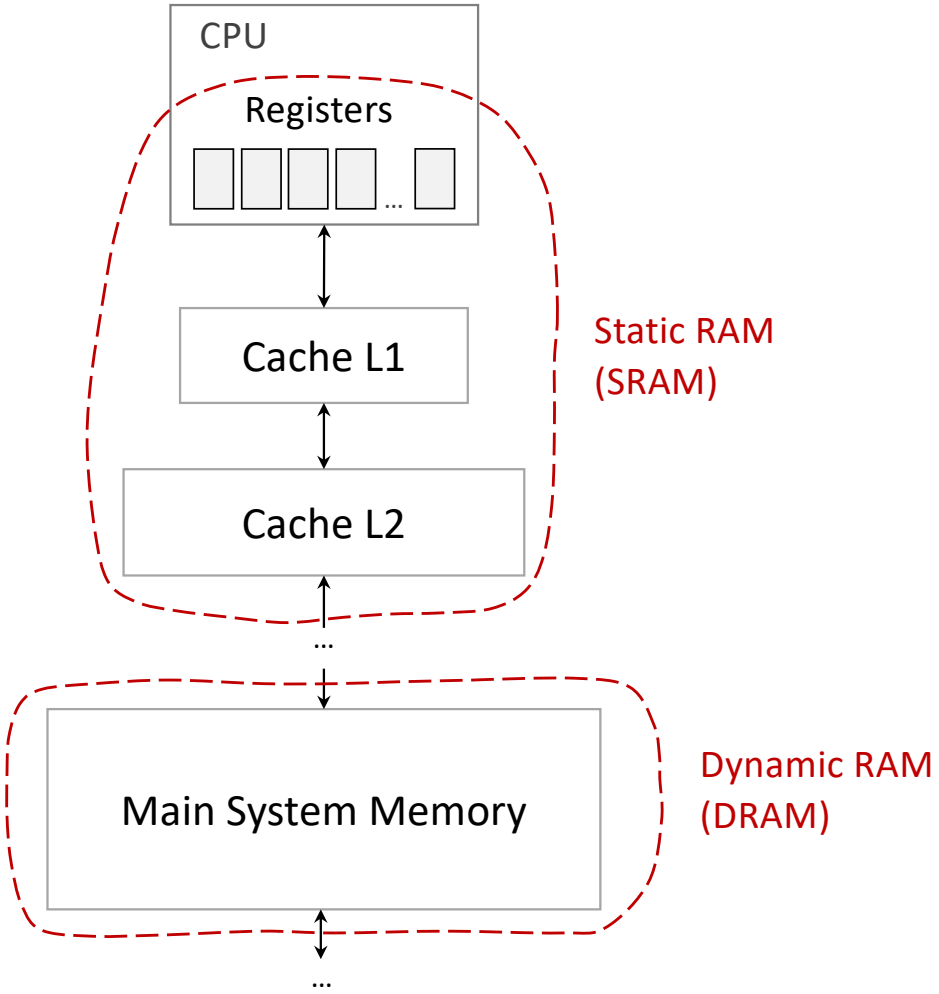
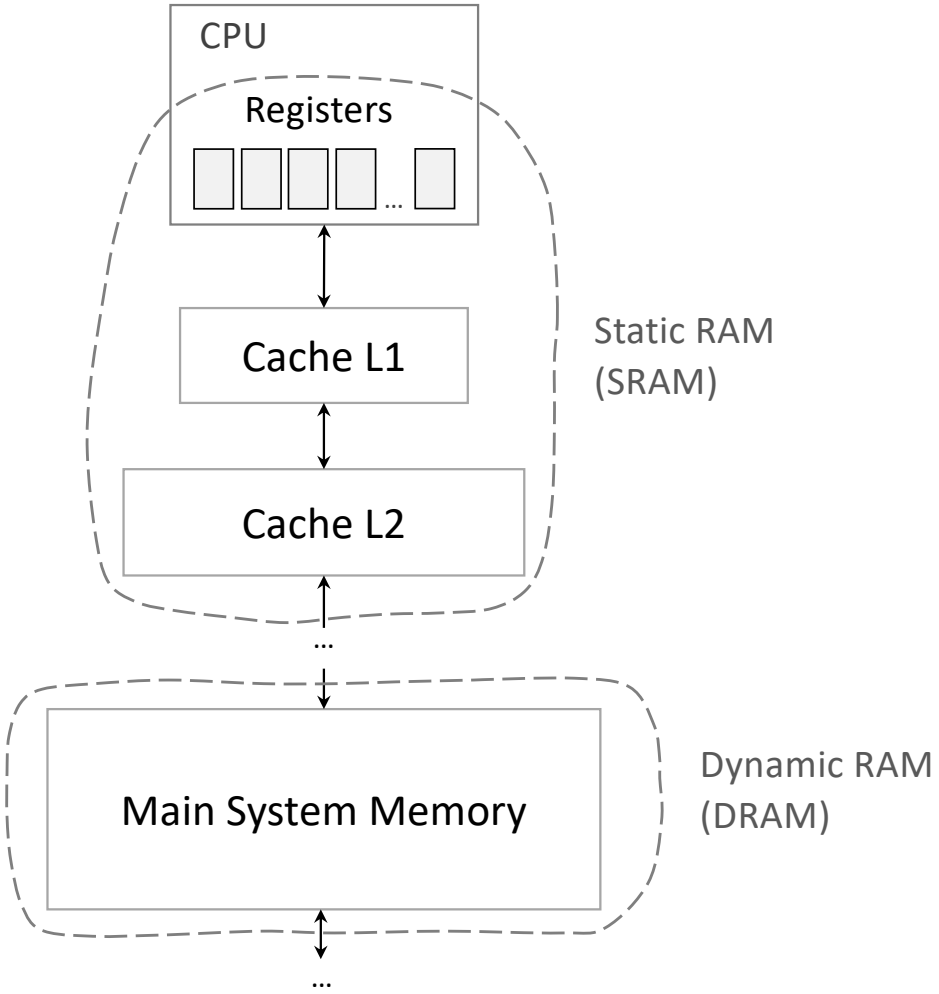
INNOPOLIS UNIVERSITY

# Memory Hierarchy – the Fundamental Idea of Computer Architecture



# The Comparison of DRAM and SRAM Memory Types




| **Characteristic** | **SRAM** | **DRAM** |
|---|---|---|
| Access Speed | Faster | Slower |
| Storage Capacity | Smaller | Larger |
| Storage Element | Flip-flop (Latch) | Capacitor |
| Usage | CPU cache, registers | System memory |
| Cost | Expensive | Cheaper |
| Power Consumption | Lower | Higher |
| Organisation | Complex | Simpler |
| Power Leakage | Not present | Significant |
| Chip Reliability | More reliable | Less reliable |
| Volatility | Both are volatile<br>(require electrical power to keep data) | |
| Memory Cell Access | Each cell is accessed directly, unlike<br>Sequential Access Memory (SAM) | |

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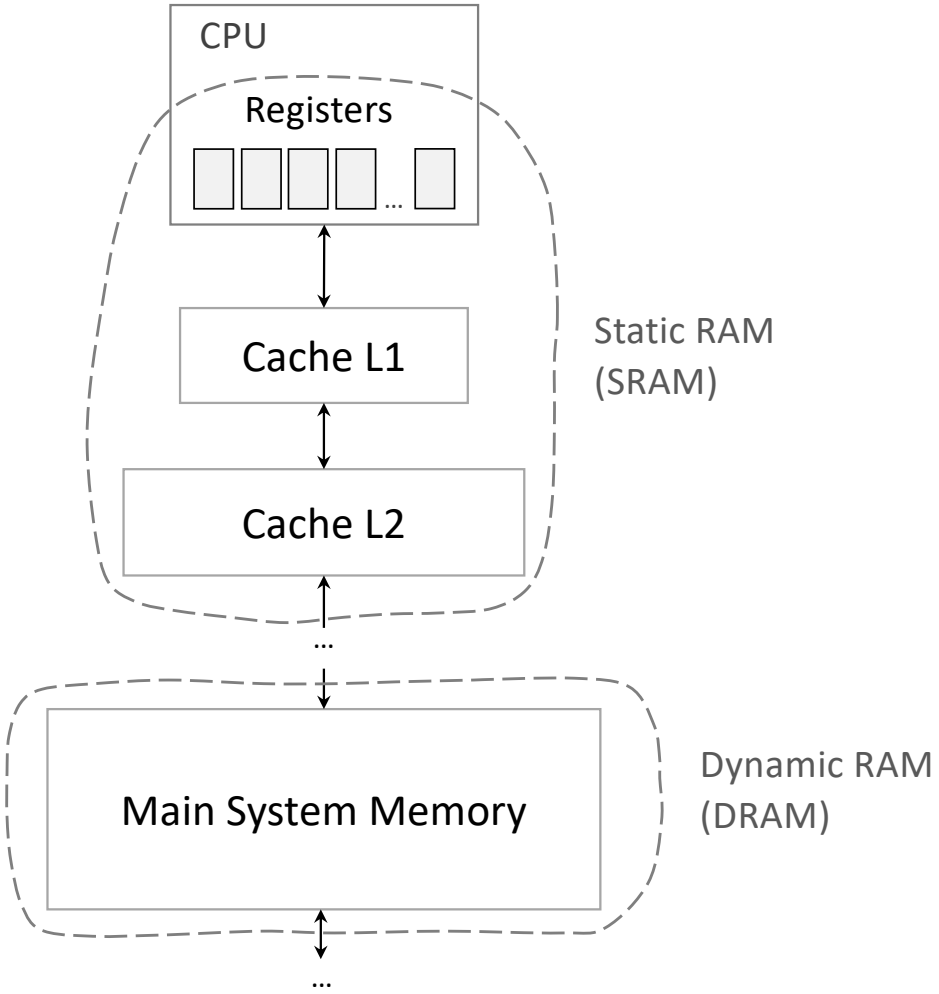


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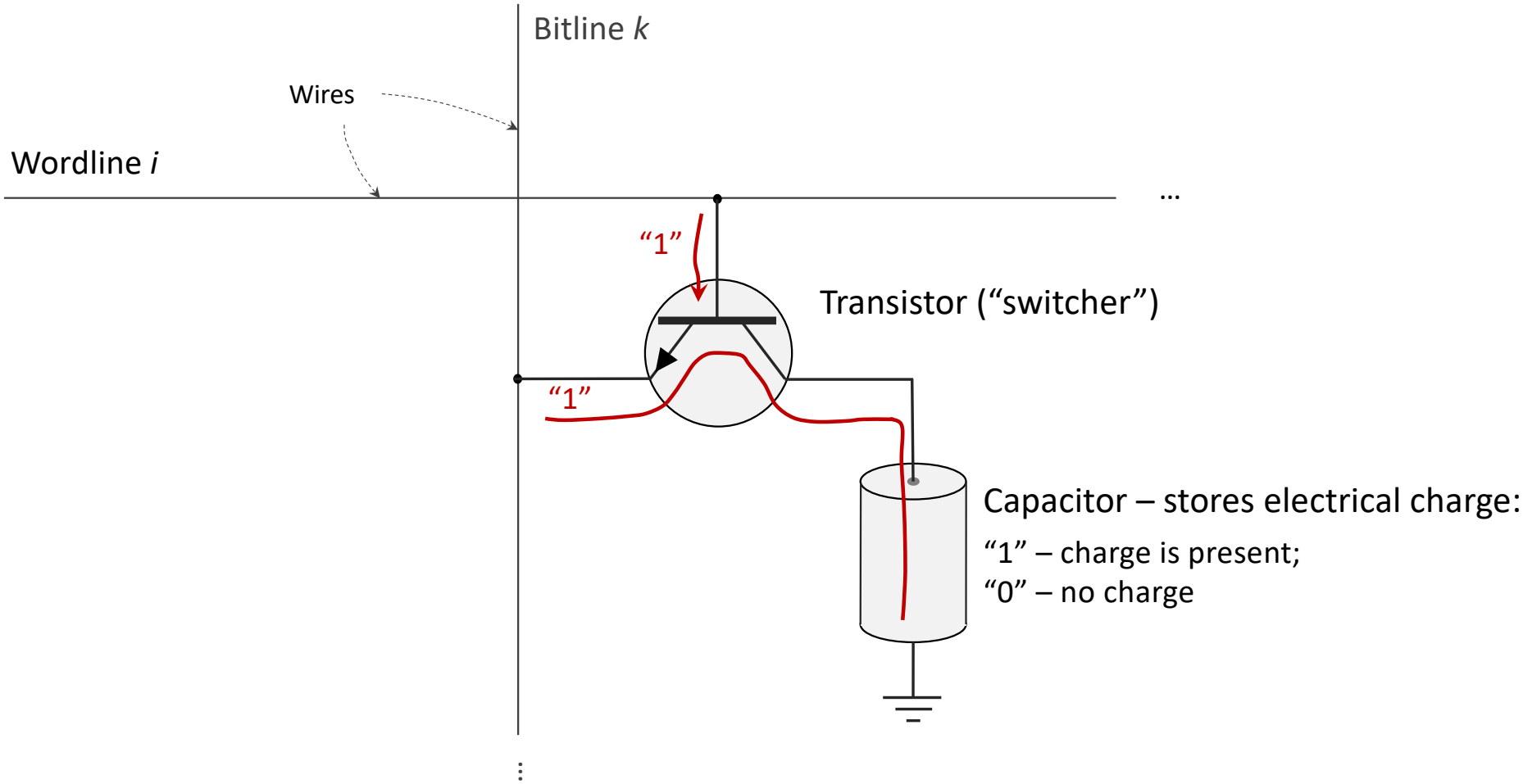
Capacitor: a physical device to store electrical charge

# DRAM memory cell



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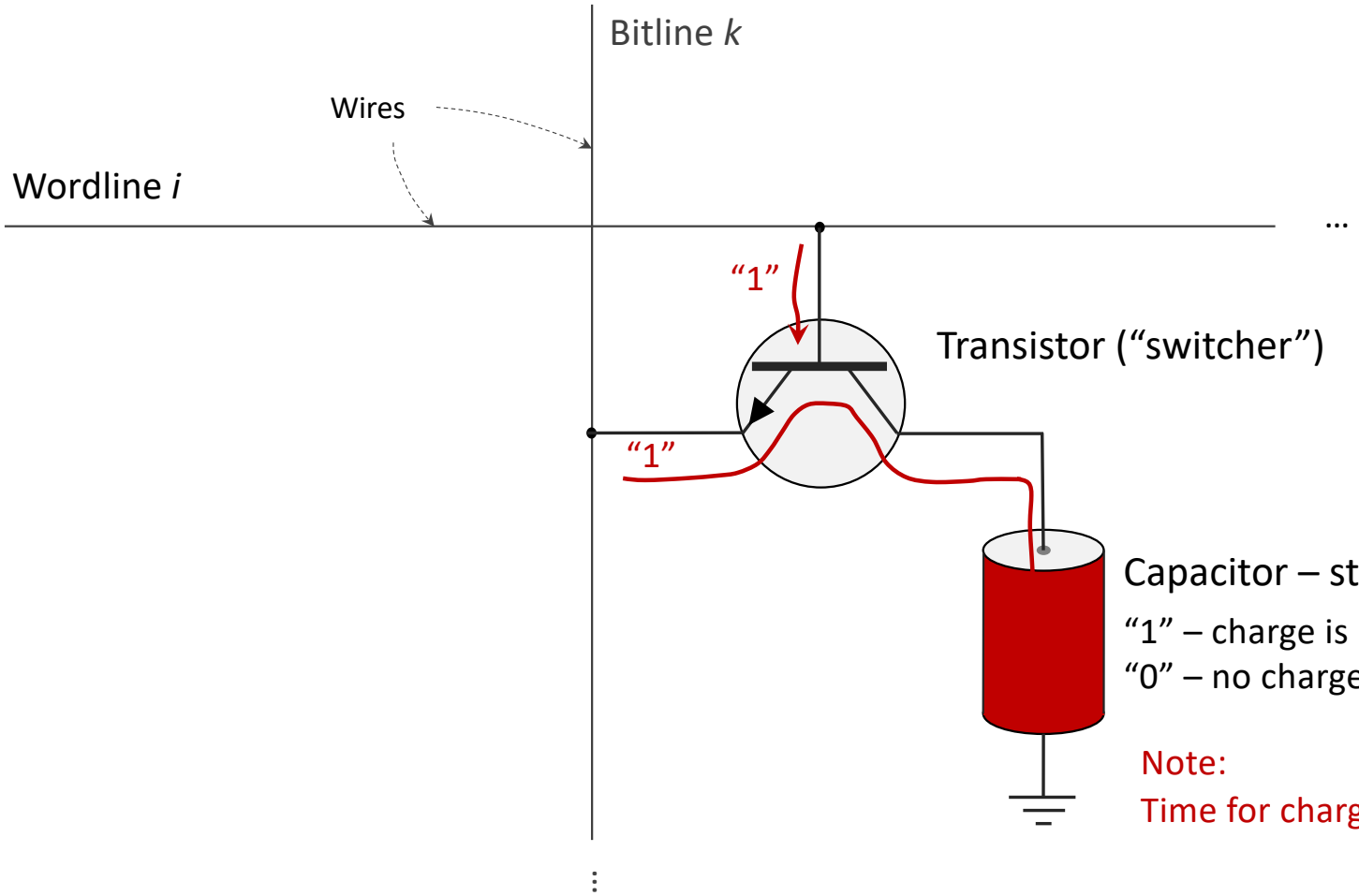

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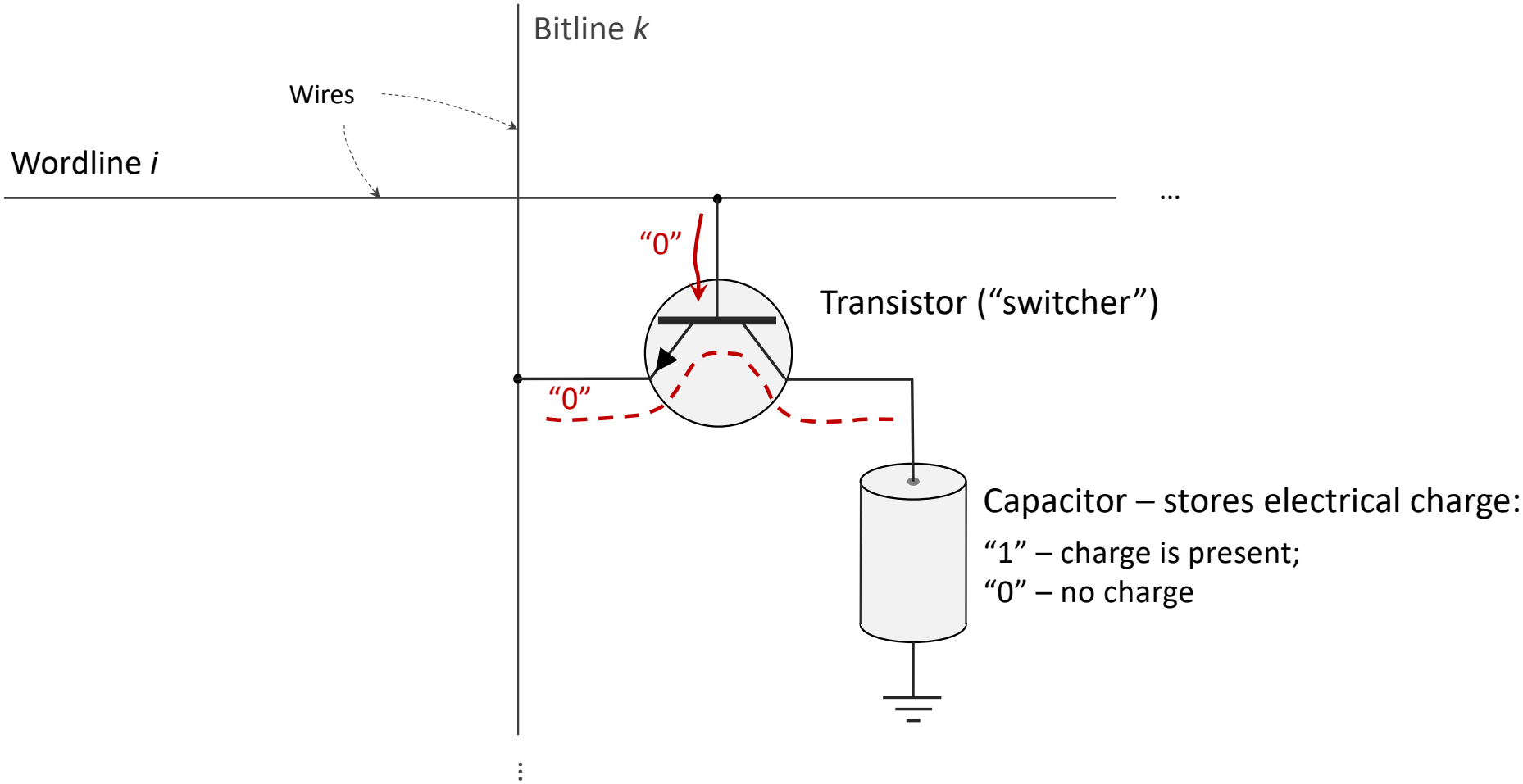

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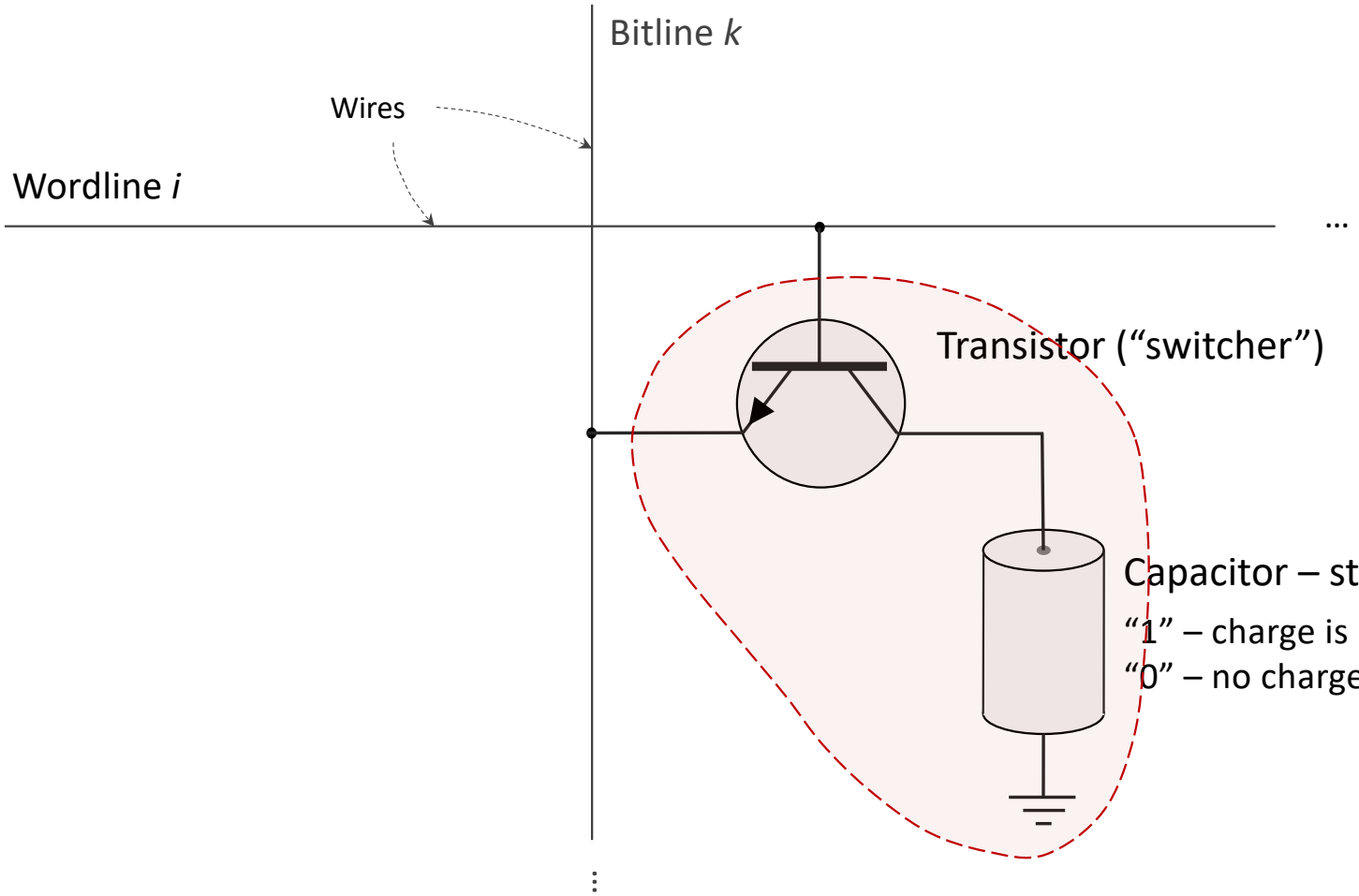
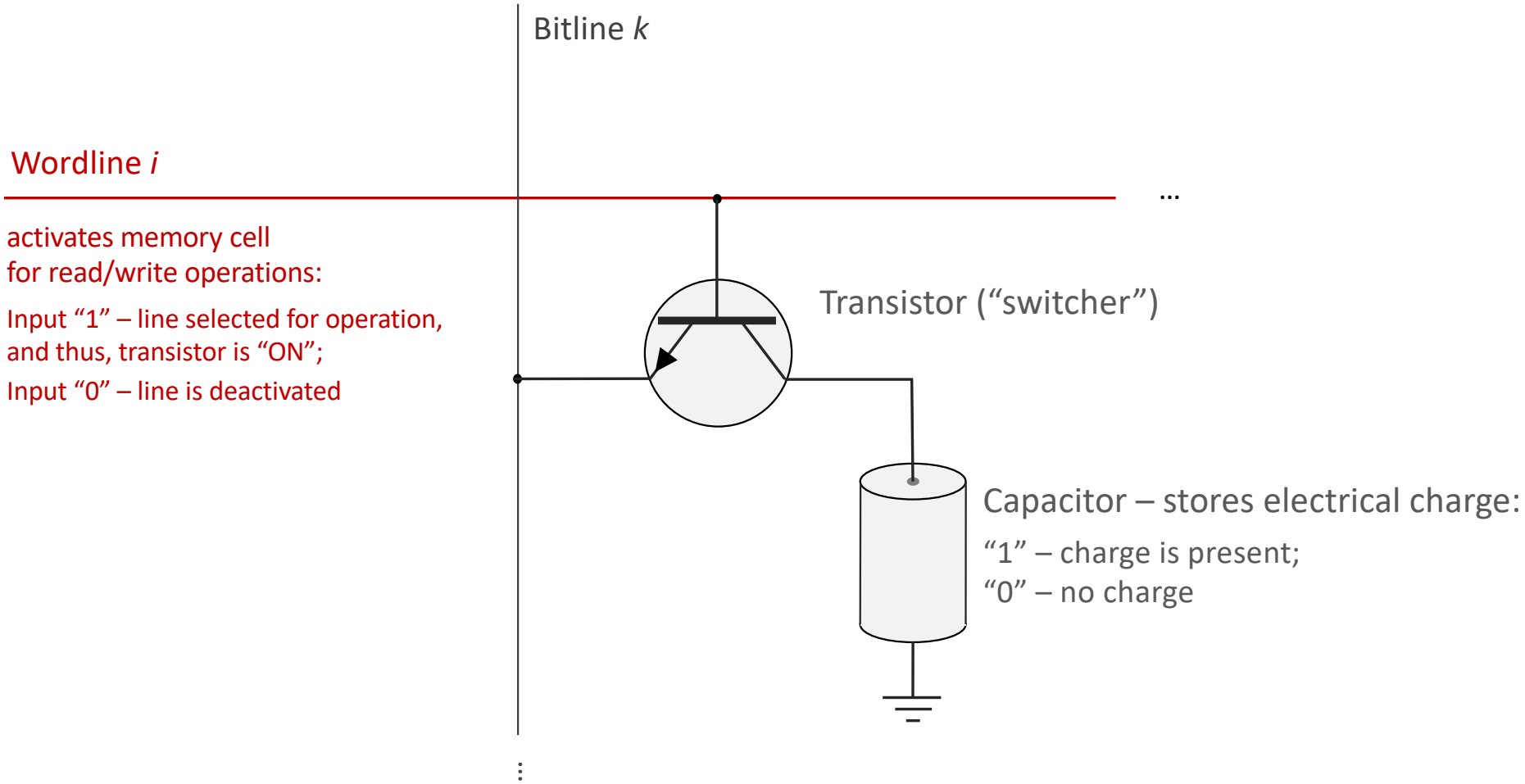



DRAM memory cell: capacitor + transistor

# DRAM memory cell



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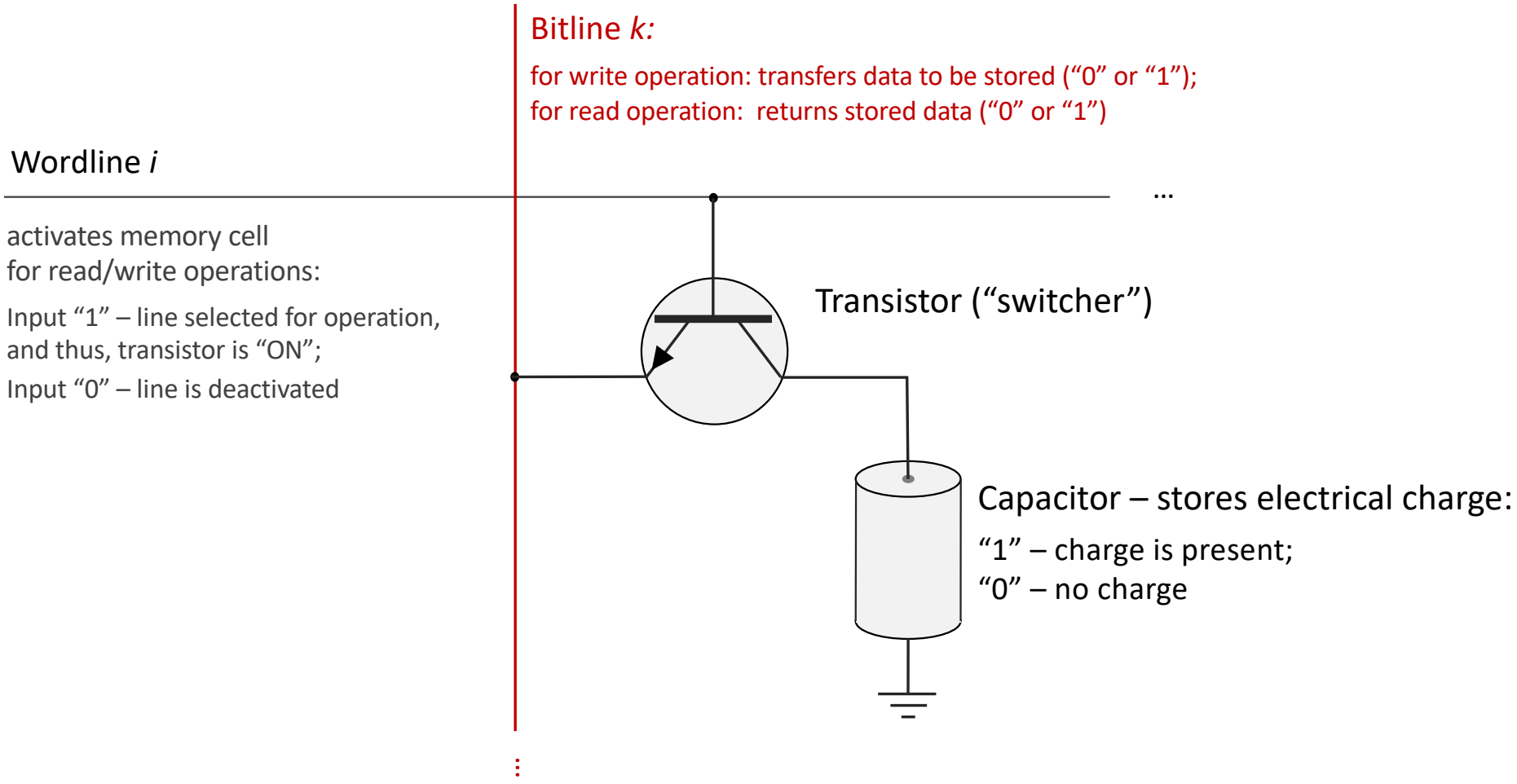

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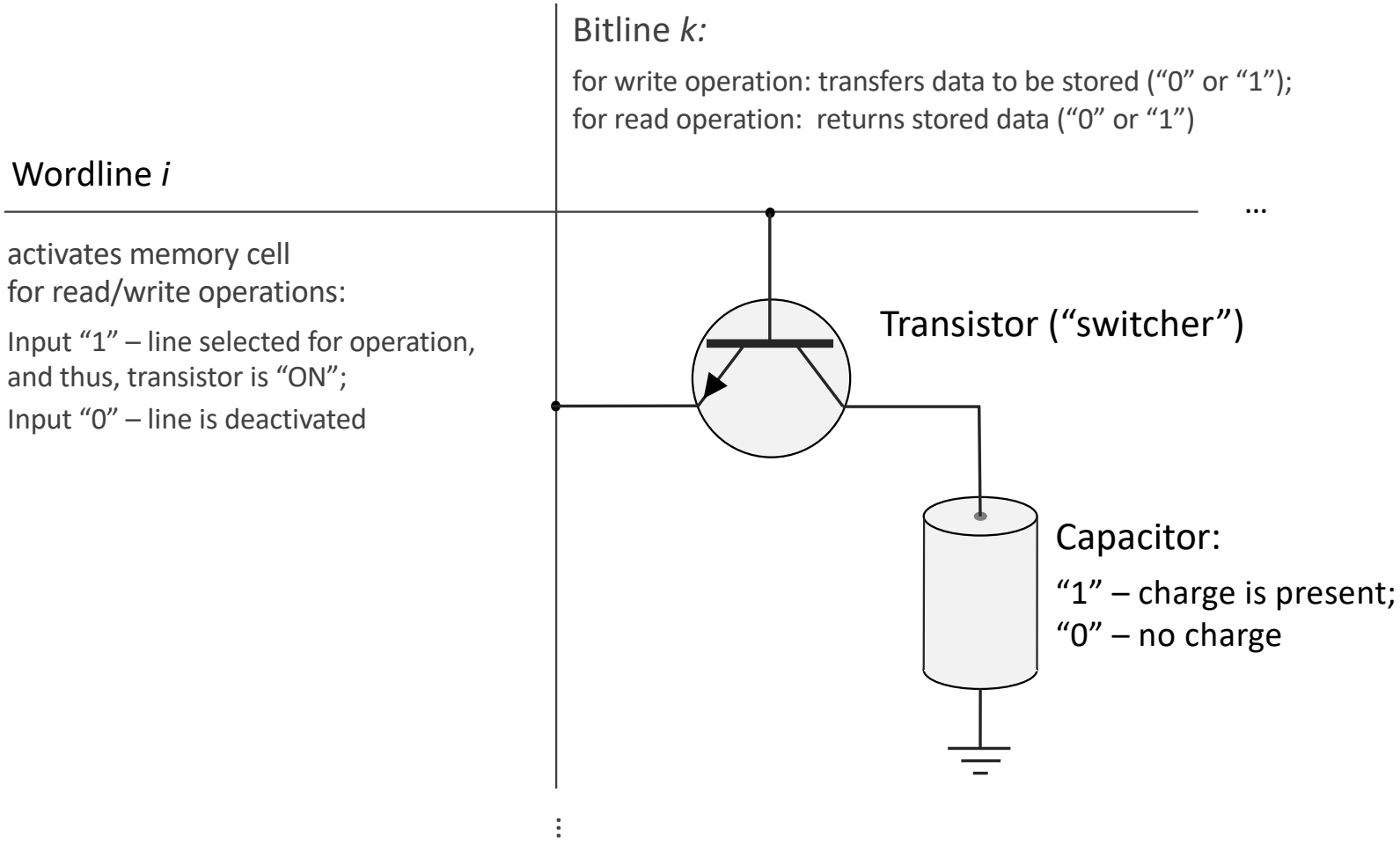
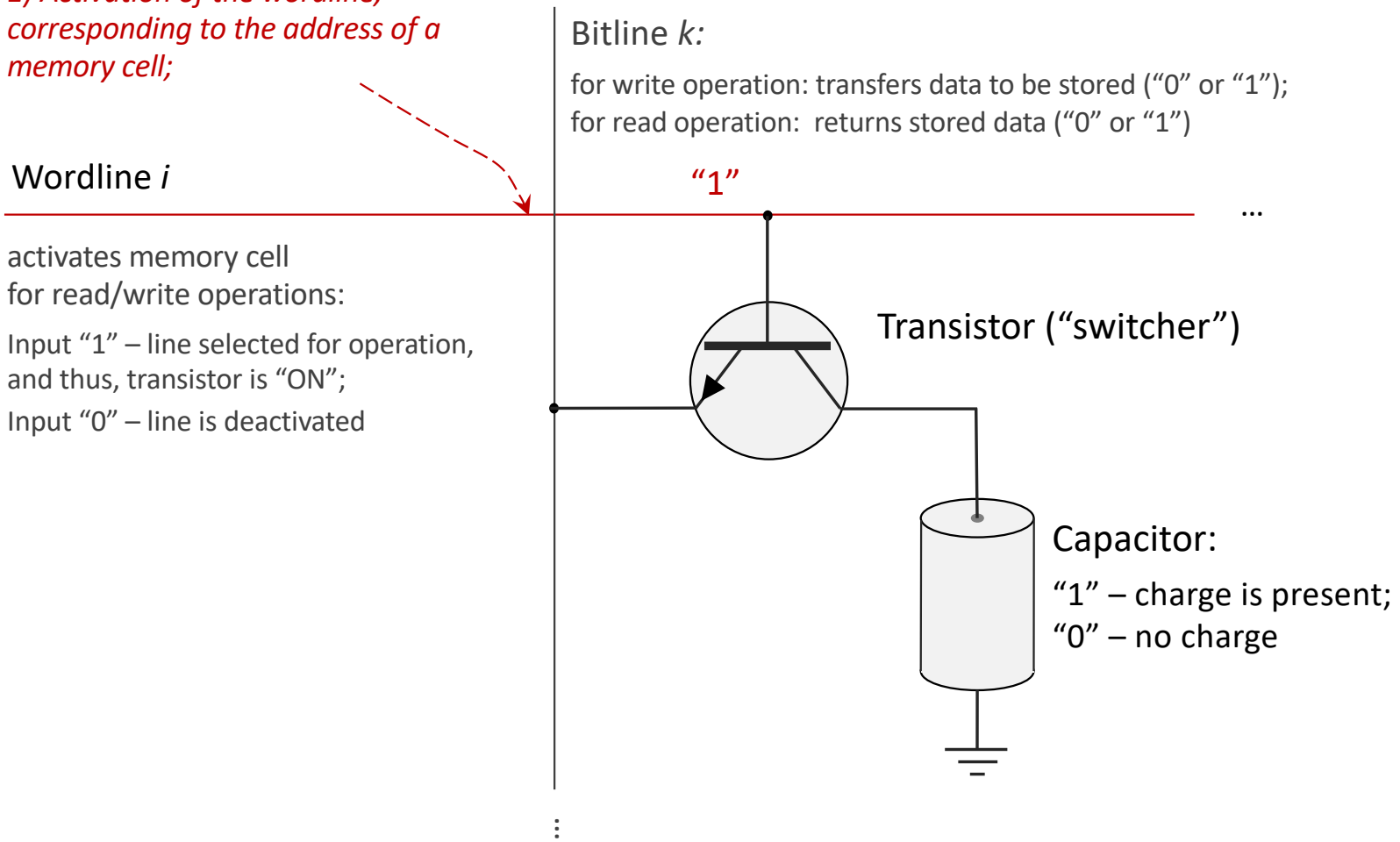


# Writing into DRAM memory cell

*1) Activation of the wordline, corresponding to the address of a memory cell;*



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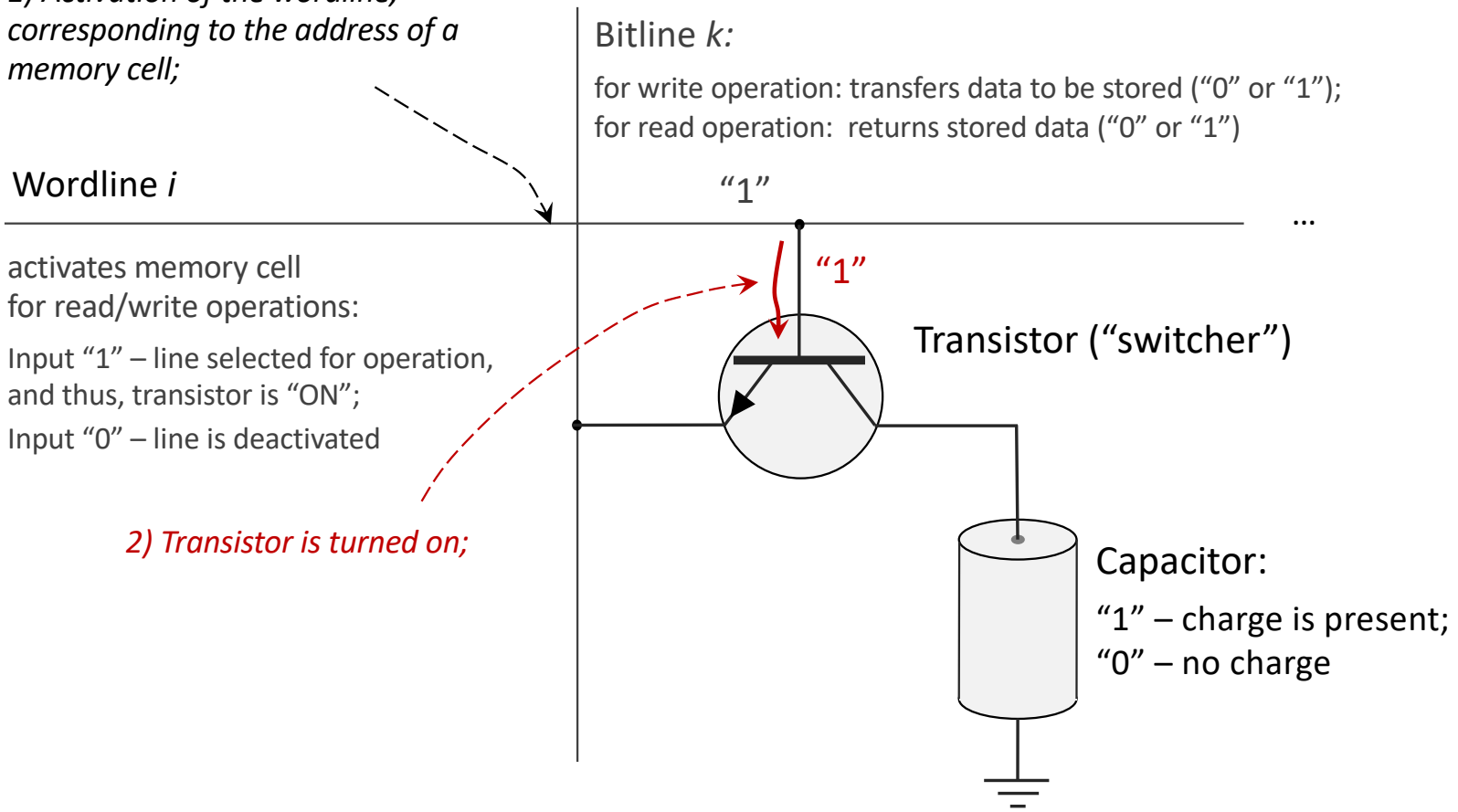

# Writing into DRAM memory cell

*1) Activation of the wordline, corresponding to the address of a memory cell;*

Bitline *k:*

for write operation: transfers data to be stored (“0” or “1”);
for read operation: returns stored data (“0” or “1”)

Wordline *i*

“1”

…

activates memory cell
for read/write operations:

Input “1” – line selected for operation, and thus, transistor is “ON”;

Input “0” – line is deactivated

“1”

Transistor (“switcher”)

“1”

*2) Transistor is turned on;*

“1”

Capacitor:

“1” – charge is present;
“0” – no charge

*3) Transfering data bit over the bitline, to be stored;*

*If “1” – capacitor gets charged (however, some time for charging is needed)*

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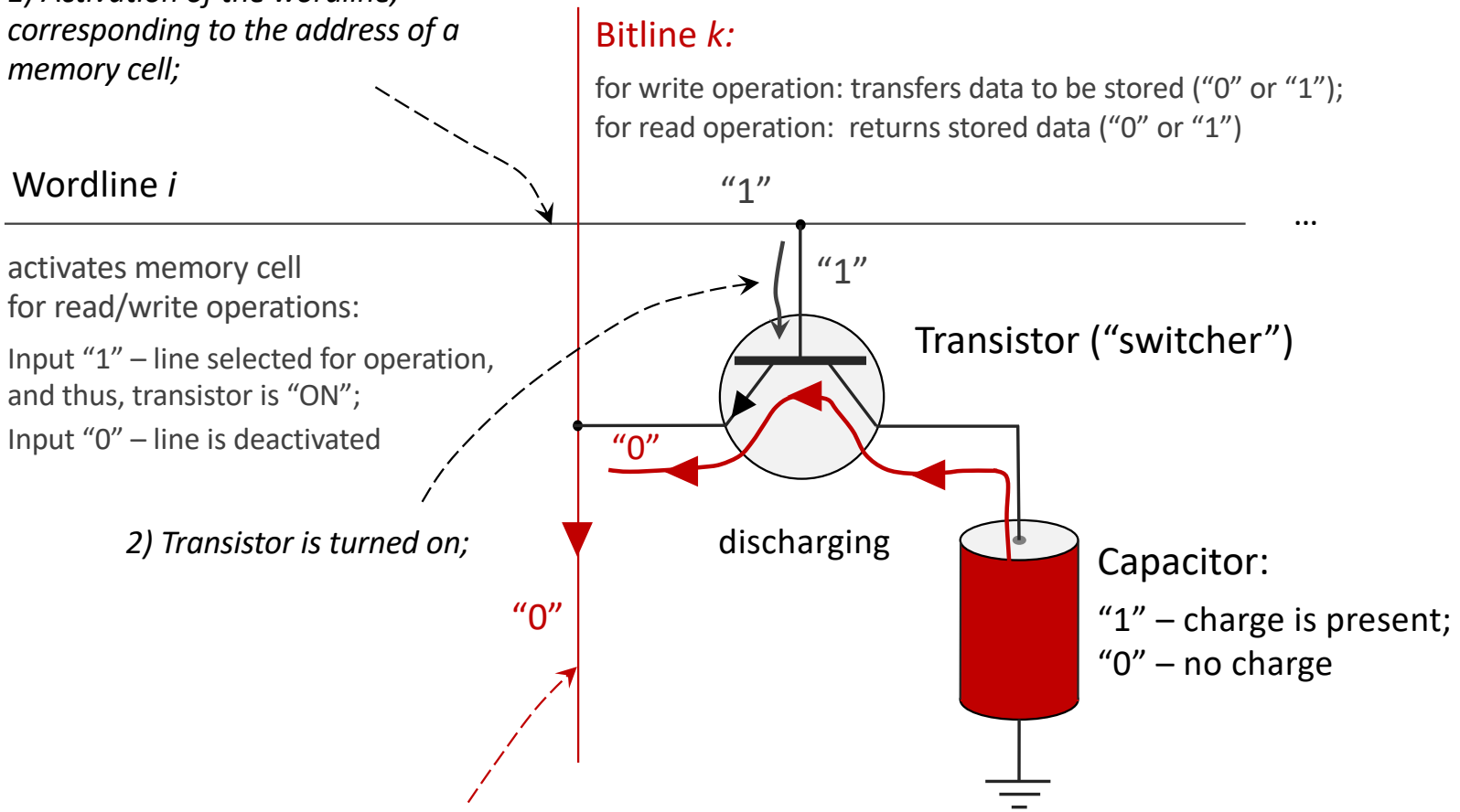


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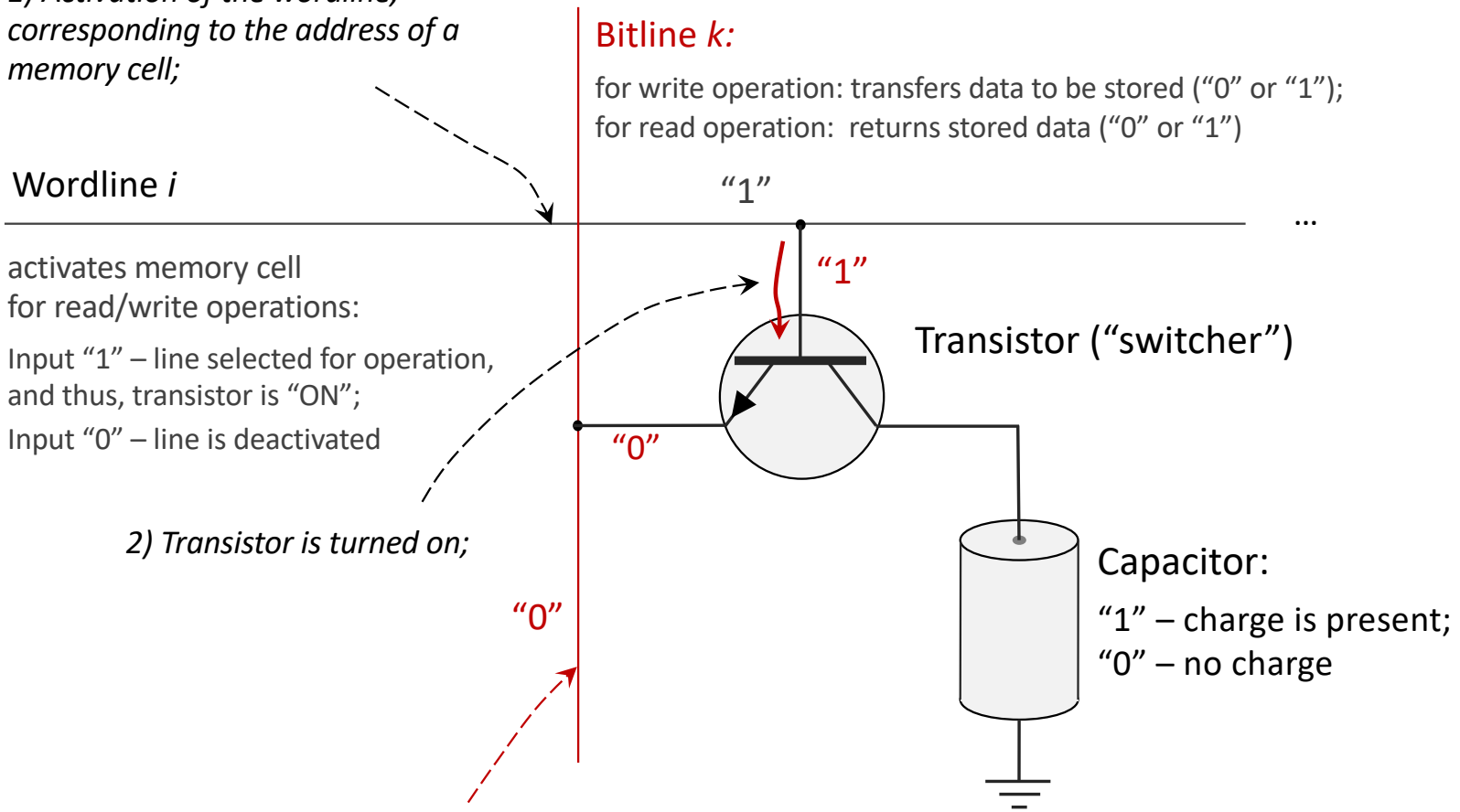


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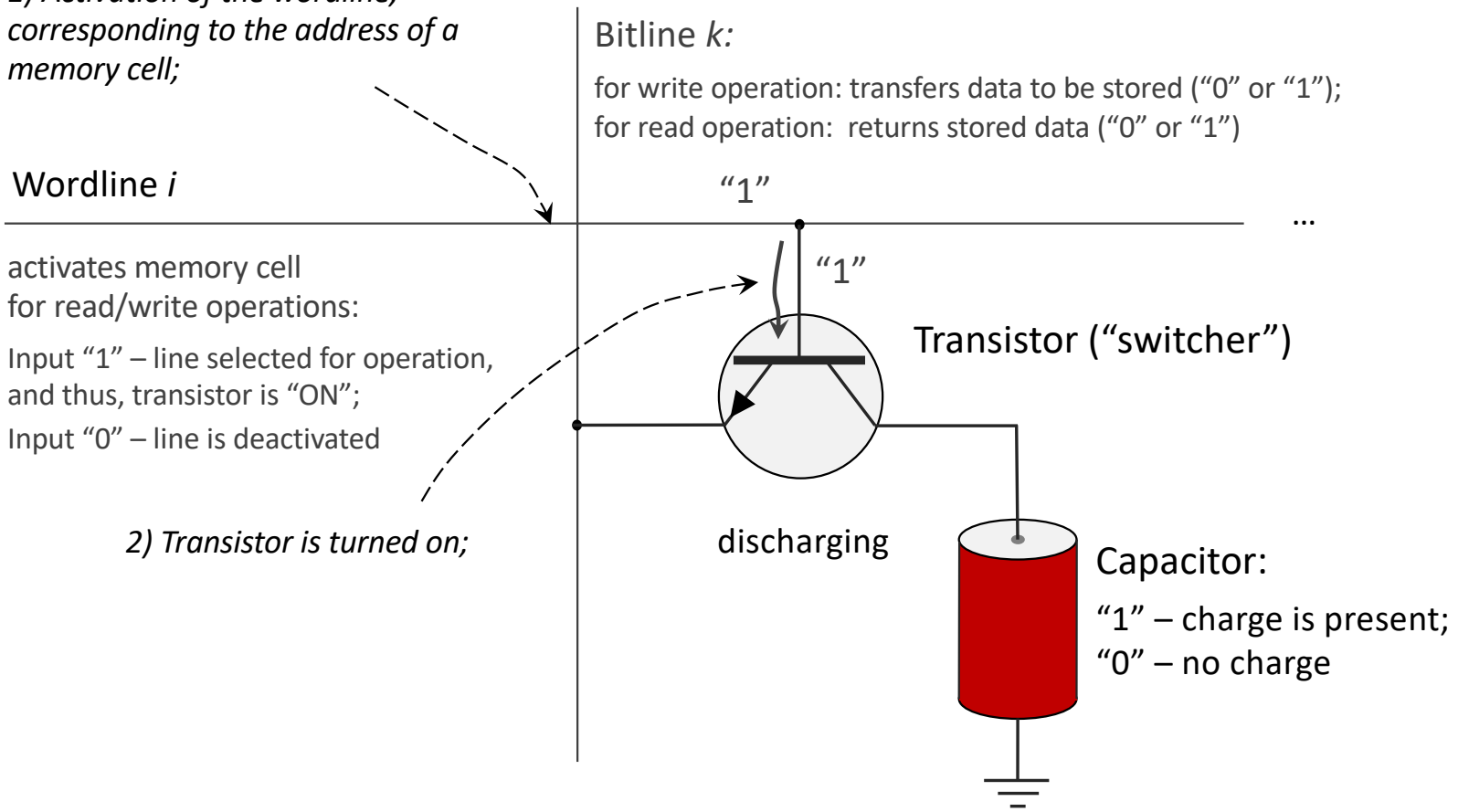

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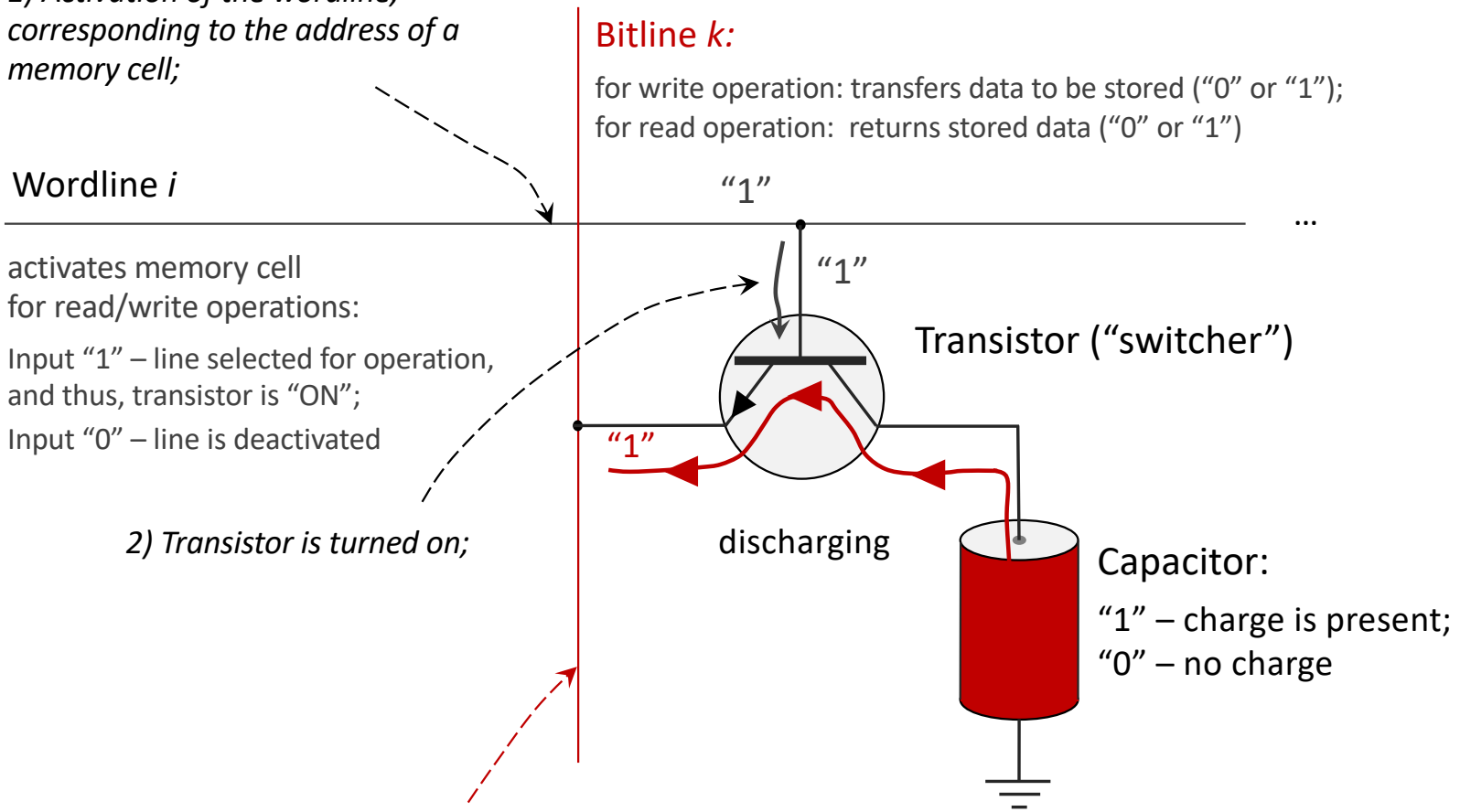
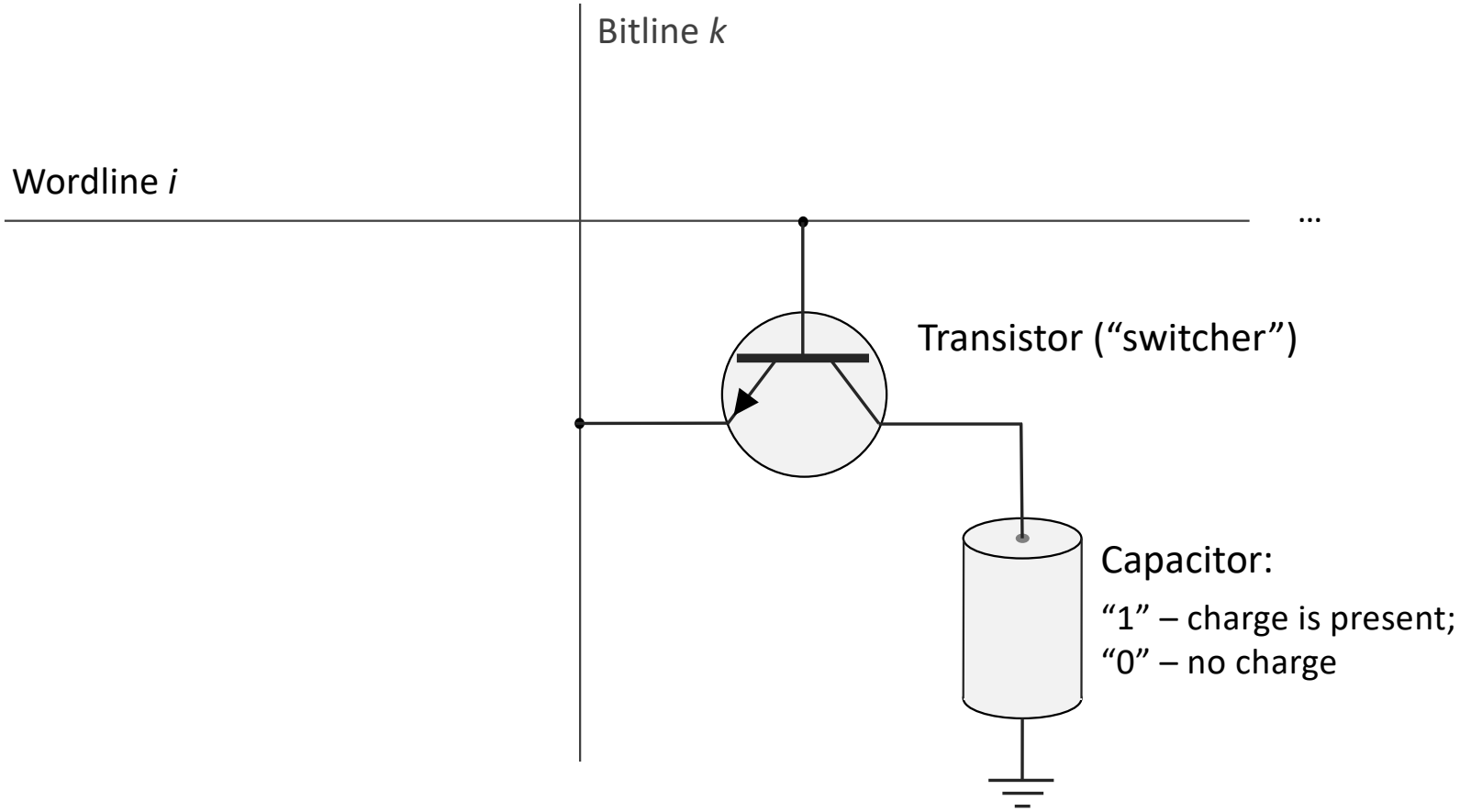



*3) Transfering data bit from capacitor over the bitline*

# A More Compact Graphical Notation for Electrical Circuits



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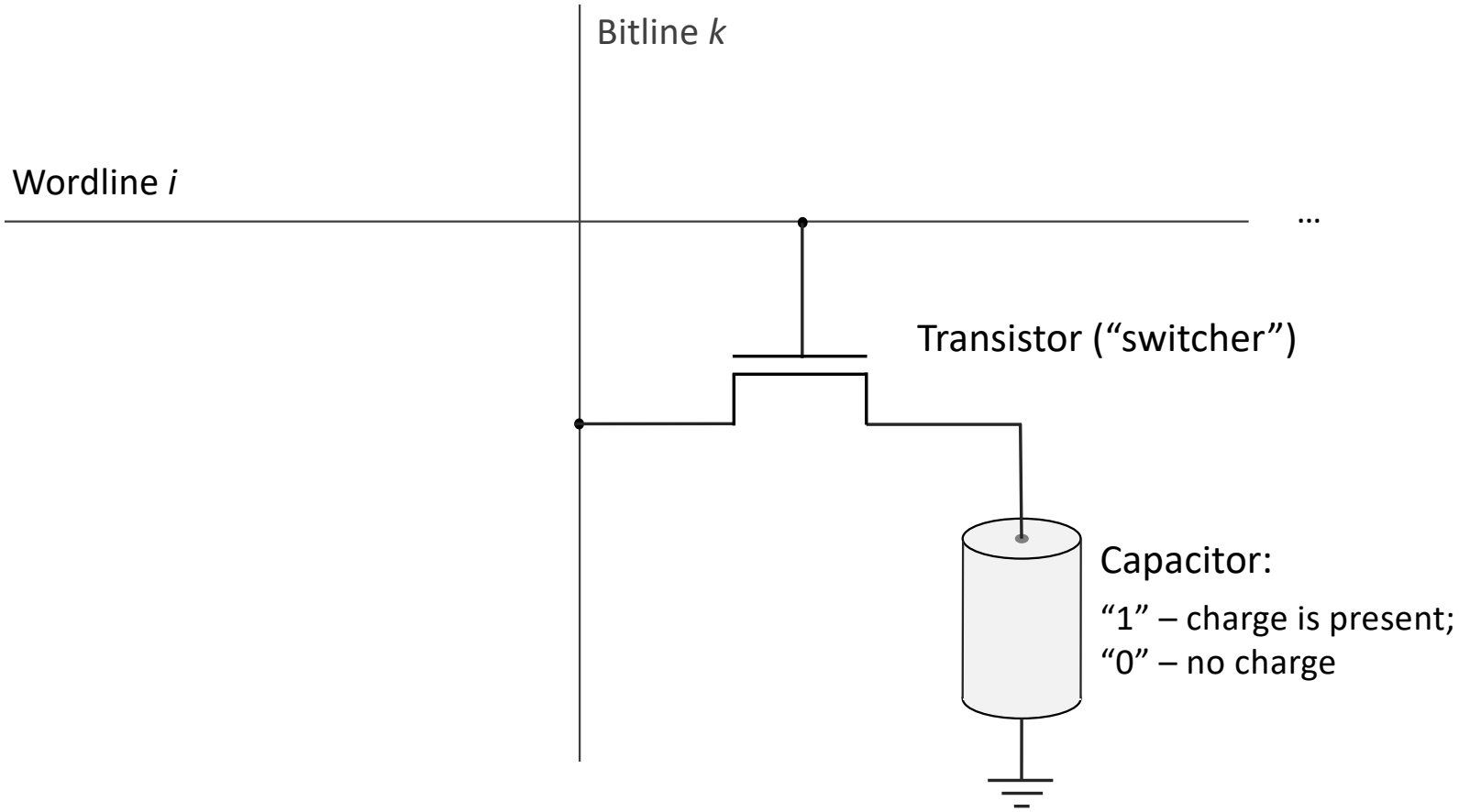

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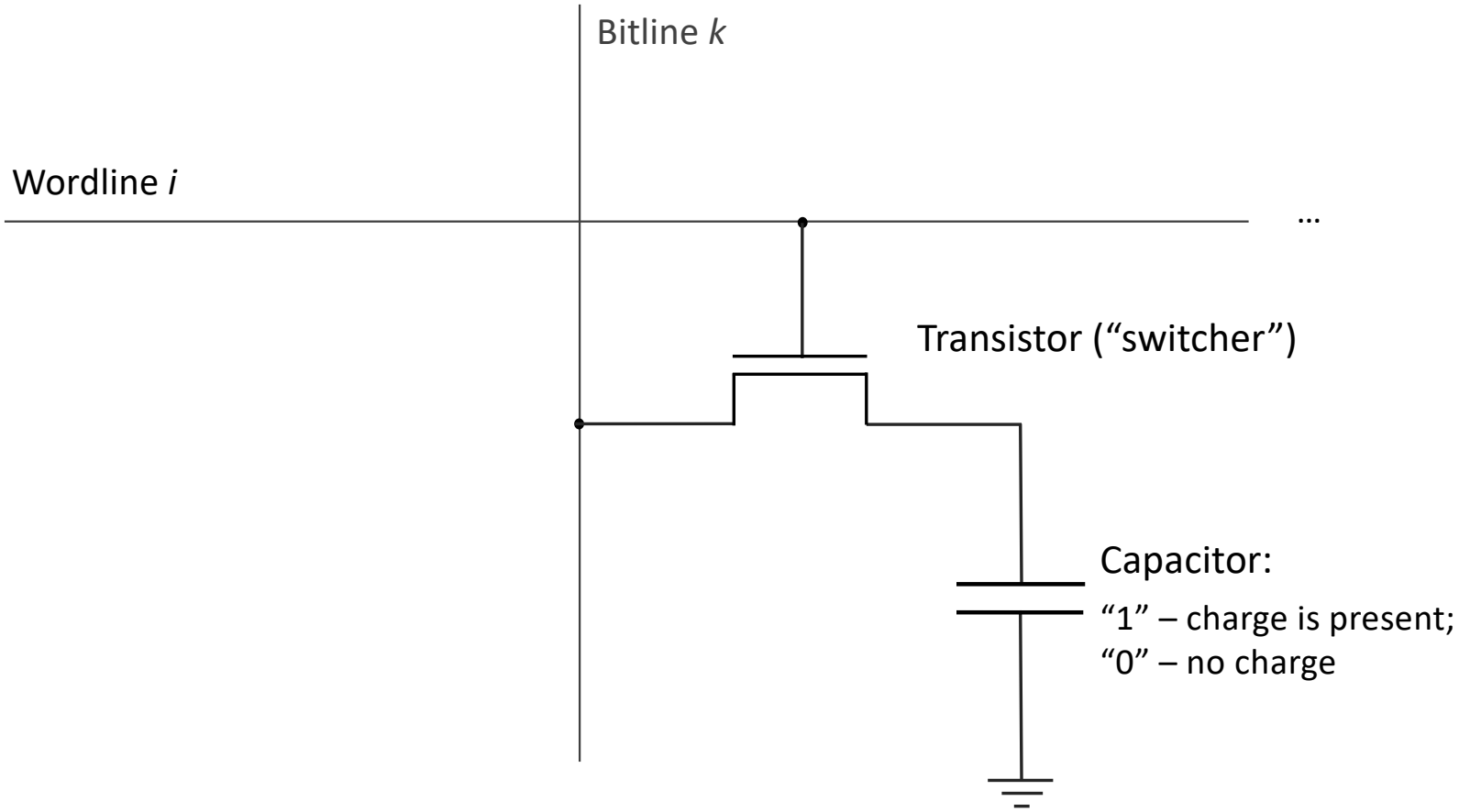
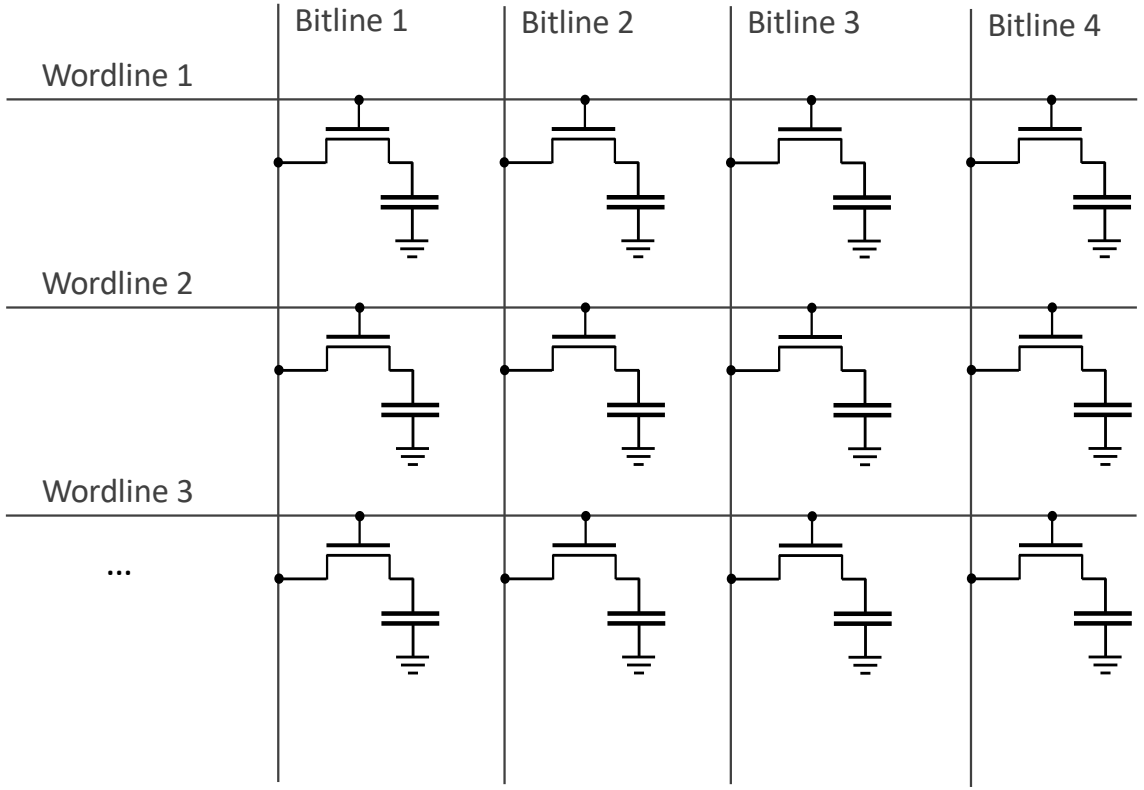


# DRAM Memory: the Work Principle

DRAM memory – a set of memory cells
(each cell contains 1 bit of data)



# DRAM Memory: the Work Principle

DRAM memory – a set of memory cells
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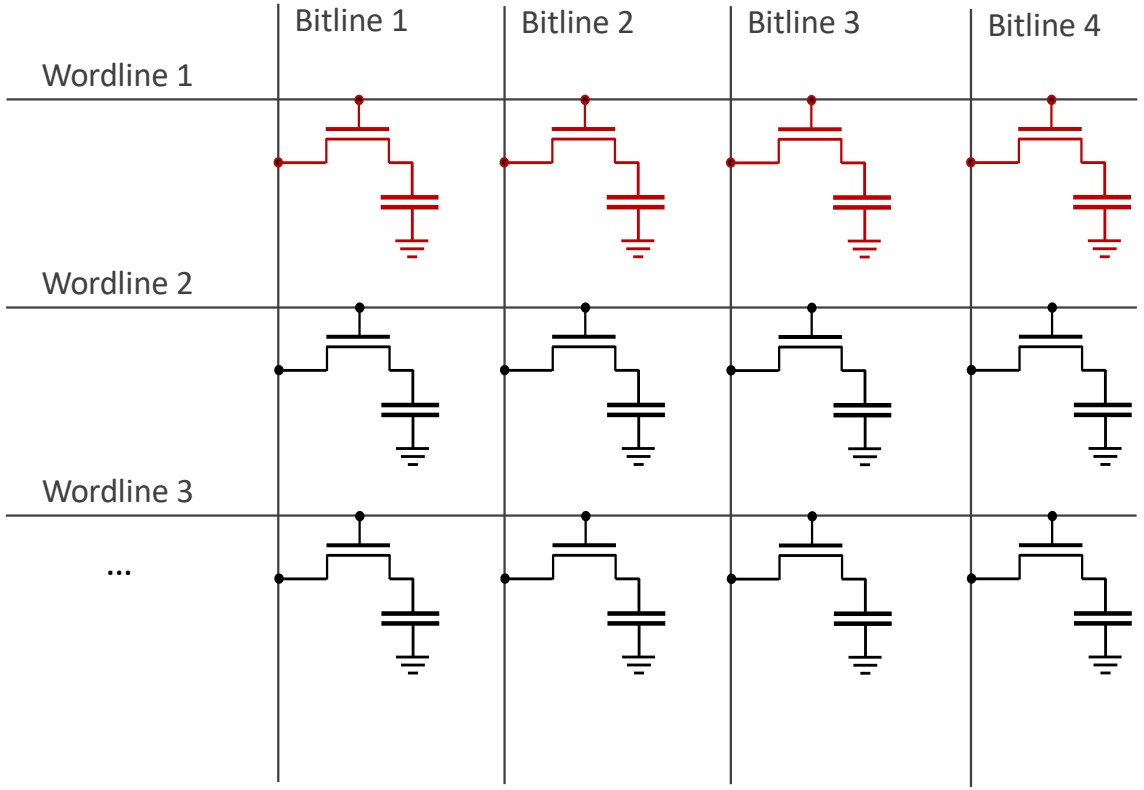
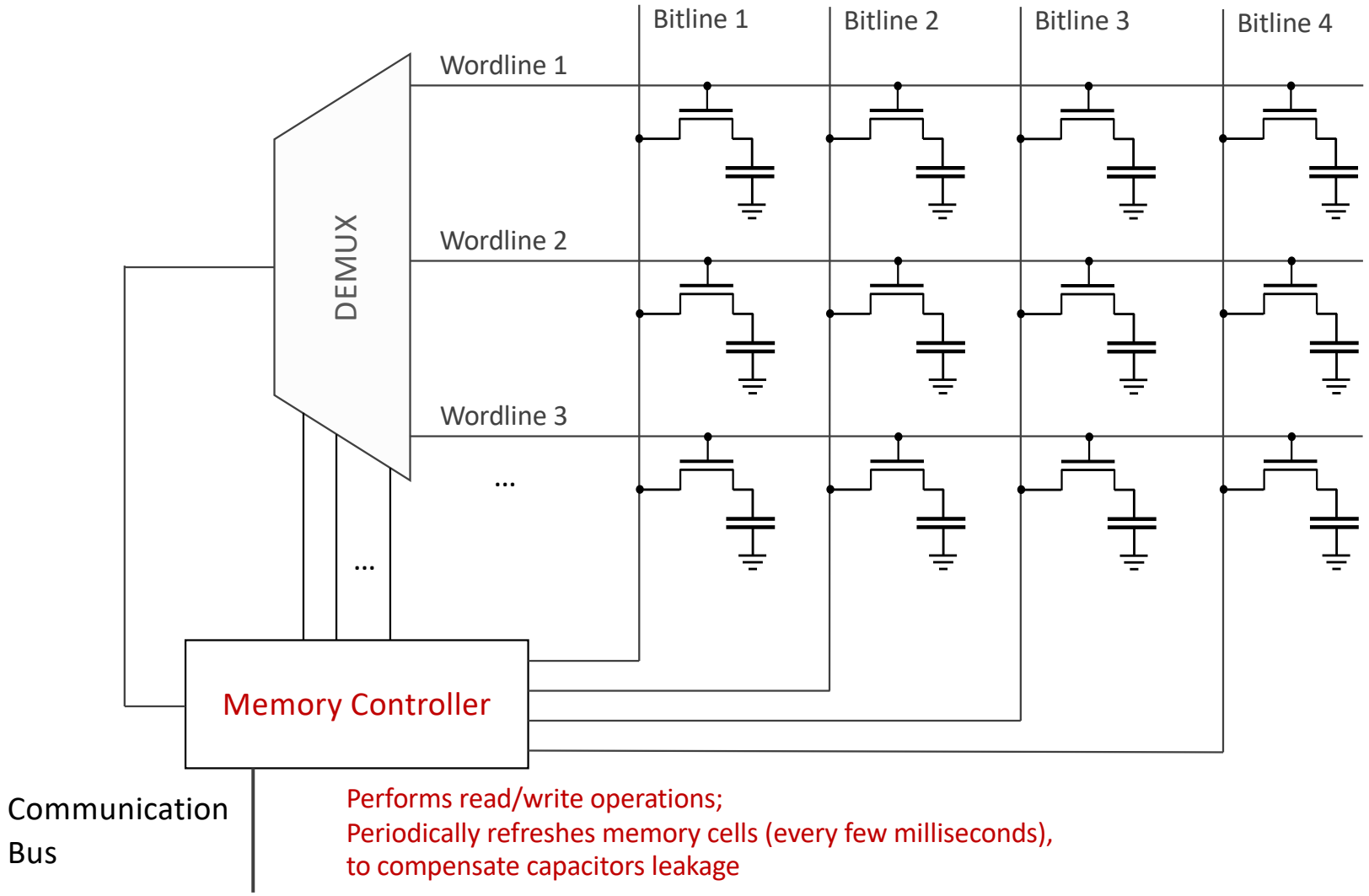
Several memory cells are connected to the same wordline



# DRAM Memory: the Work Principle

Memory controller operates with memory cells,
by using demultiplexors, encoders, etc.




Performs read/write operations;
Periodically refreshes memory cells (every few milliseconds),
to compensate capacitors leakage

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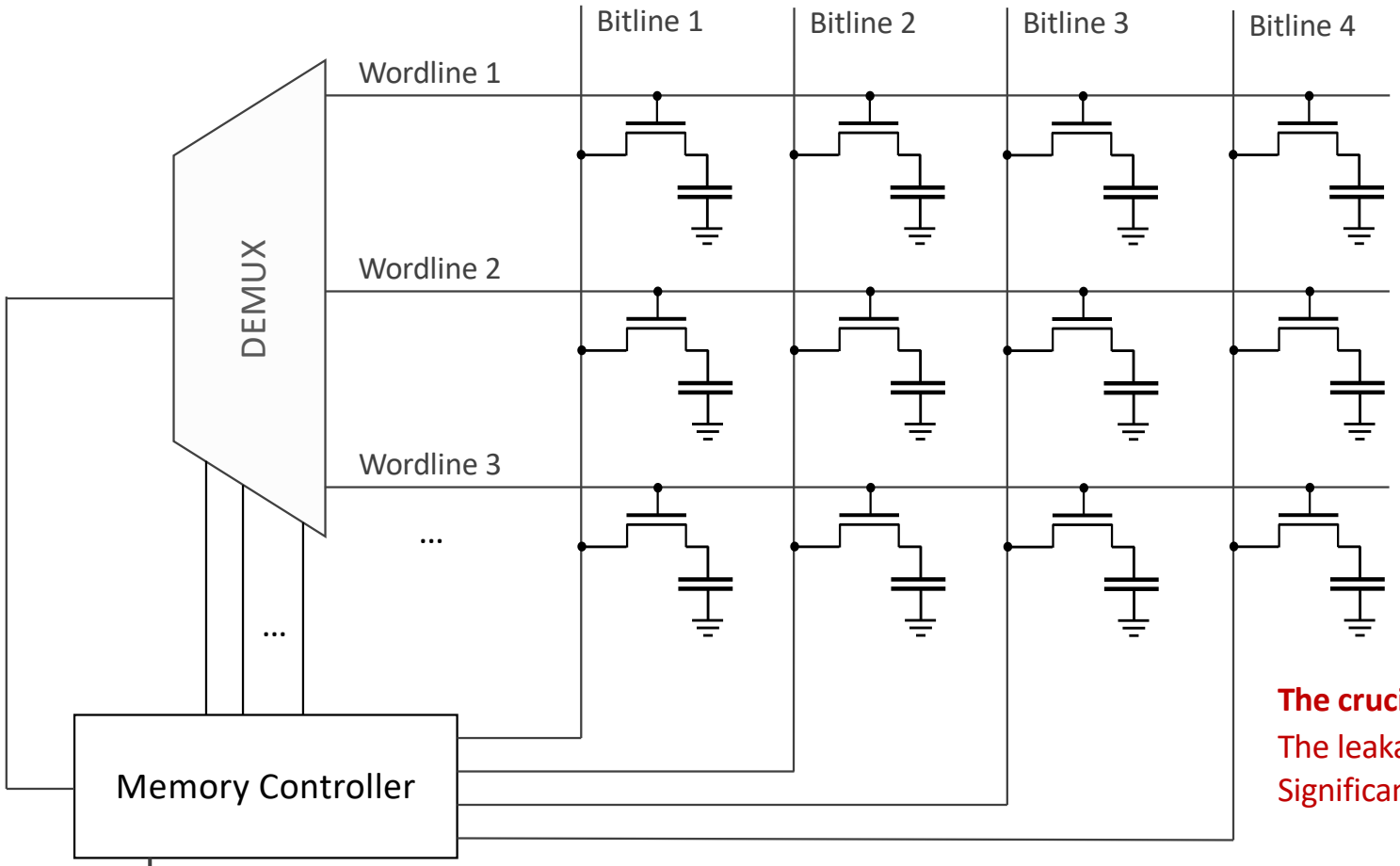


**The crucial problems:**

The leakage of capacitors;

Significant time needed for charging

Communication Bus

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Periodically refreshes memory cells (every few milliseconds), to compensate capacitors leakage

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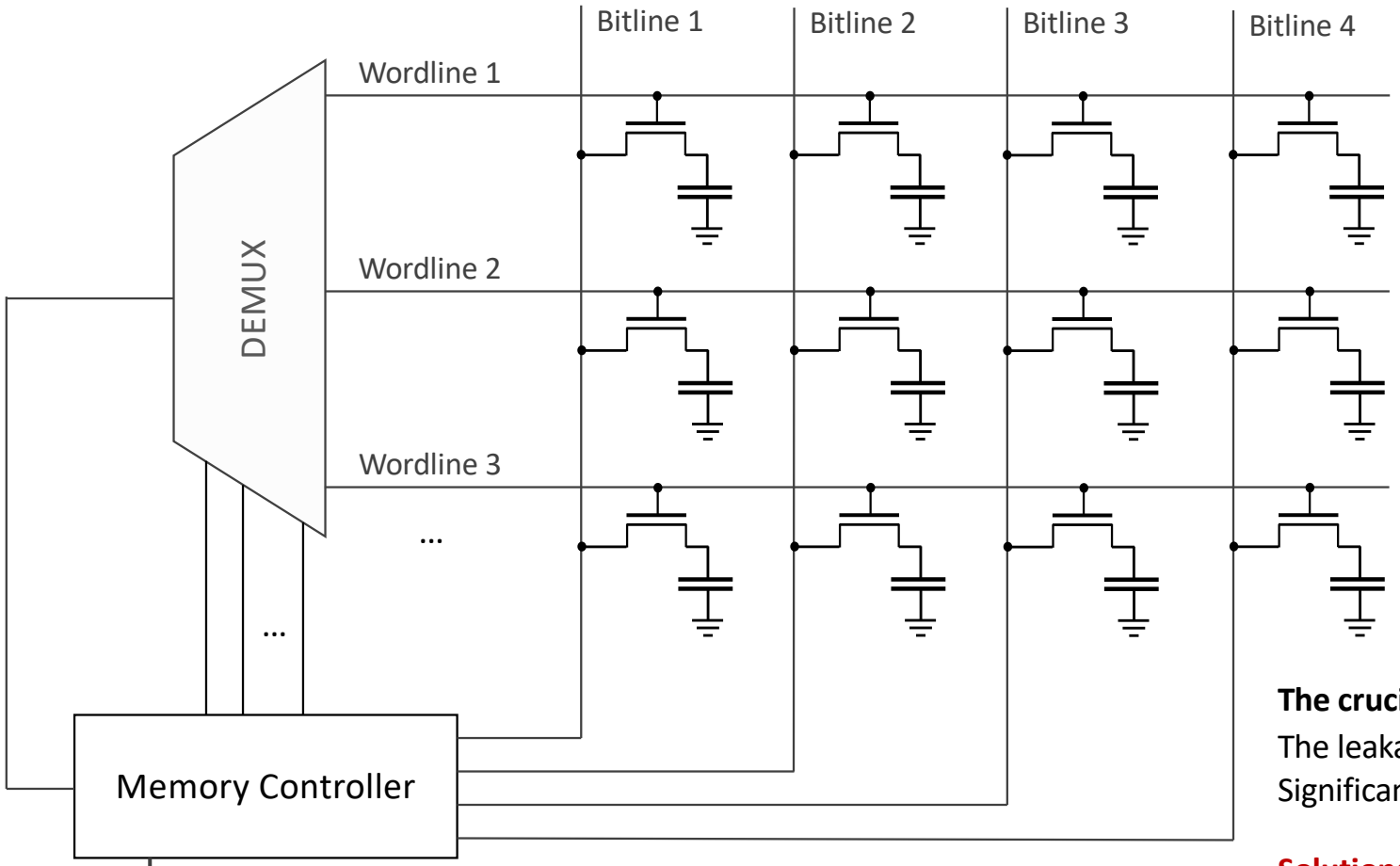



Performs read/write operations;
Periodically refreshes memory cells (every few milliseconds), to compensate capacitors leakage

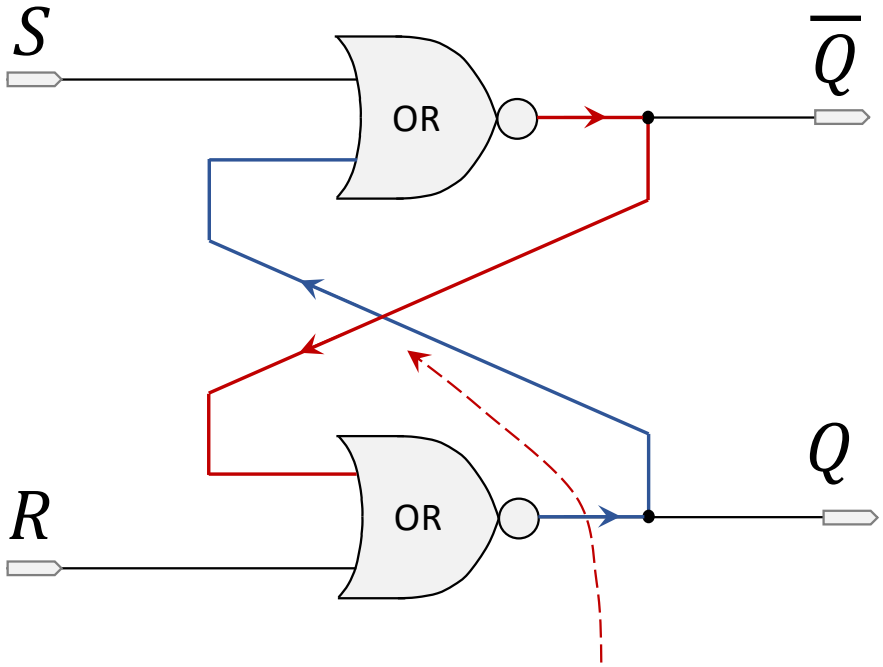
**The crucial problems:**

The leakage of capacitors;
Significant time needed for charging

**Solution:**

To use SRAM,
which relies on latches and flip-flops
(different from capacitors)

# Latch: an electronic circuit to store one bit of information

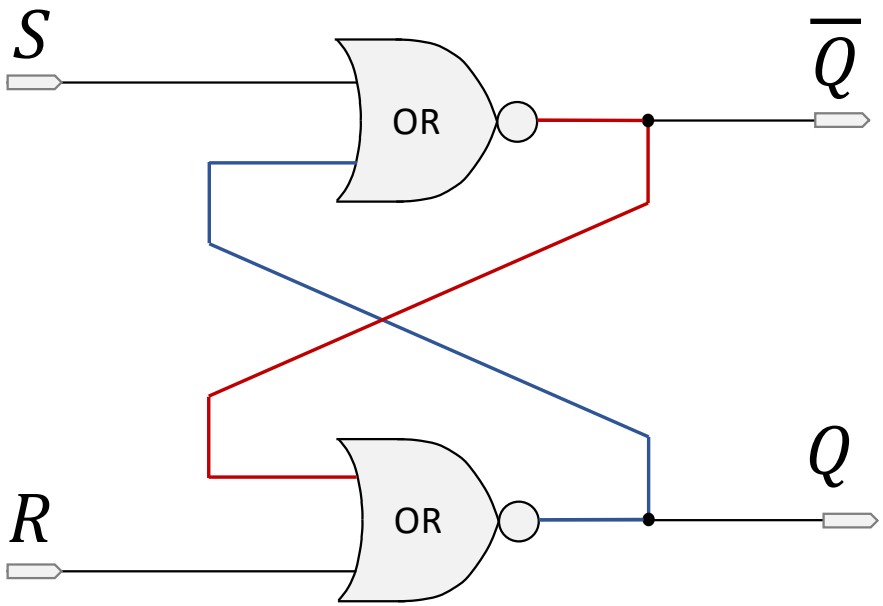



| S | R | Q |
|---|---|---|
| 1 | 0 | 1 |
| 0 | 1 | 0 |
| 0 | 0 | $Q^{\text{prev}}$ |
| 1 | 1 | Illegal inputs |

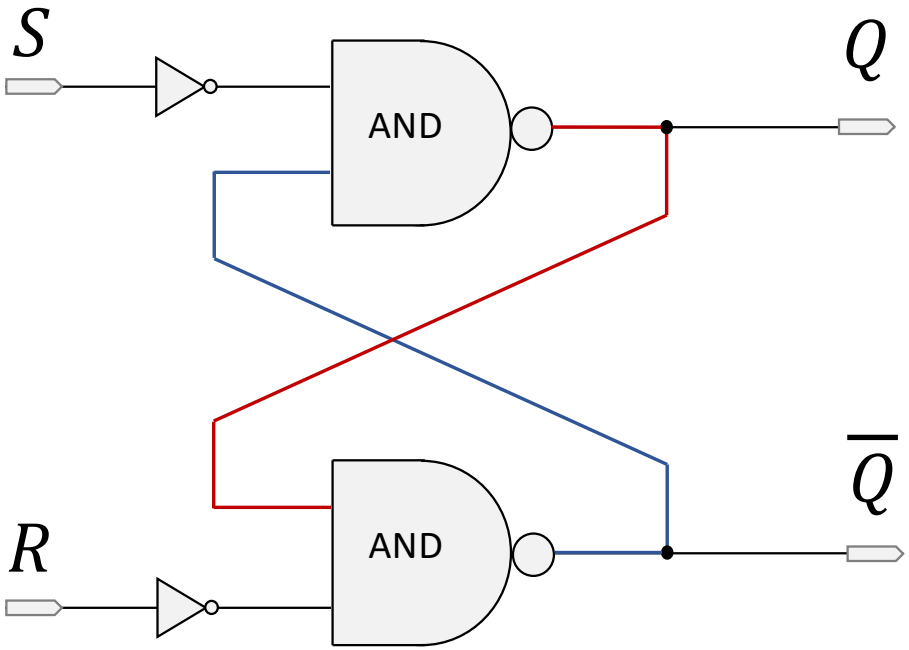
Cross-coupled connection of logic gates – the key feature of latches and flip-flops: the output signal of one gate serves as an input for another gate

# Latch: multiple logic implementations are available

1) Implementation by using NOR logic gates:

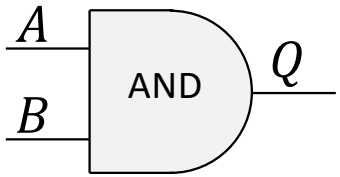



2) by using NAND logic gates:




**These representations are logical oversimplified representations, hiding many implementation details**

# Recap: Each logic gate is an electronic circuit, implemented by using transistors

<table>
<tr><th>Logic Gate</th><th>Symbolic Representation</th><th>Truth Table</th><th>Implementation with Transistors</th></tr>
<tr>
<td>AND</td>
<td> 
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<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td></tr>
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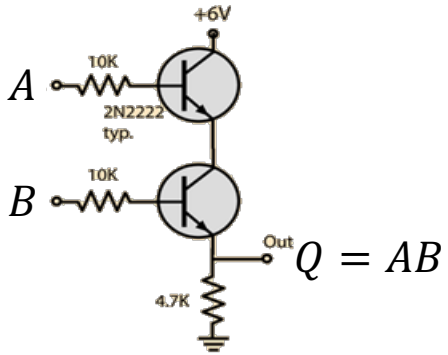
<td> 
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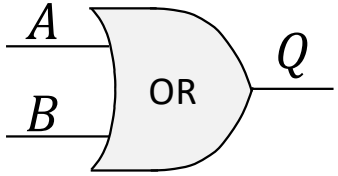
<td>OR</td>
<td> 
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<tr><th>A</th><th>B</th><th>Q=A+B</th></tr>
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<tr><td>1</td><td>0</td><td>1</td></tr>
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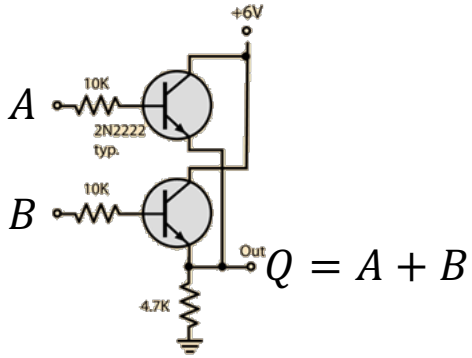
<td> 
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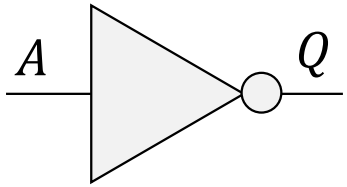
<td> 
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<tr><th>A</th><th>Q=A'</th></tr>
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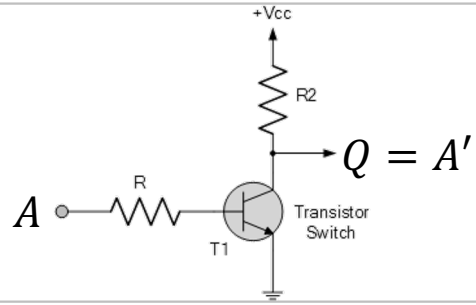
<td> 
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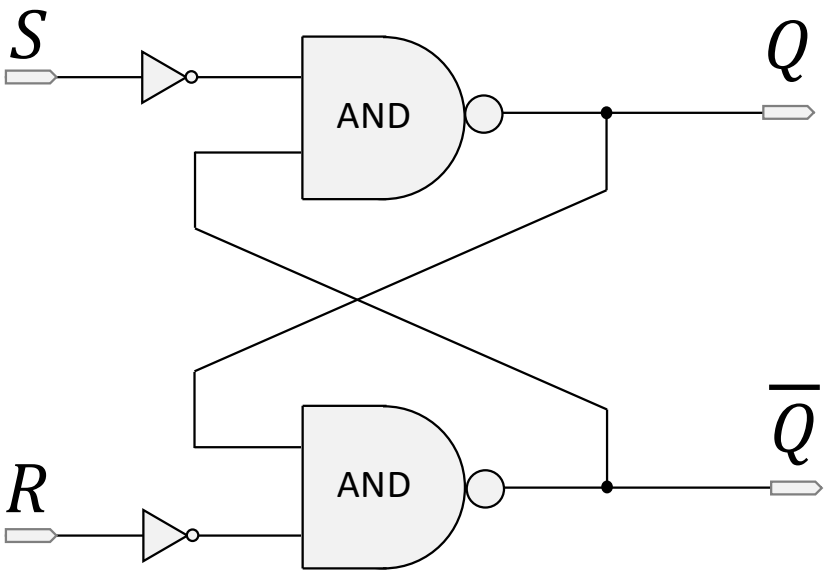
Transistor implementations are taken from http://hyperphysics.phy-astr.gsu.edu/hbase/Electronic/trangate.html#c1 and https://www.electronics-tutorials.ws/logic/logic_4.html

Latch Logical representation:




Electrical circuit implementation (one of many):

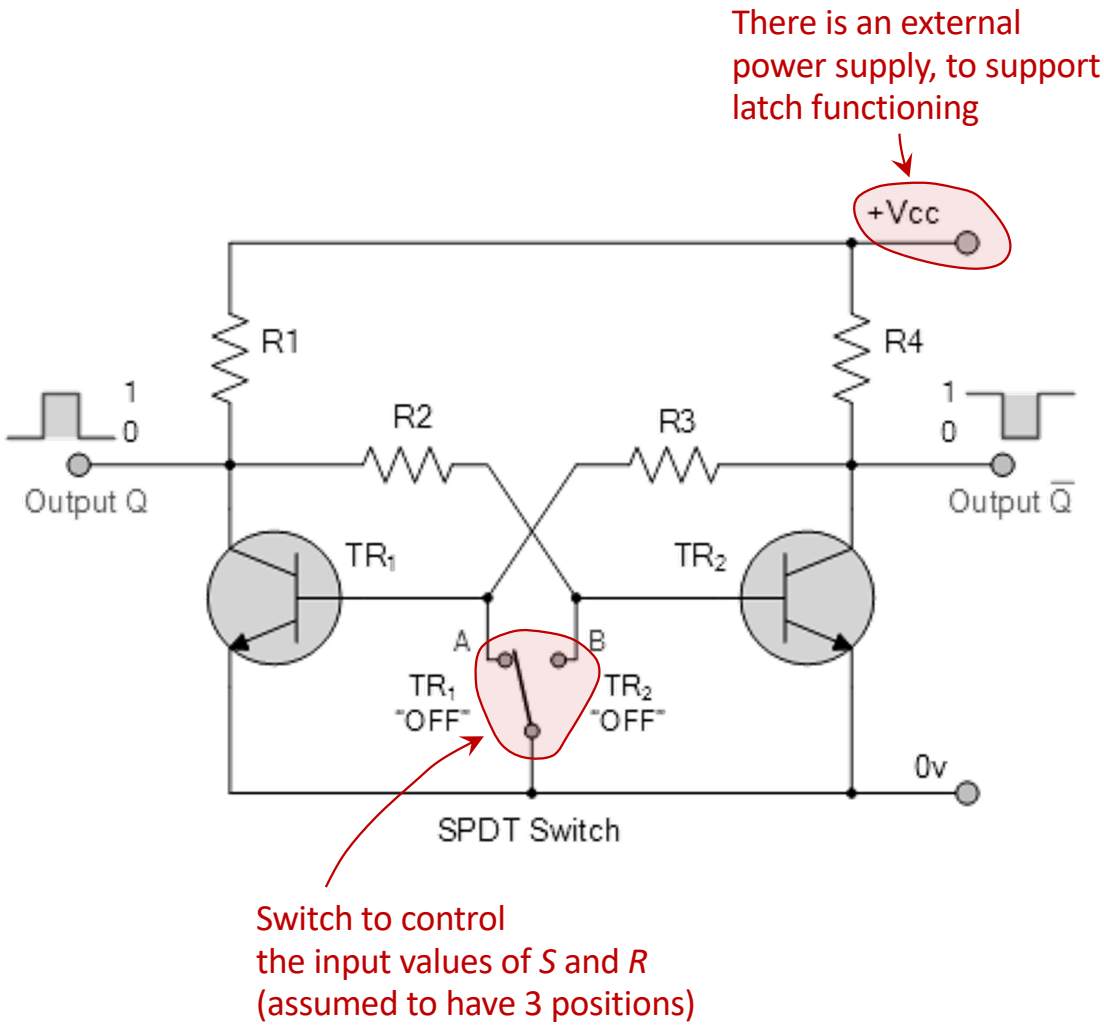



Image is taken from https://www.electronics-tutorials.ws/waveforms/bistable.html

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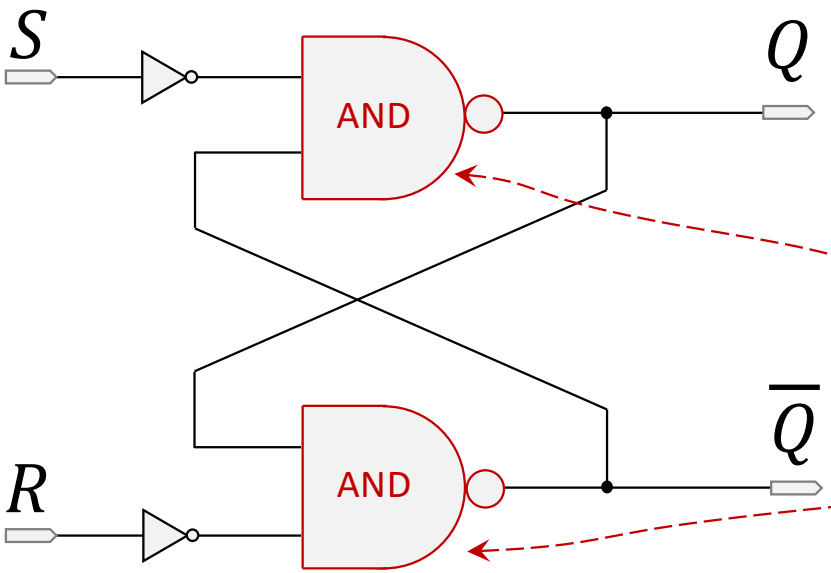


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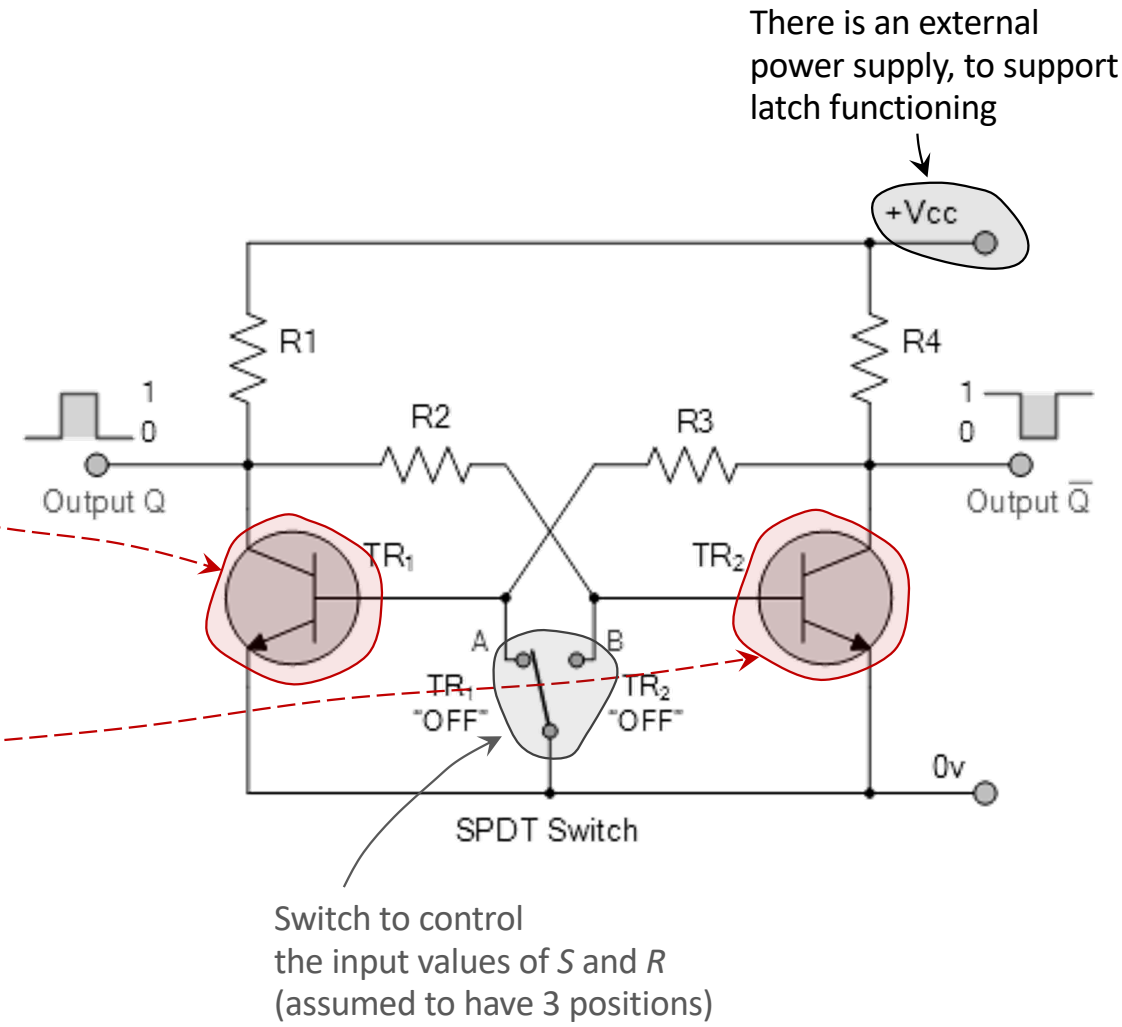

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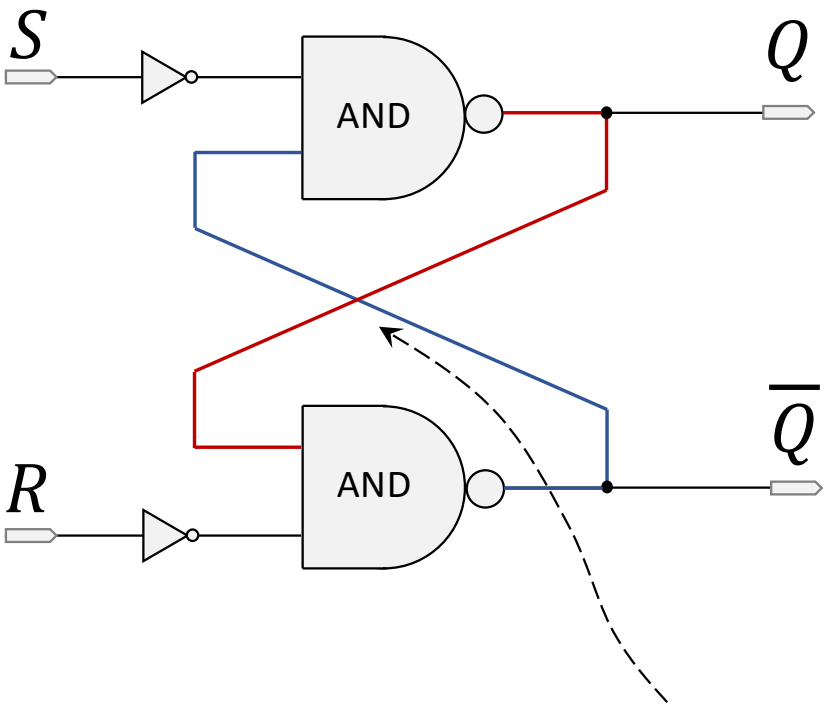


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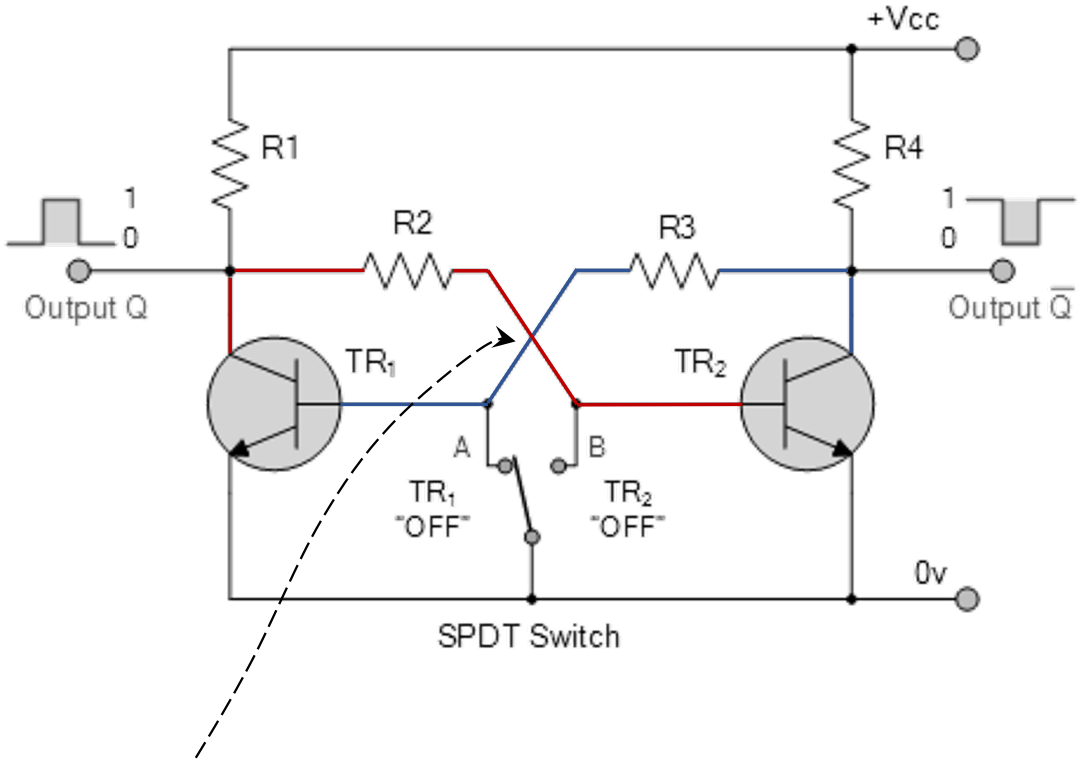
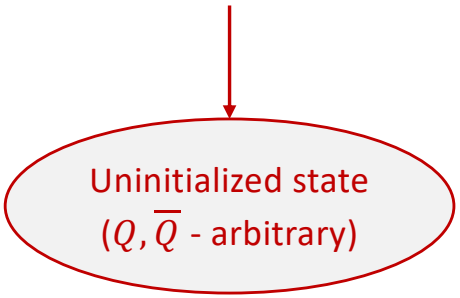
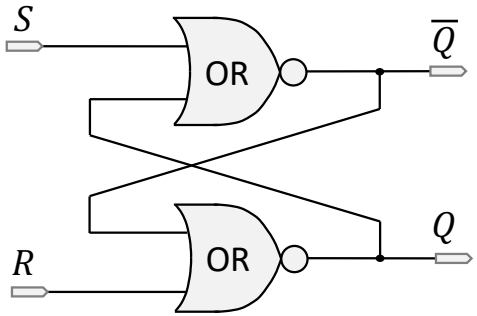


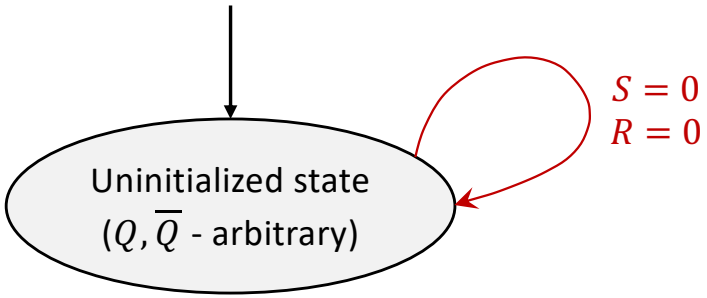

Cross-coupled connections between gates and corresponding transistors

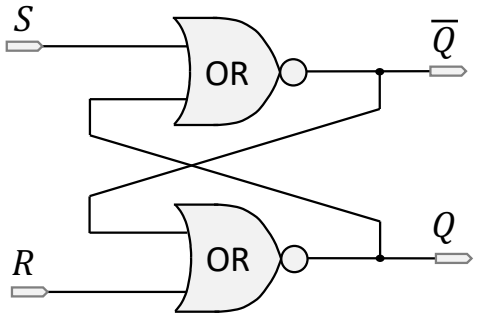
State-Transition Diagram for a Latch



State-Transition Diagram for a Latch



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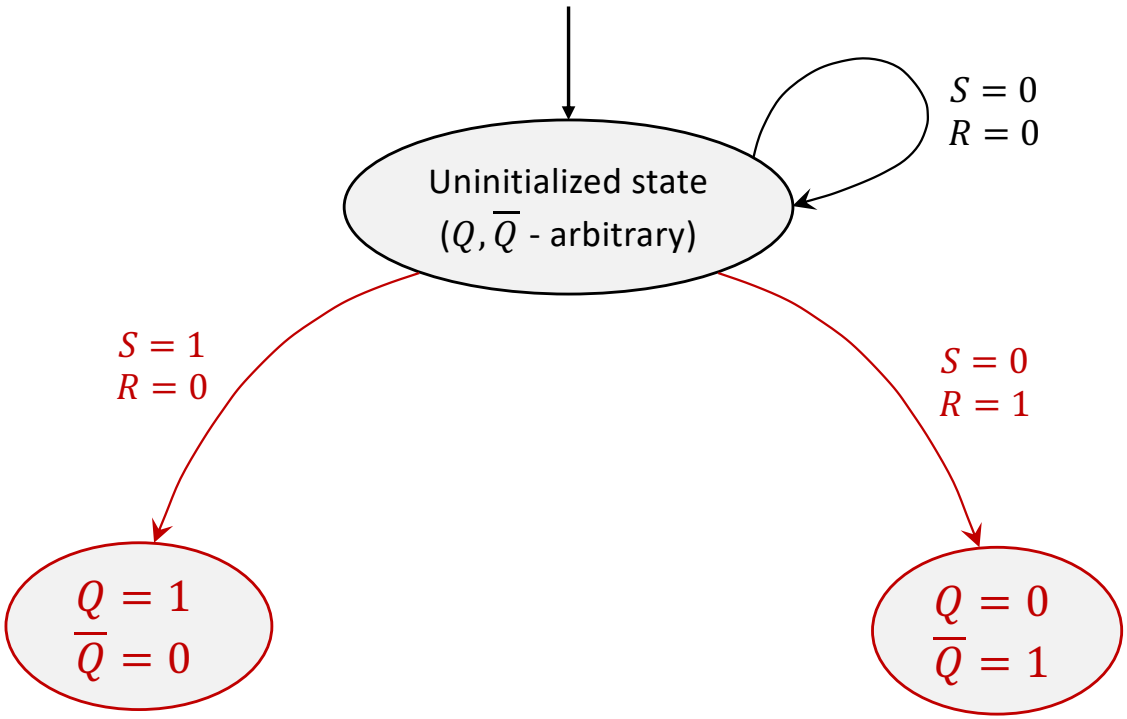


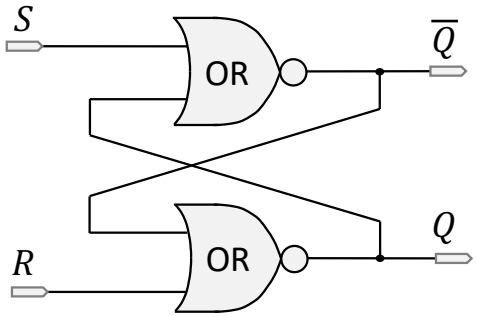

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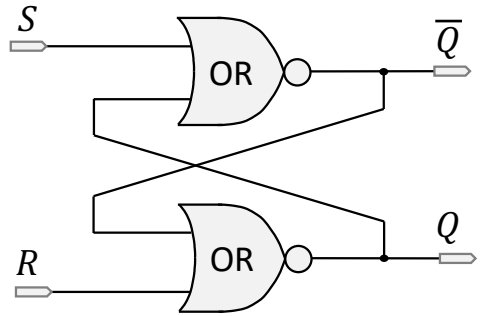


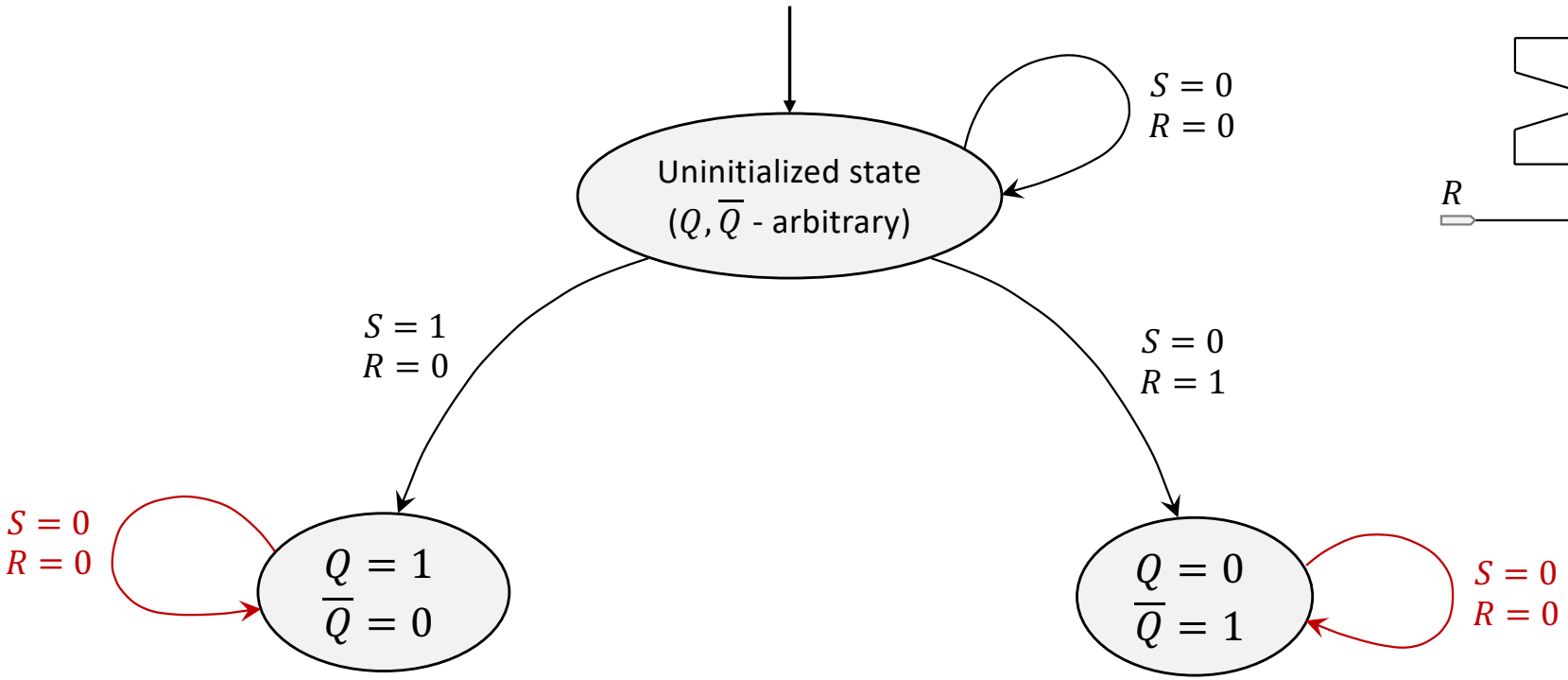

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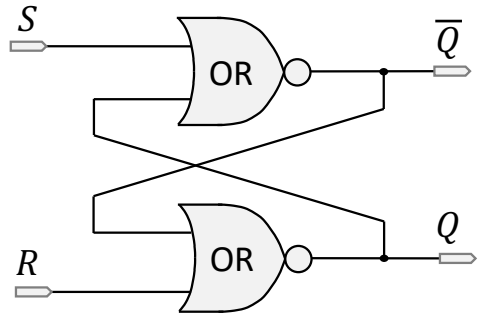


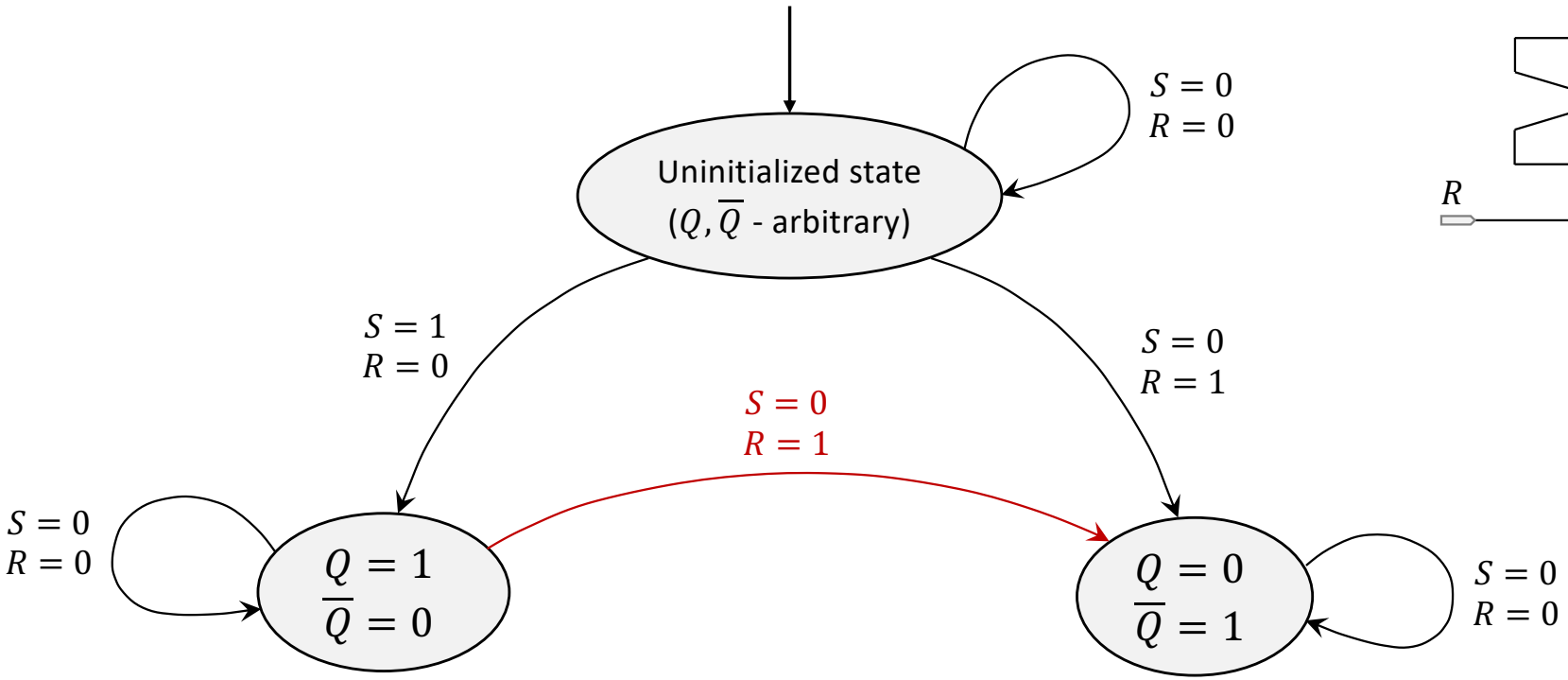

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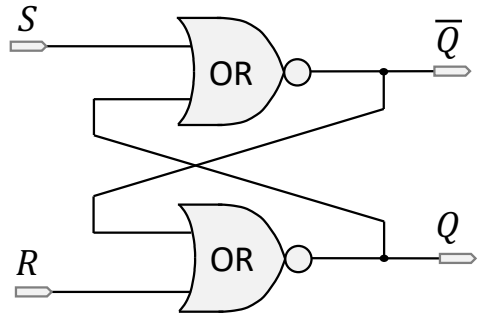


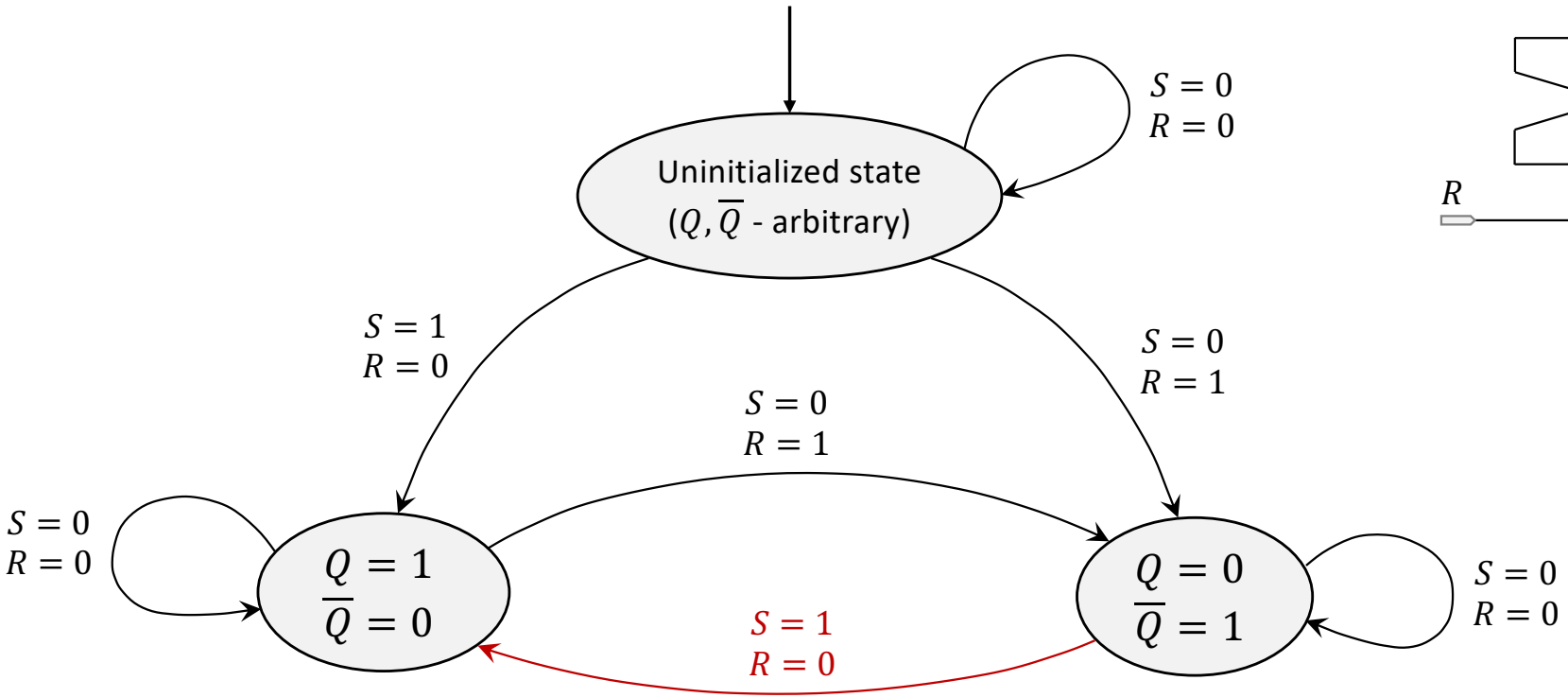

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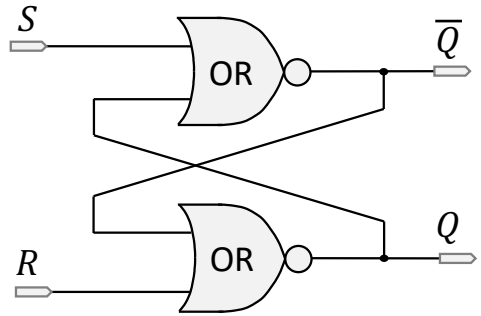


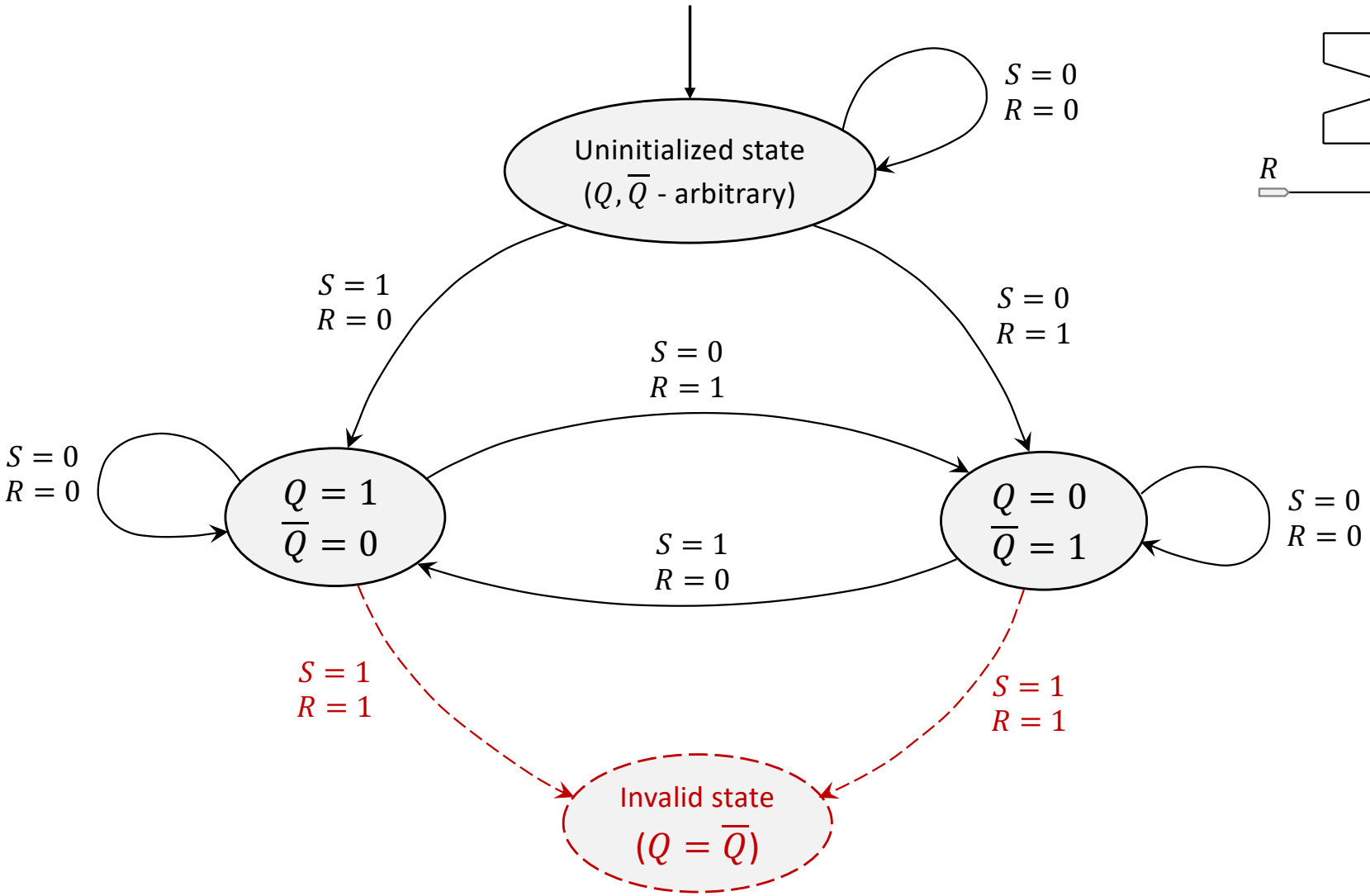

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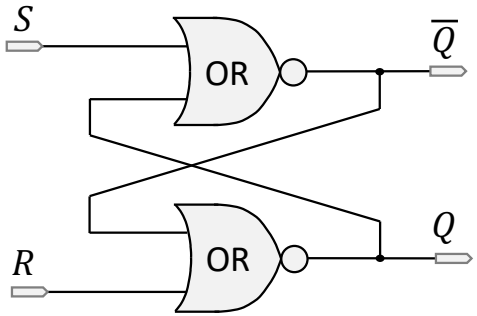


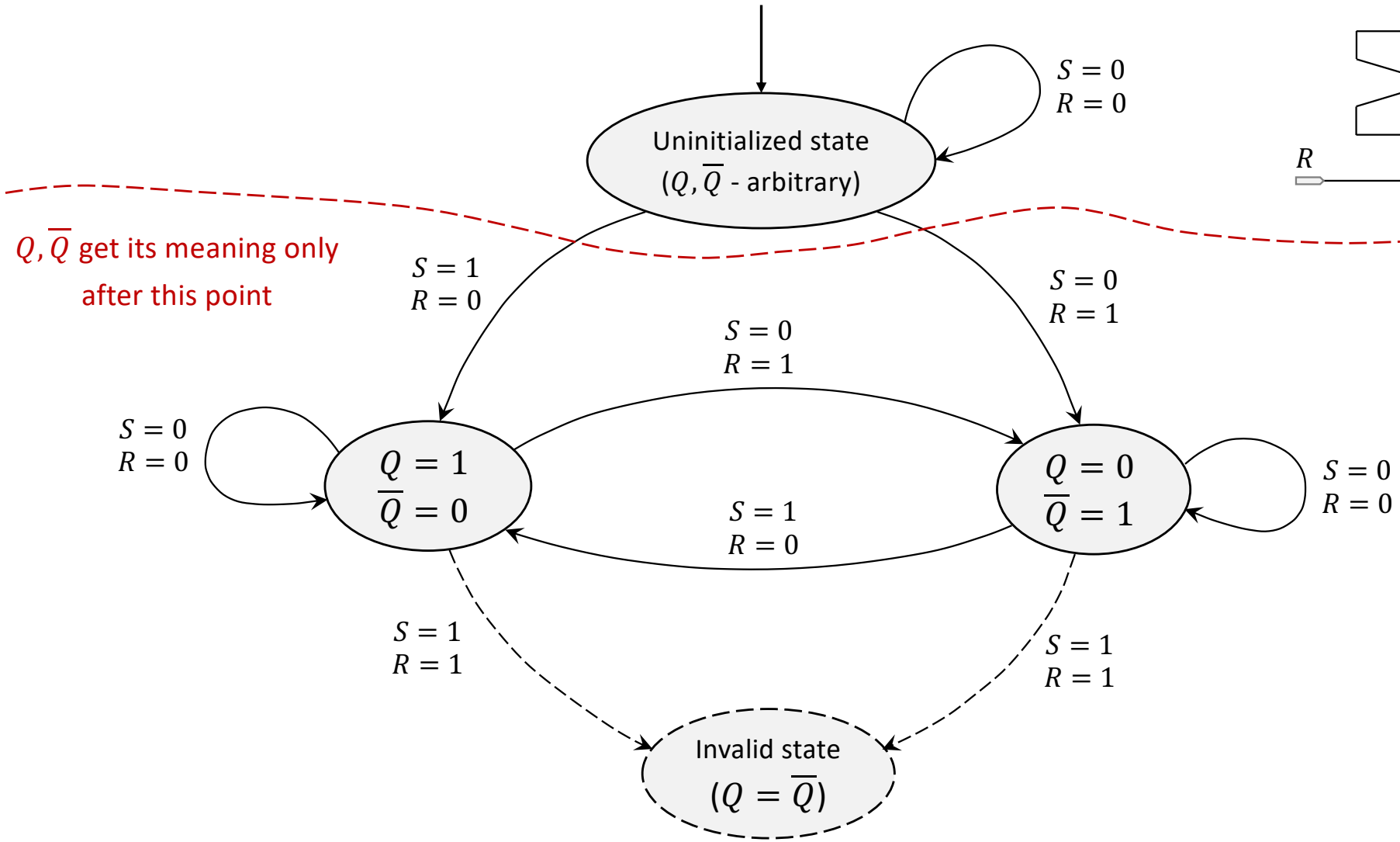

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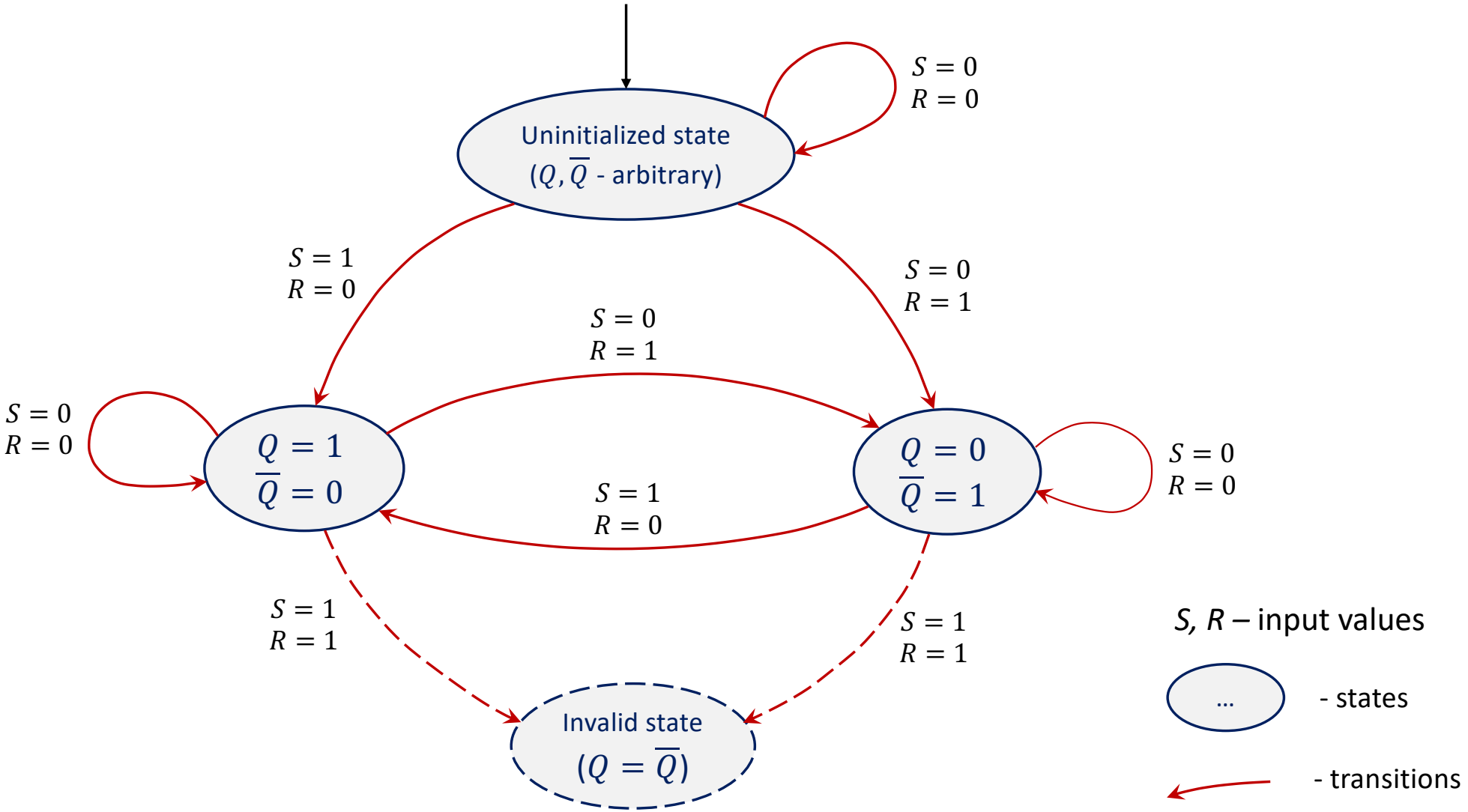
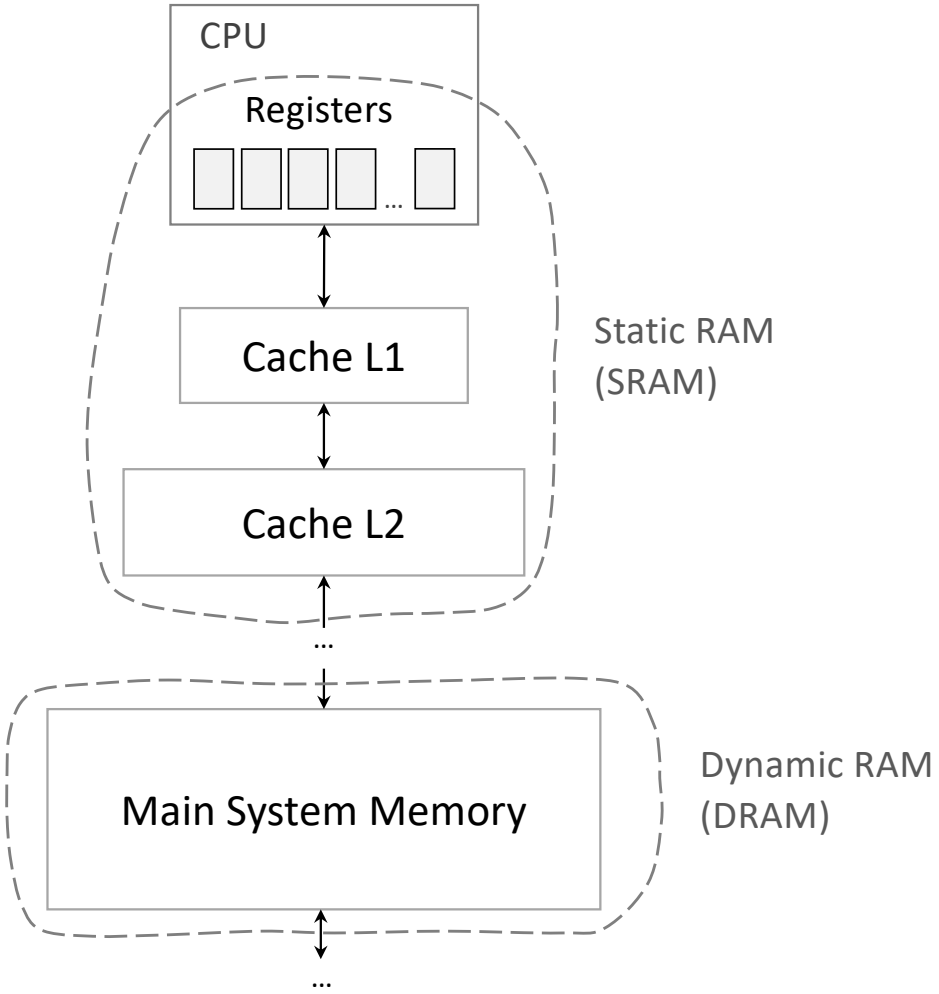
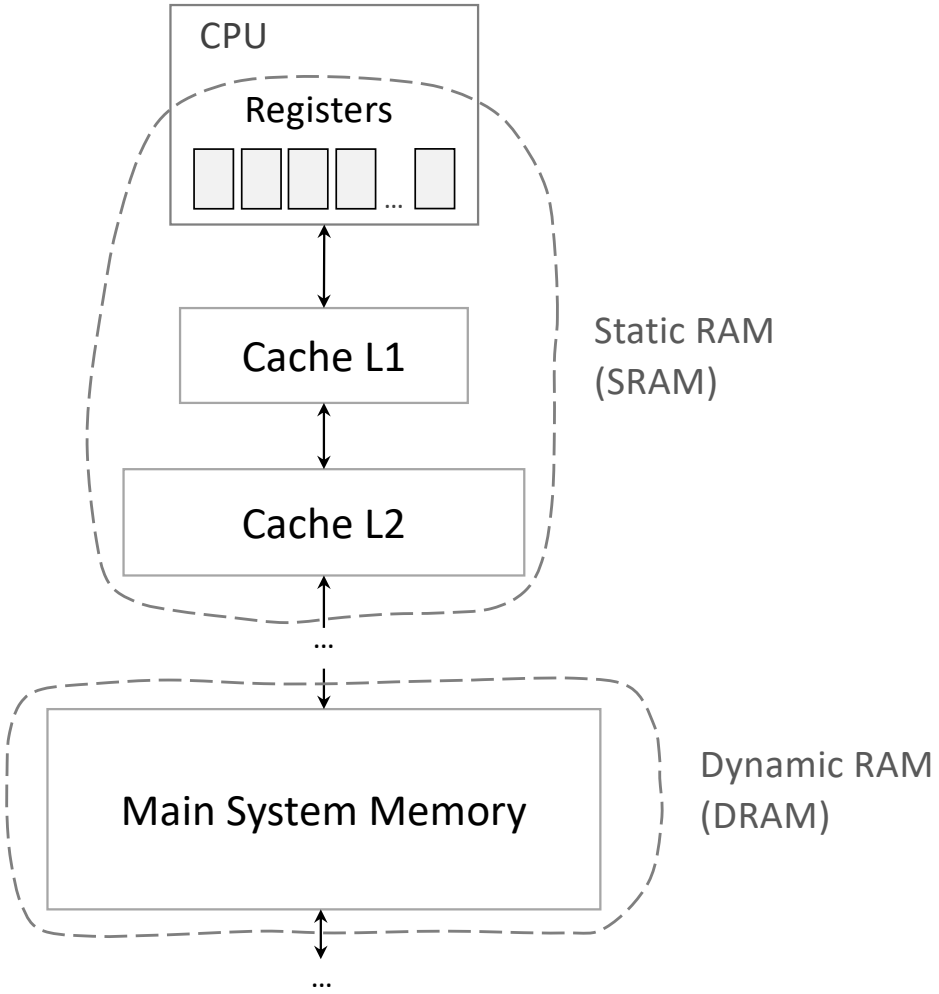


# The Comparison of DRAM and SRAM Memory Types




| **Characteristic** | **SRAM** | **DRAM** |
|---|---|---|
| Access Speed | | |
| Storage Capacity | | |
| Storage Element | | |
| Usage | | |
| Cost | | |
| Power Consumption | | |
| Organisation | | |
| Power Leakage | | |
| Chip Reliability | | |
| Volatility | | |
| Memory Cell Access | | |

# The Comparison of DRAM and SRAM Memory Types




| Characteristic | SRAM | DRAM |
|---|---|---|
| Access Speed | Faster | Slower |
| Storage Capacity | | |
| Storage Element | | |
| Usage | | |
| Cost | | |
| Power Consumption | | |
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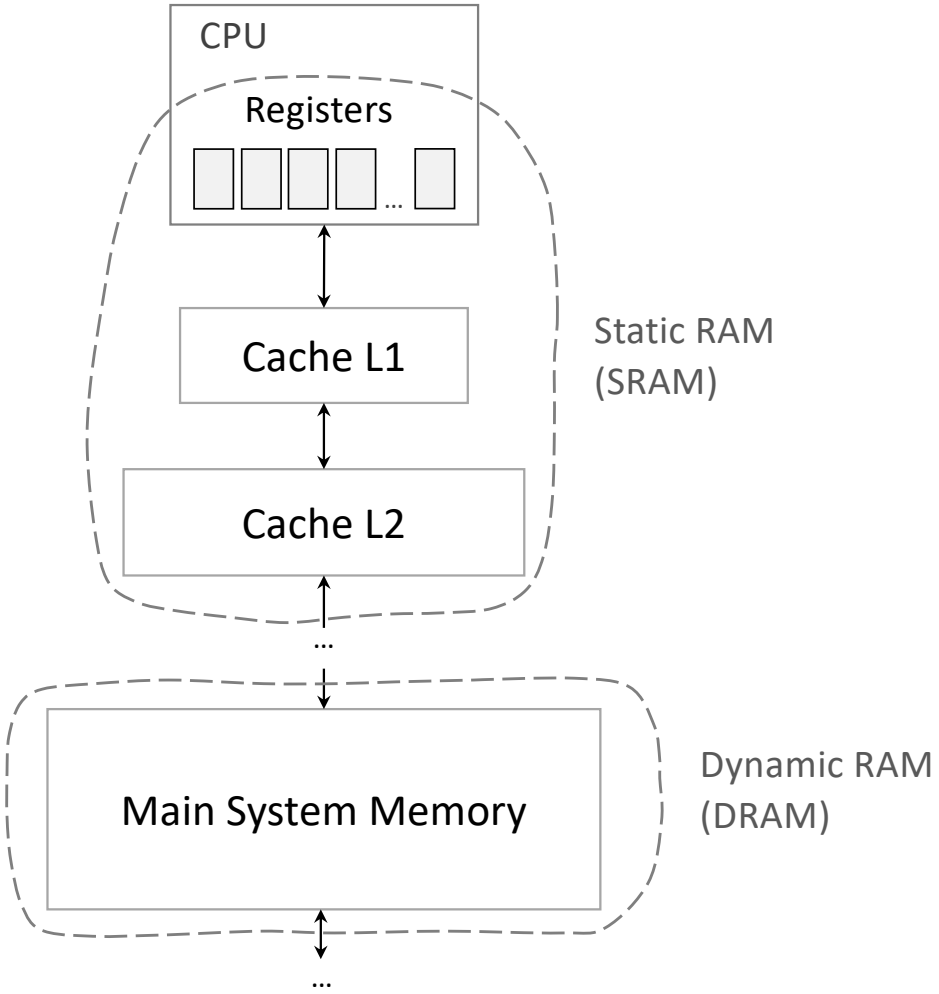


| Characteristic | SRAM | DRAM |
|---|---|---|
| Access Speed | Faster | Slower |
| Storage Capacity | Smaller | Larger |
| Storage Element | | |
| Usage | | |
| Cost | | |
| Power Consumption | | |
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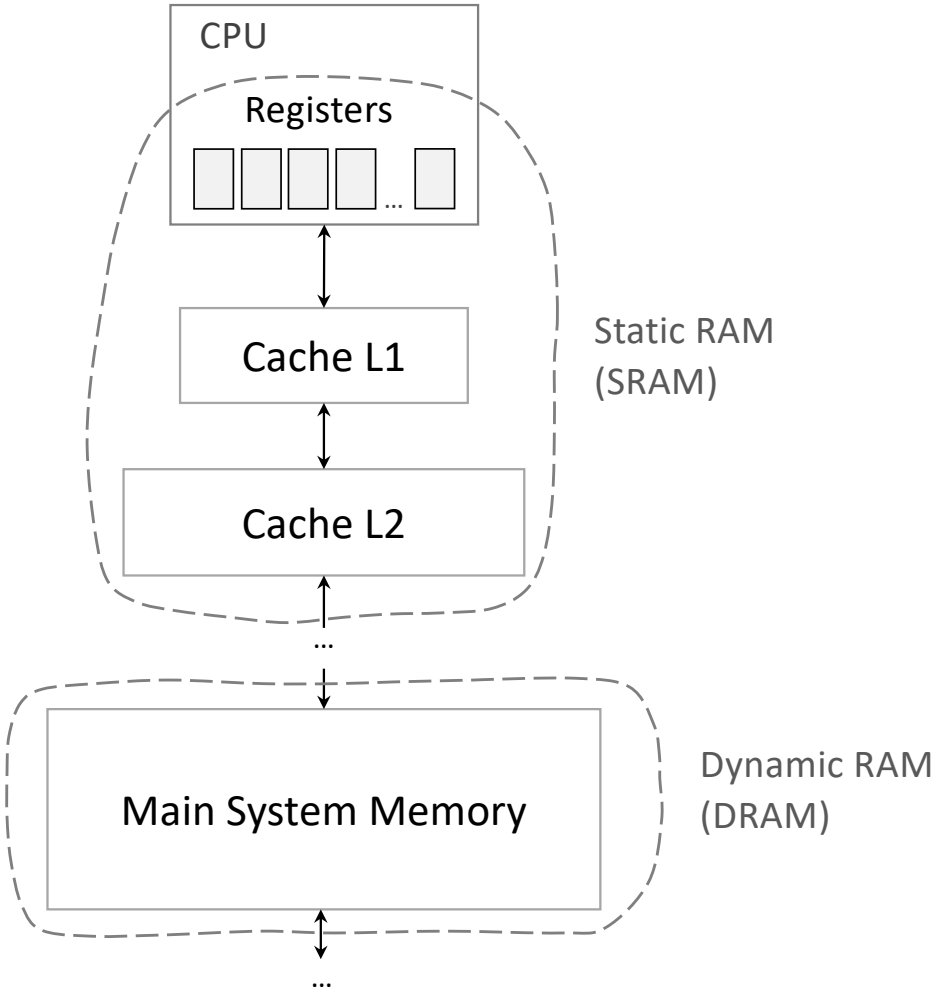


| **Characteristic** | **SRAM** | **DRAM** |
|---|---|---|
| Access Speed | Faster | Slower |
| Storage Capacity | Smaller | Larger |
| Storage Element | Flip-flop | Capacitor |
| Usage | | |
| Cost | | |
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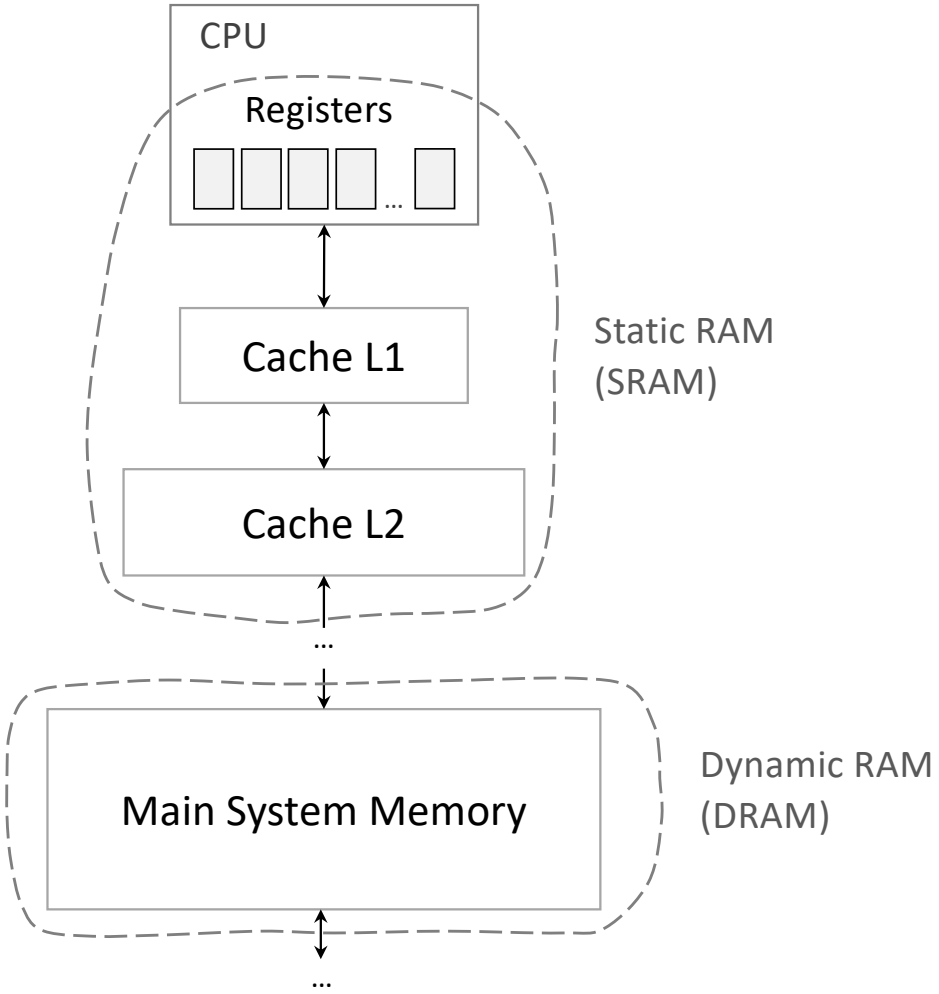


| Characteristic | SRAM | DRAM |
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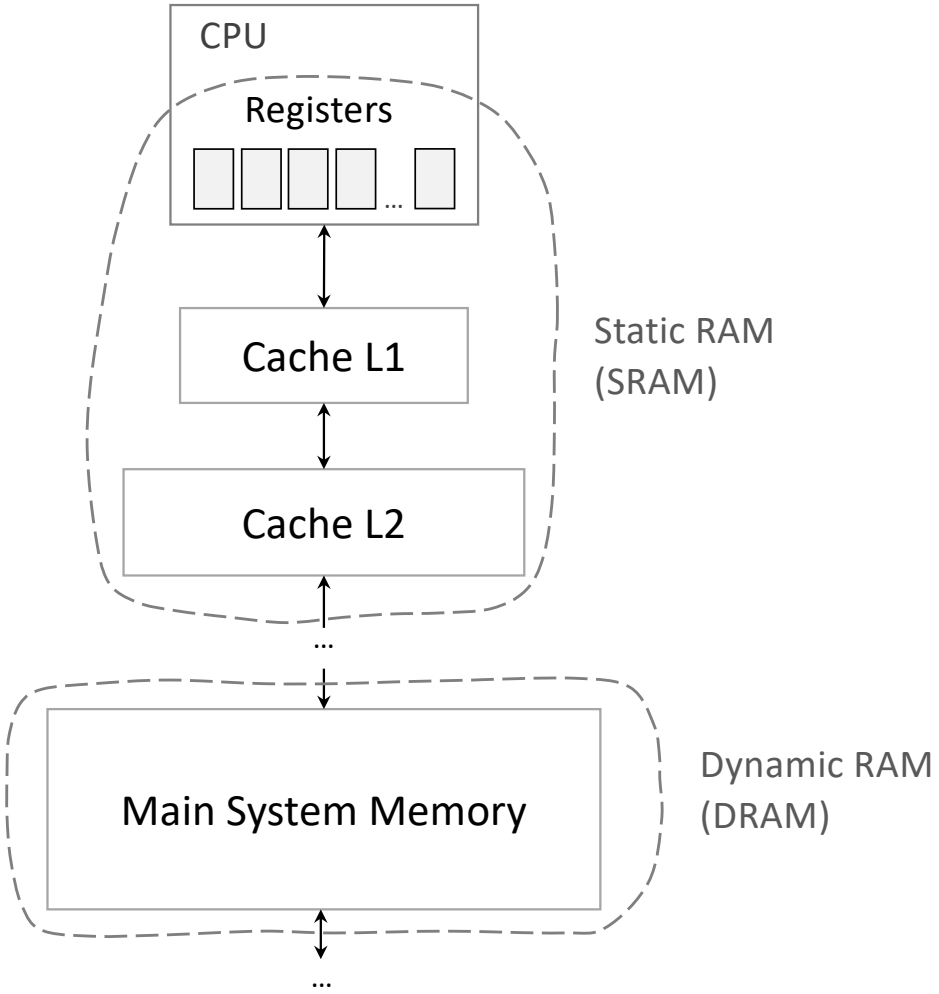


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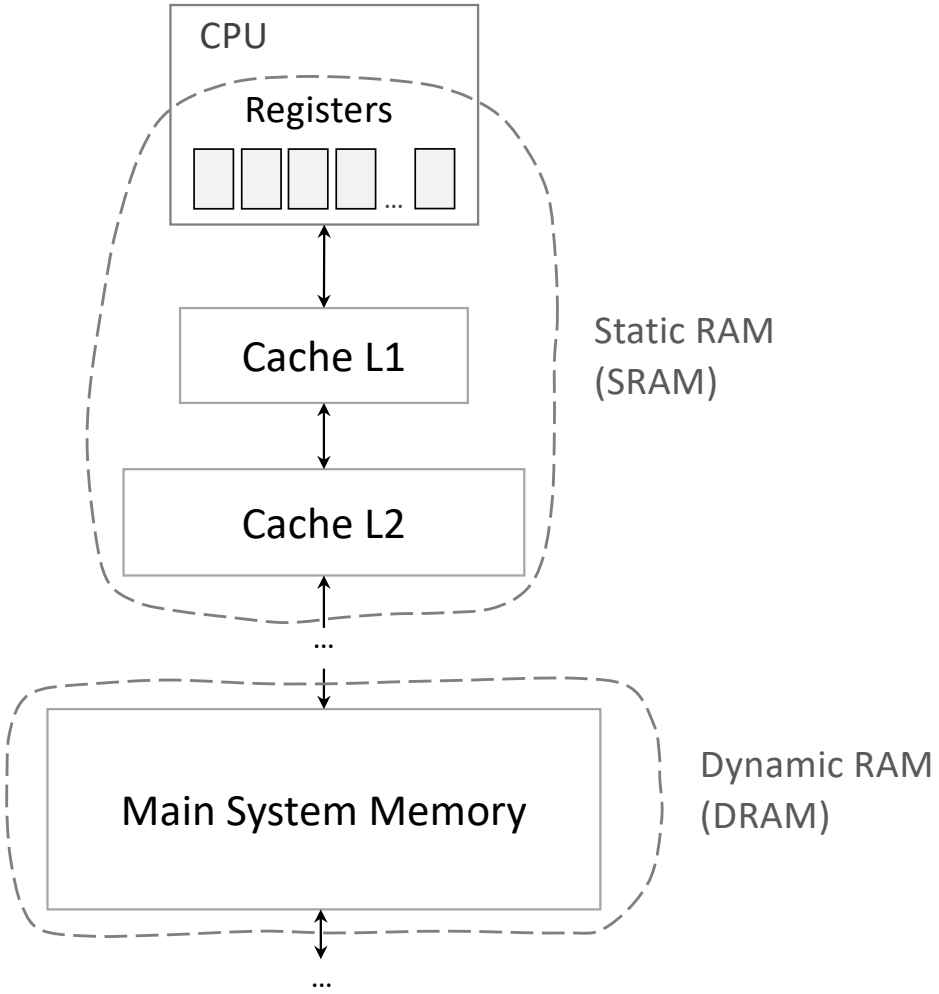


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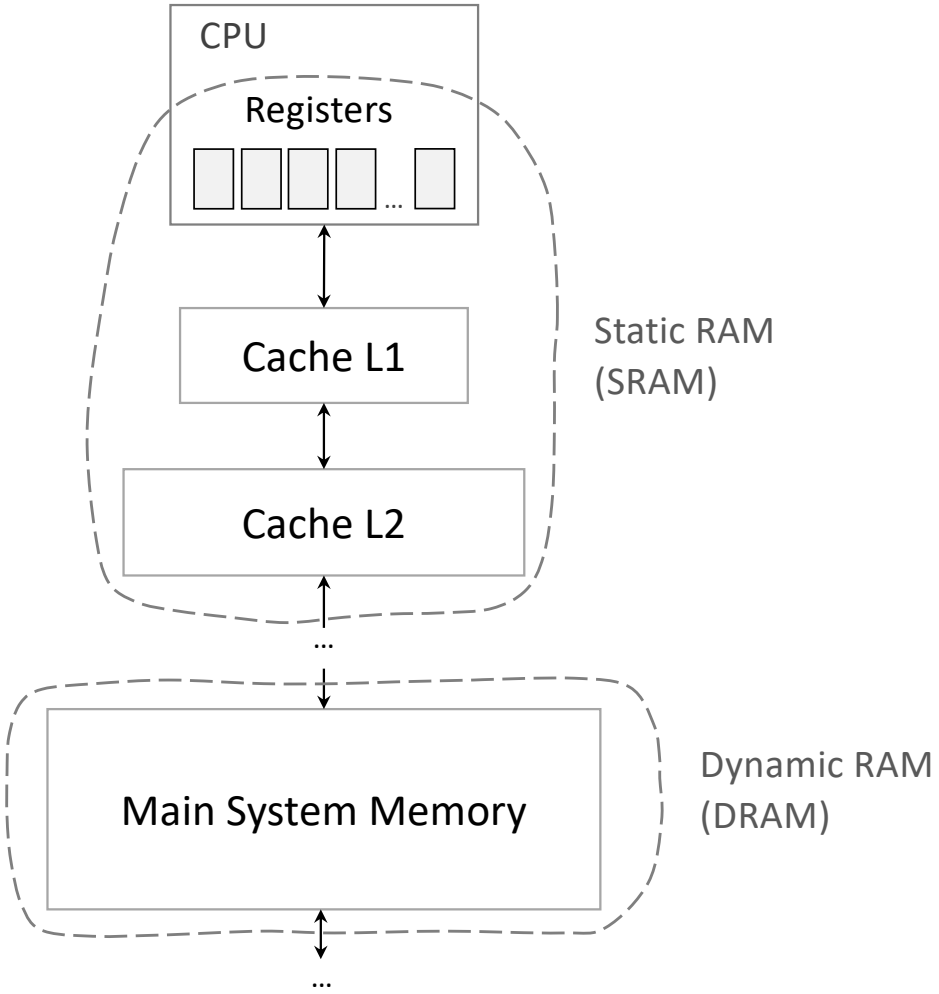


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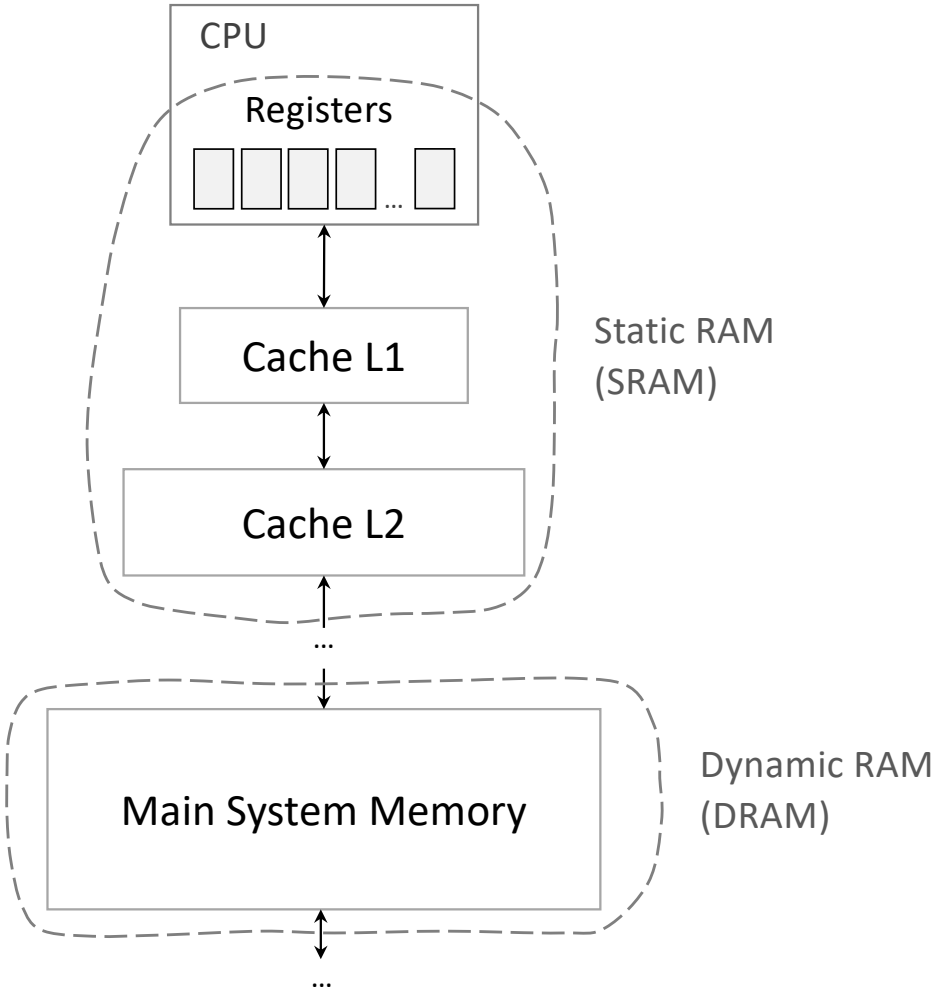


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| Organisation | Complex | Simpler |
| Power Leakage | Not present | Significant |
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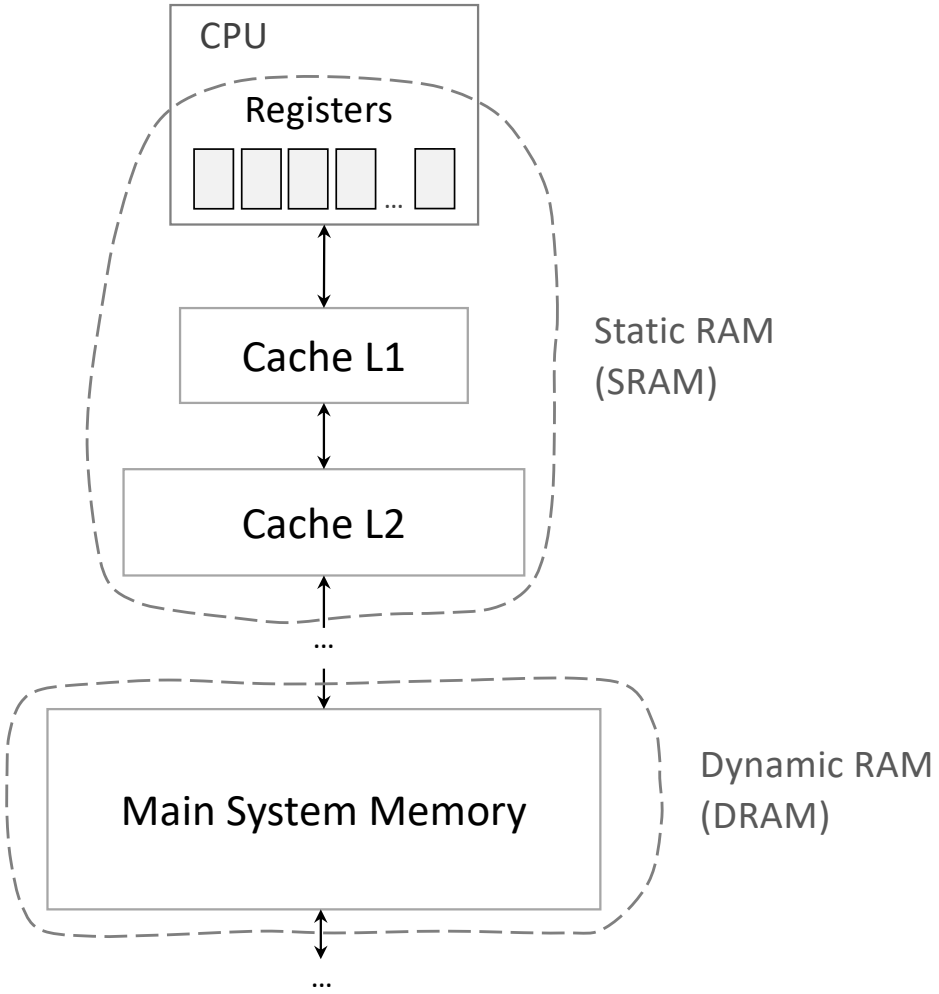


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| Power Leakage | Not present | Significant |
| Chip Reliability | More reliable | Less reliable |
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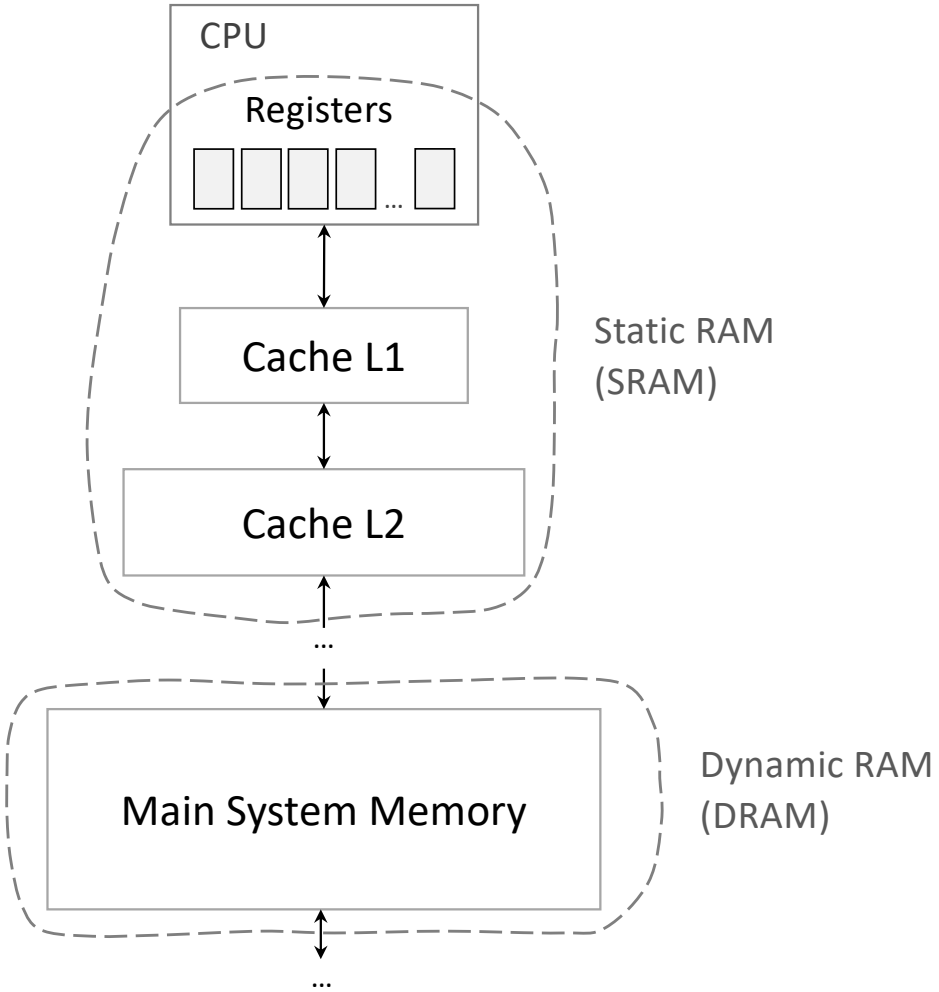


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| Organisation | Complex | Simpler |
| Power Leakage | Not present | Significant |
| Chip Reliability | More reliable | Less reliable |
| Volatility | Both are volatile (loose data if power is off) | |
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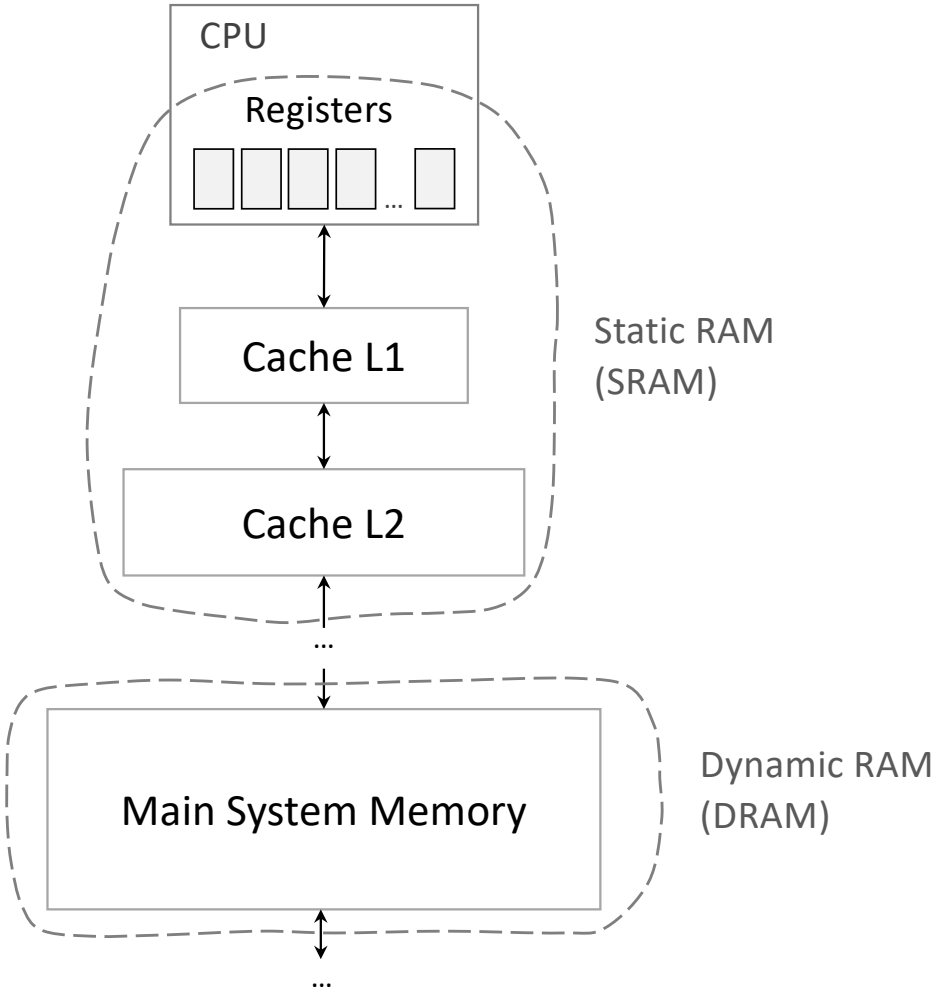


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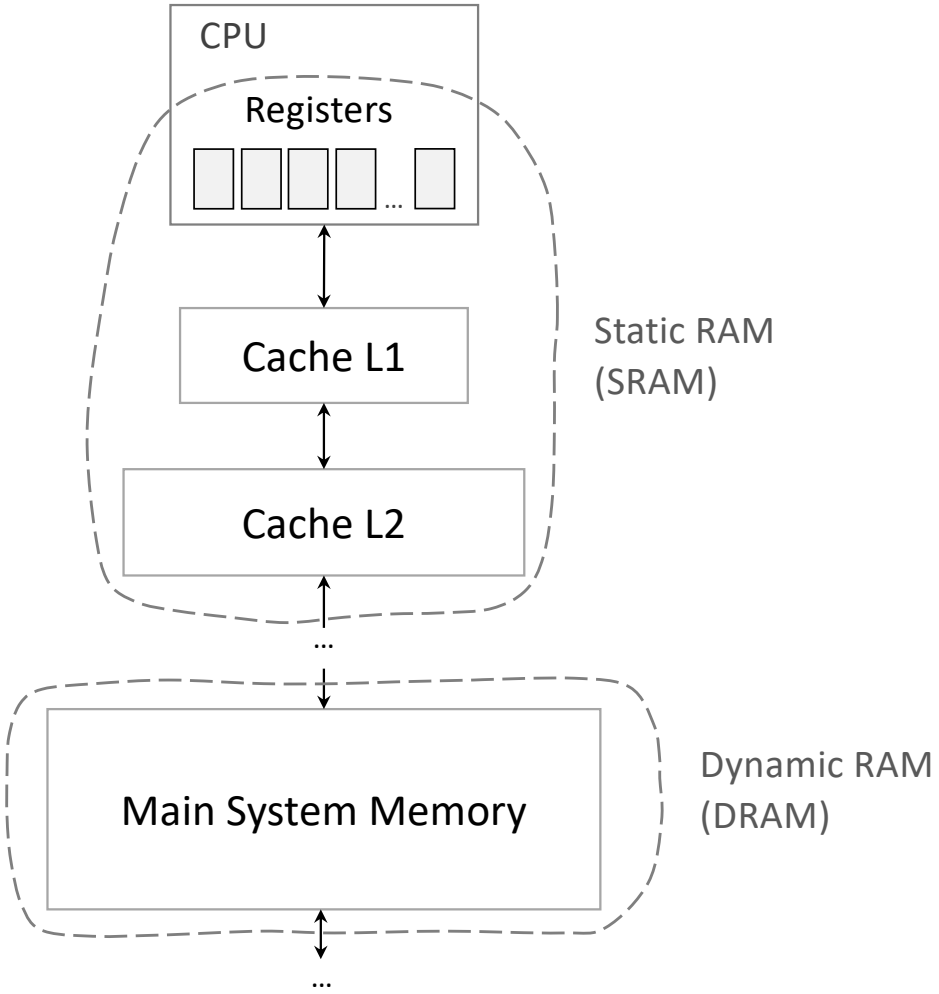


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