

A

B

C

D

A

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C

D

ZynqSoC\_Ethernet  
ZynqSoC\_Ethernet.SchDoc

USB  
USB.SchDoc

DDR3  
DDR3.SchDoc

UART\_RXD  
UART\_TXD  
USB\_PHY  
USB\_TYPEC\_INT\_B

UART\_RXD  
UART\_TXD  
USB\_PHY  
USB\_TYPEC\_INT\_B

ZYNQ\_I2C

ZYNQ\_I2C

SYZGY\_I2C

SYZGY  
SYZGY.SchDoc

SYZGY\_I2C

POD\_SUPPLY\_ENSW1  
POD\_SUPPLY\_ENSW2  
POD\_SUPPLY\_ENSW3  
POD\_SUPPLY\_ENSW4  
POD\_SUPPLY\_PGOOD

POD\_SUPPLY\_ENSW1  
POD\_SUPPLY\_ENSW2  
POD\_SUPPLY\_ENSW3  
POD\_SUPPLY\_ENSW4  
POD\_SUPPLY\_PGOOD

USER\_BUTTON\_0  
USER\_BUTTON\_1  
USER\_LED  
TEST\_MODE

MICROSD

Config  
Config.SchDoc

MICROSD

PS\_MIO1\_500

PS\_MIO1\_500

BOOT\_MODE

BOOT\_MODE

SYS\_SUPPLY\_I2C

SYS\_SUPPLY\_I2C

USER\_BUTTON\_0  
USER\_BUTTON\_1  
USER\_LED  
TEST\_MODE

SYS\_SUPPLY\_CE  
SYS\_SUPPLY\_ENSEQ  
SYS\_SUPPLY\_RST\_B

SYS\_SUPPLY\_PGOOD

Power  
Power.SchDoc

SYS\_SUPPLY\_I2C

SYS\_SUPPLY\_CE  
SYS\_SUPPLY\_ENSEQ  
SYS\_SUPPLY\_RST\_B

SYS\_SUPPLY\_PGOOD

### Test Points

PCB

HUB7012S-PCB-20171017

ASSEMBLY

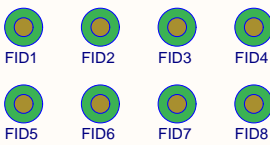
HUB7012S-ASSY

Opal Kelly Logo

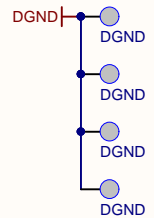
BARCODE LABEL

LABEL-USB-SN

### Fiducials



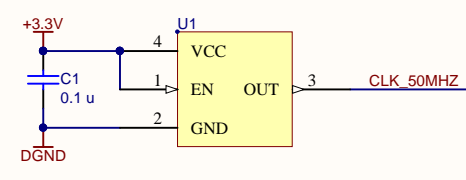
### Mounting Holes



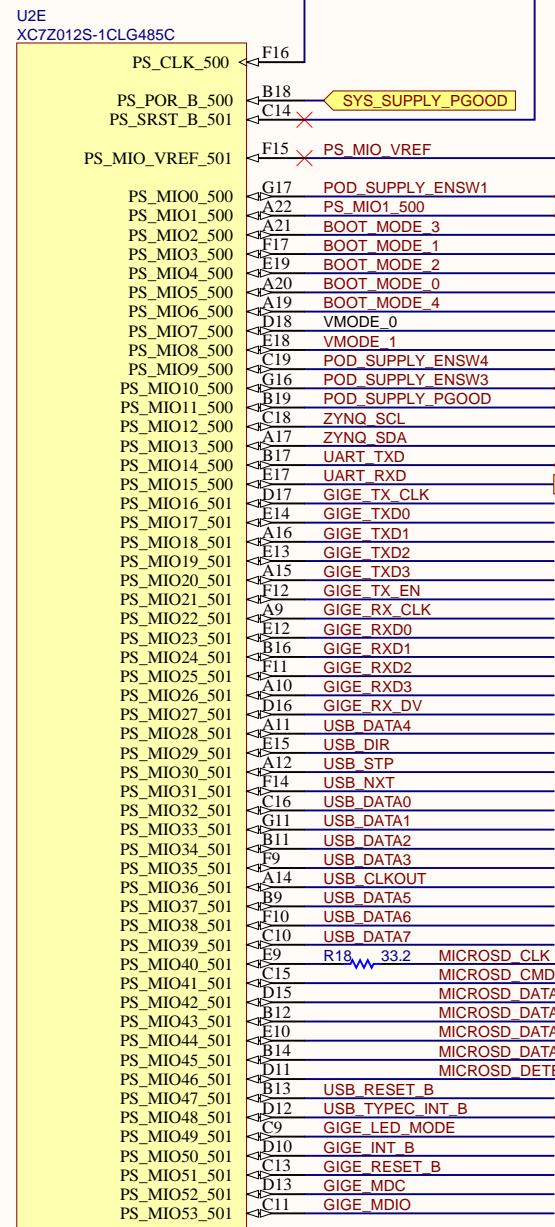
Title: <i>HUB7012S - Top</i>			
Size: C		Number: xxx	Revision: A
Date: 10/17/2017	Time: 12:36:57 PM		Sheet 1 of 7
File: C:\work\hub7012s-pcb\trunk\Top.SchDoc			



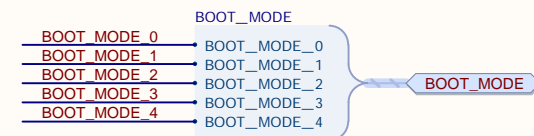
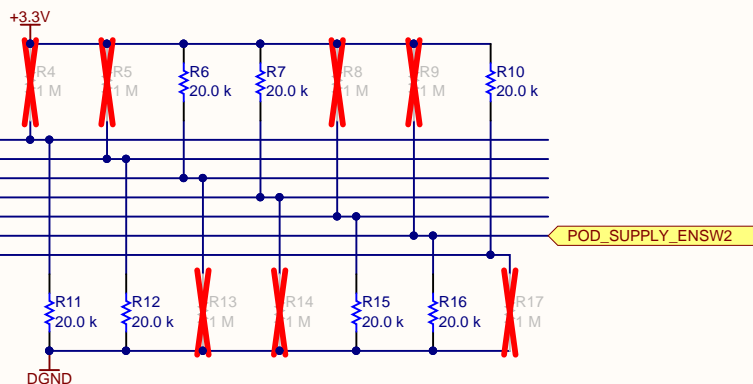
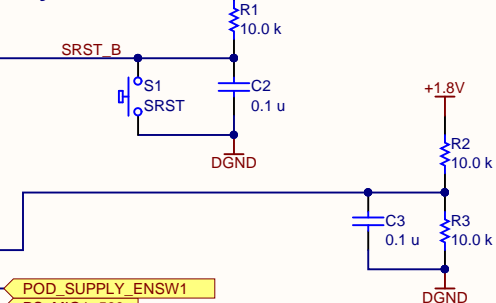
## 50MHz Clock



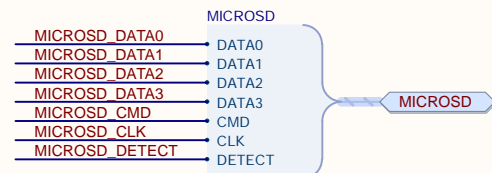
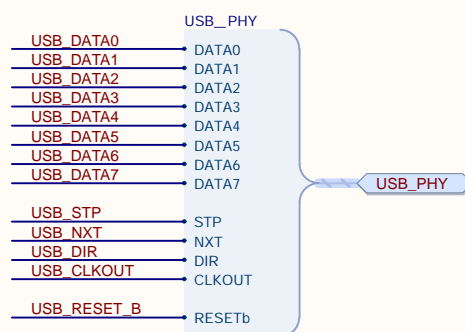
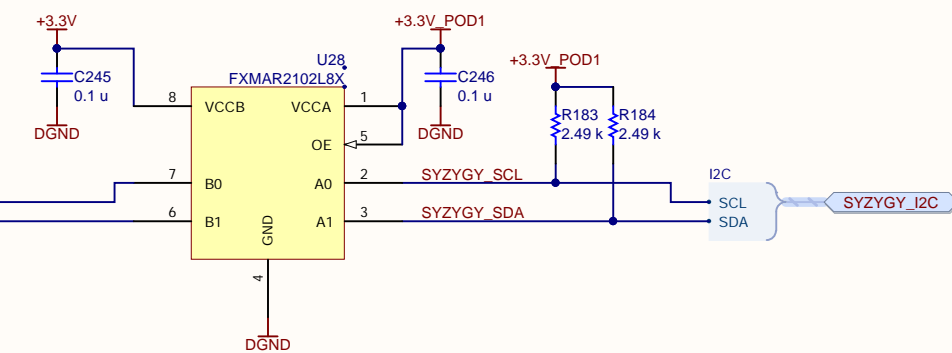
## Zynq SoC I/O



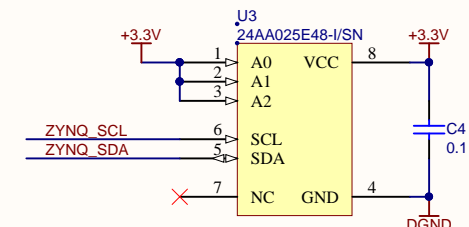
## Sys Reset



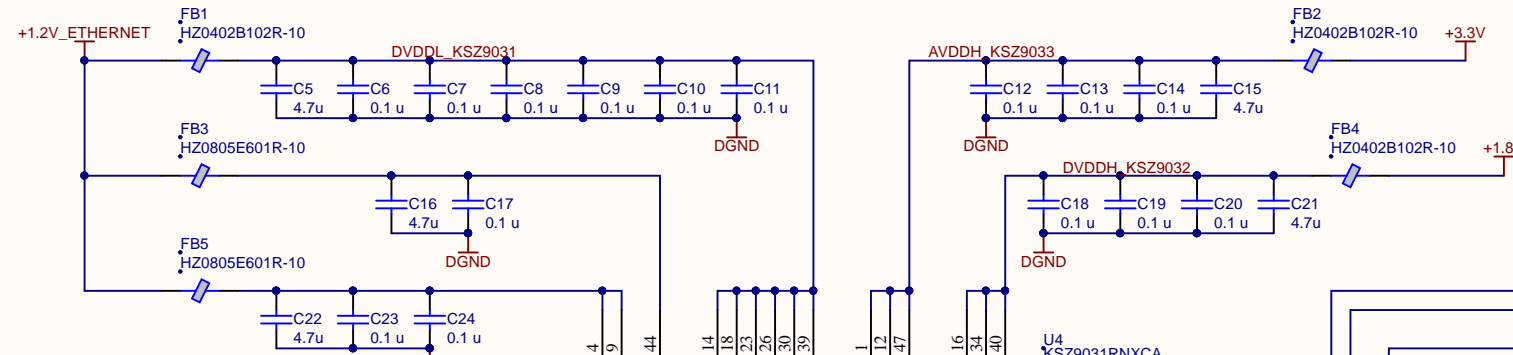
## FX3 I2C Level Translator / Isolator



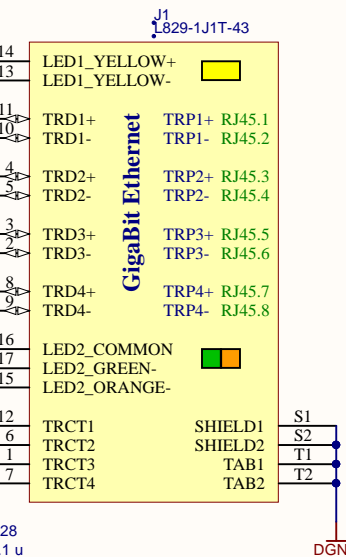
## Ethernet MAC ID PROM



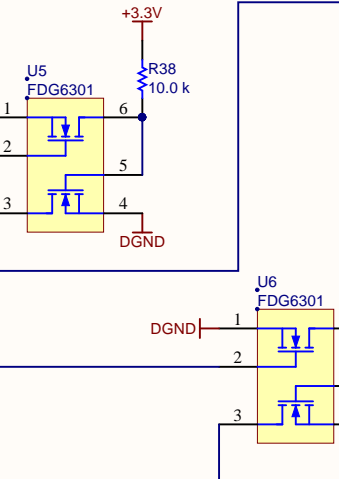
## Ethernet Transceiver



## Ethernet RJ45



## LED Level Shifters



Title HUB7012S - Zynq SoC

Size: C

Number: xxx

Revision: 1

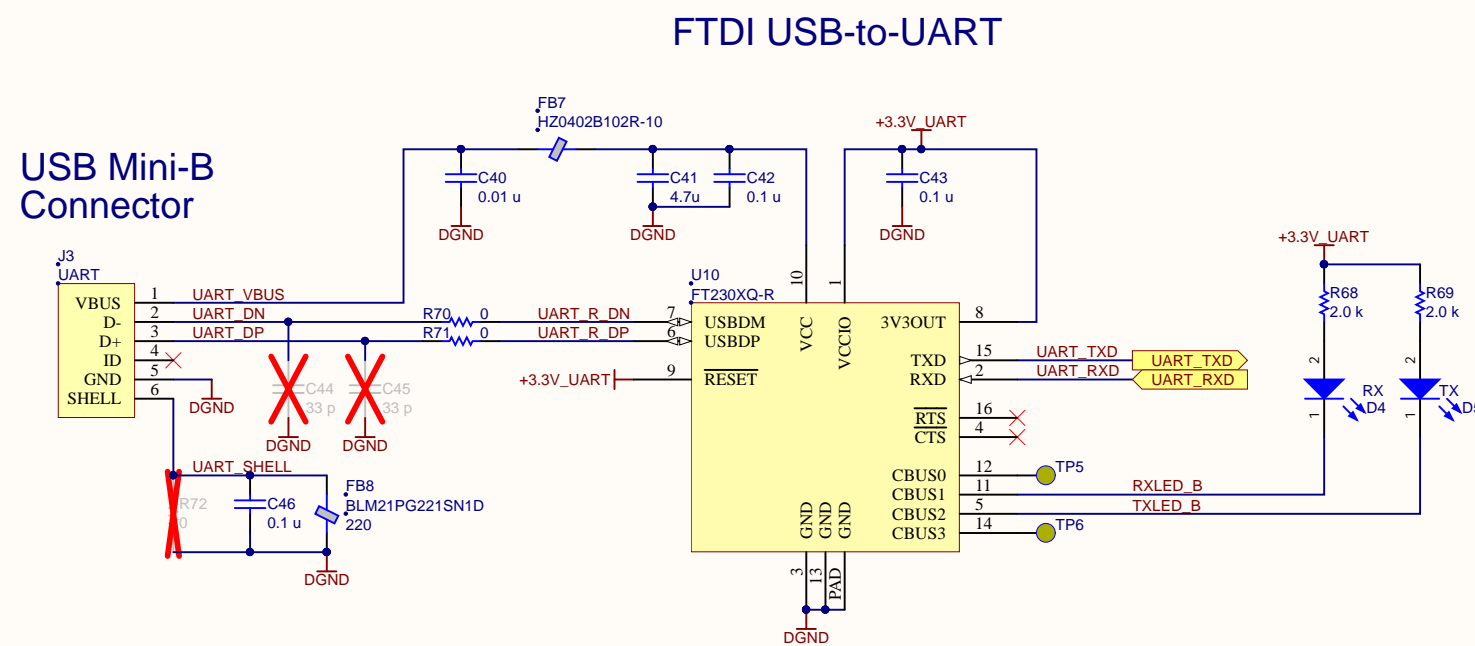
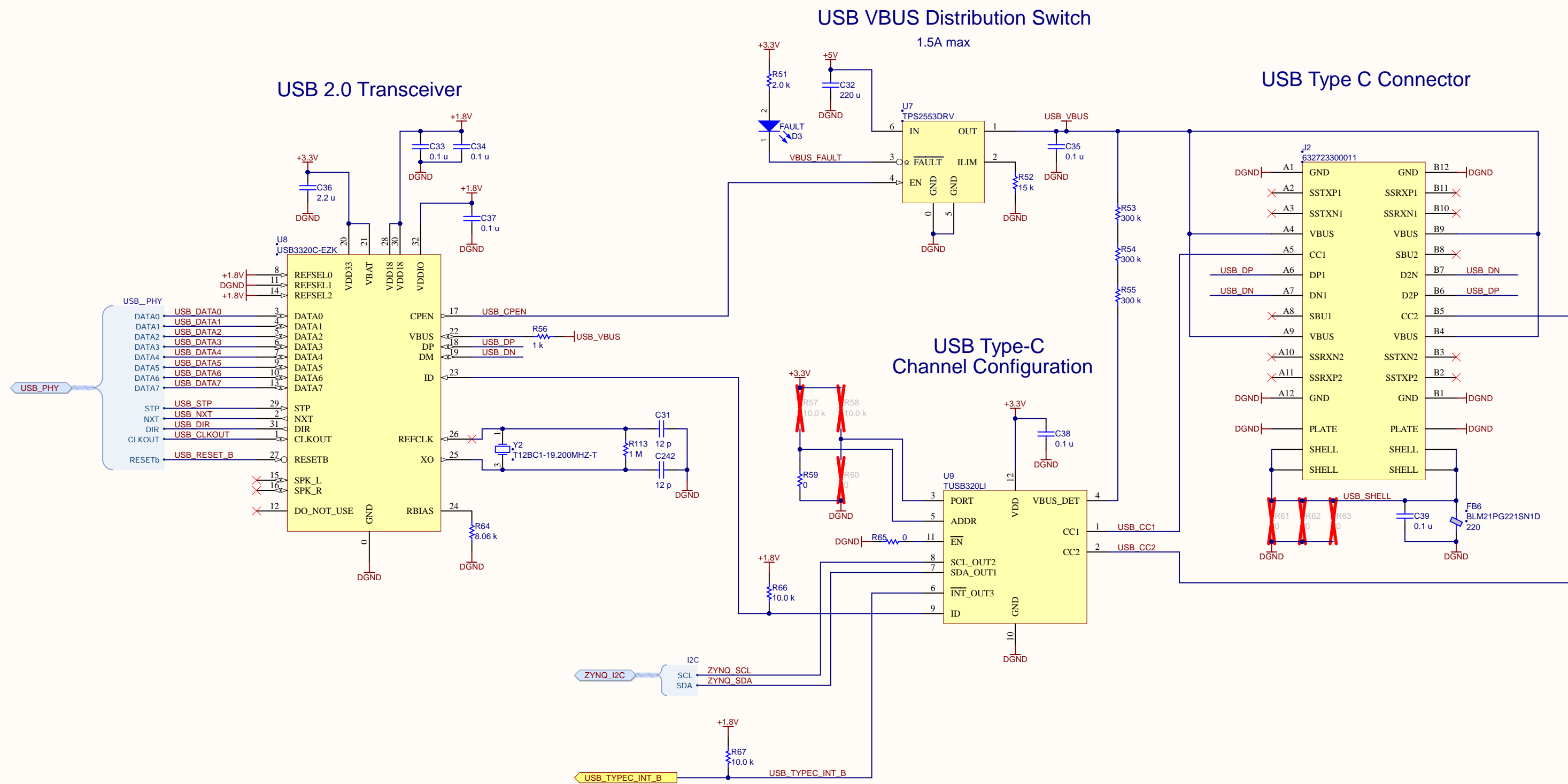
Date: 10/17/2017

Time: 12:36:58 PM

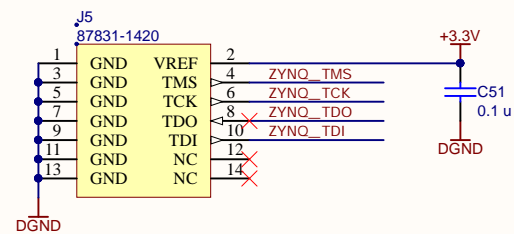
Sheet 2 of 7

File: C:\work\hub7012s-pcb\trunk\ZynqSoC\_Ethernet.SchDoc

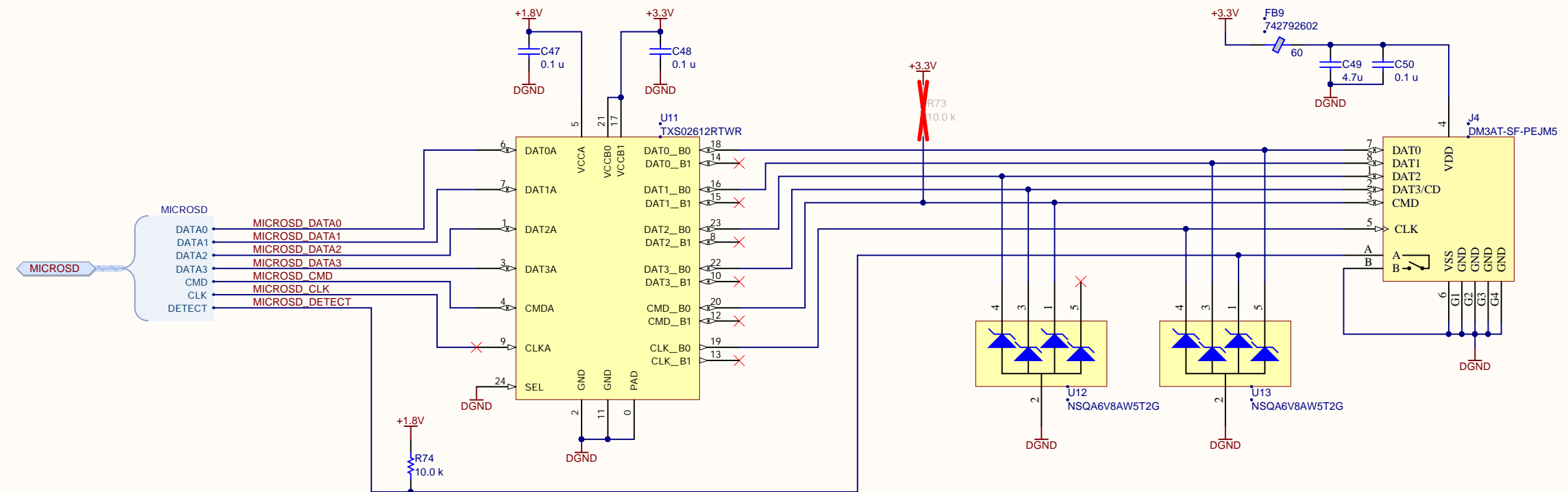
Opal Kelly  
13500 SW 72nd Ave Ste 100  
Portland, OR 97223  
http://www.opalkelly.com



## JTAG Header

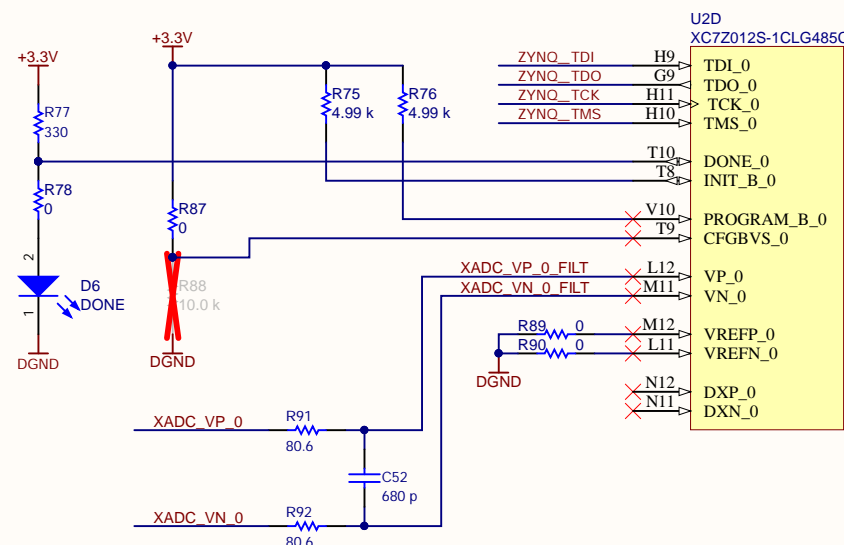


## microSD Level Translator



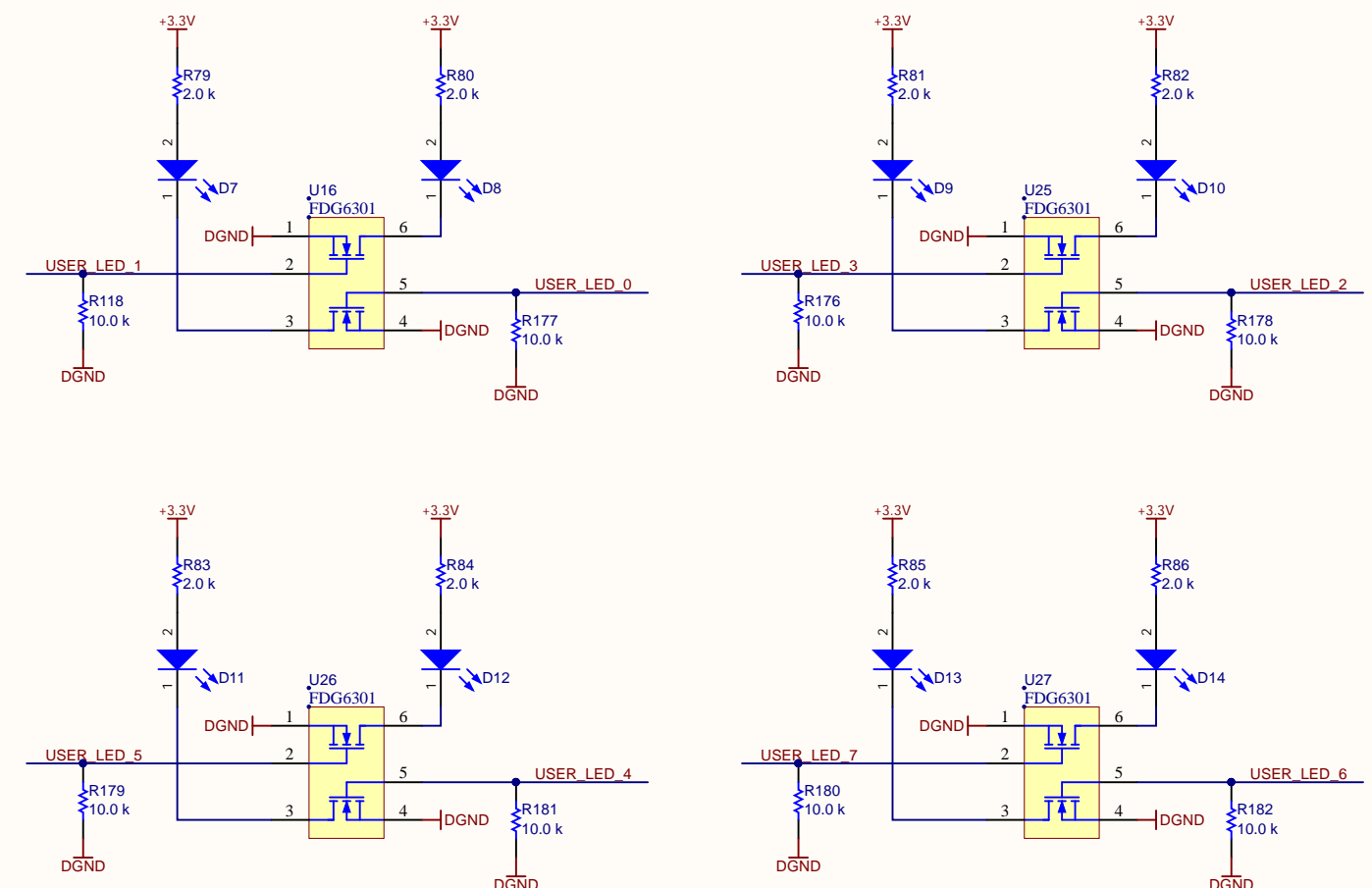
## microSD Card Connector

## Zynq Configuration

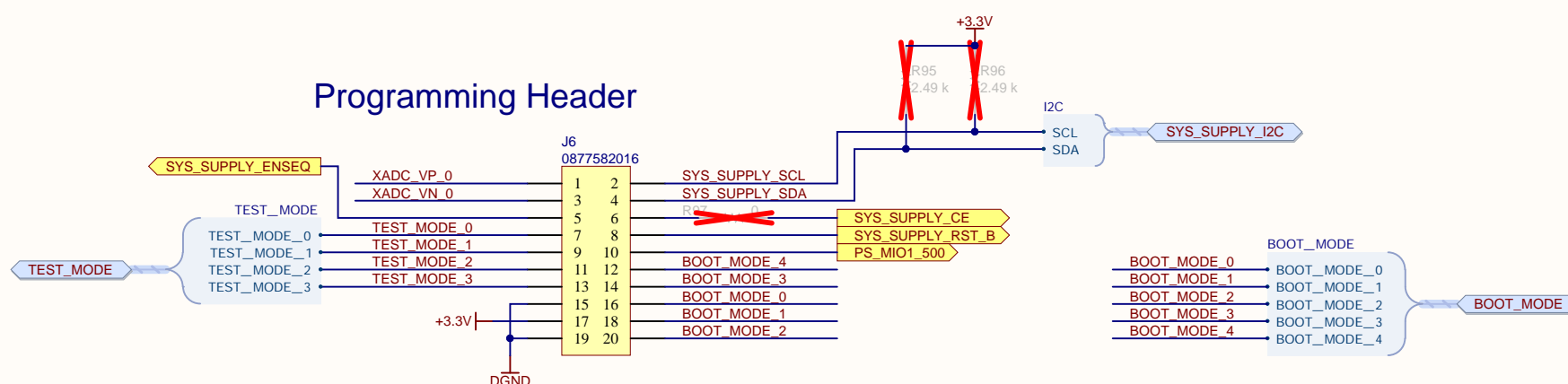


ADC anti-aliasing filter values chosen for sample rate of 1 Ms/s. See XADC User Guide UG480.

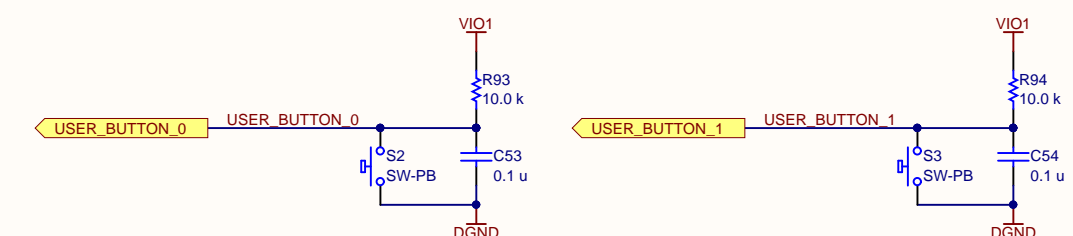
## User LEDs



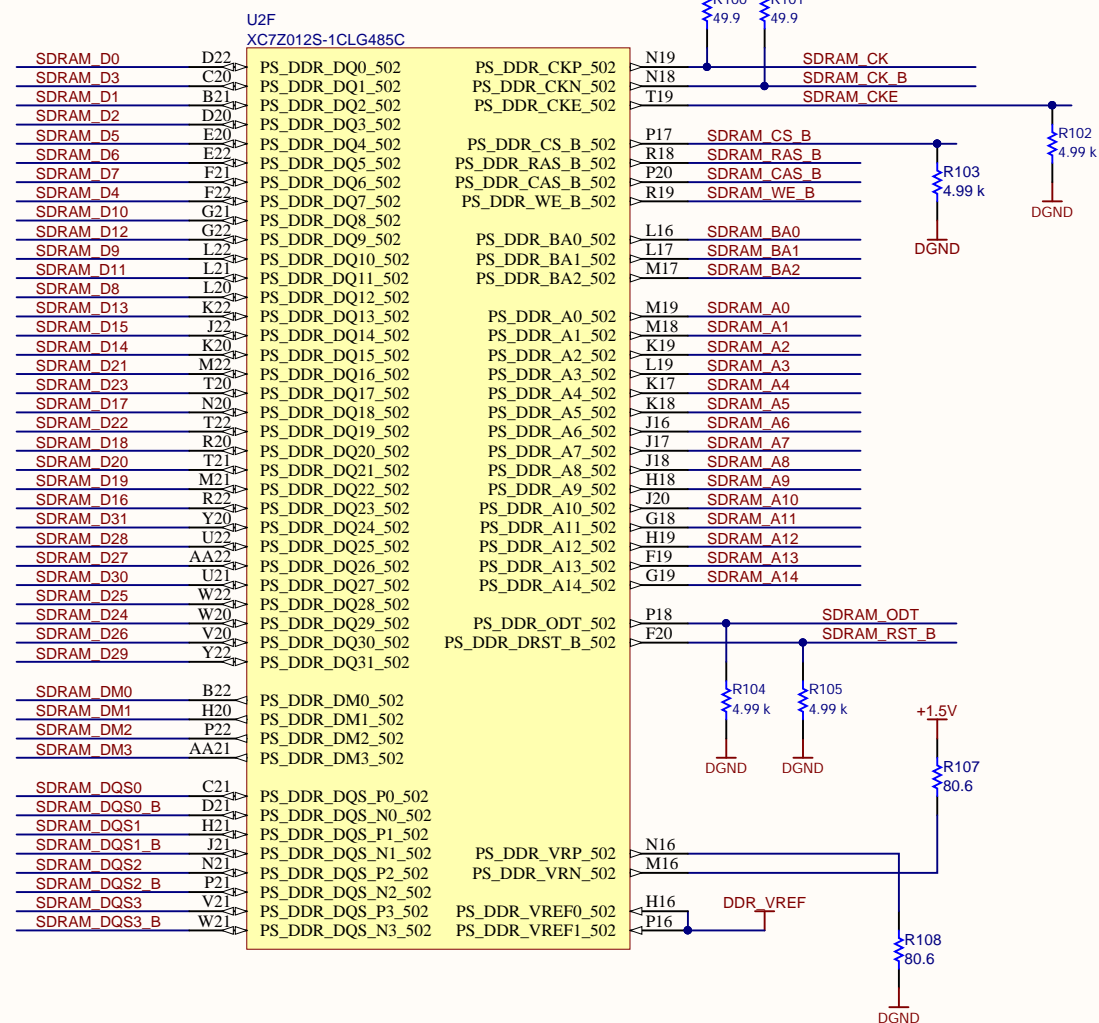
## Programming Header



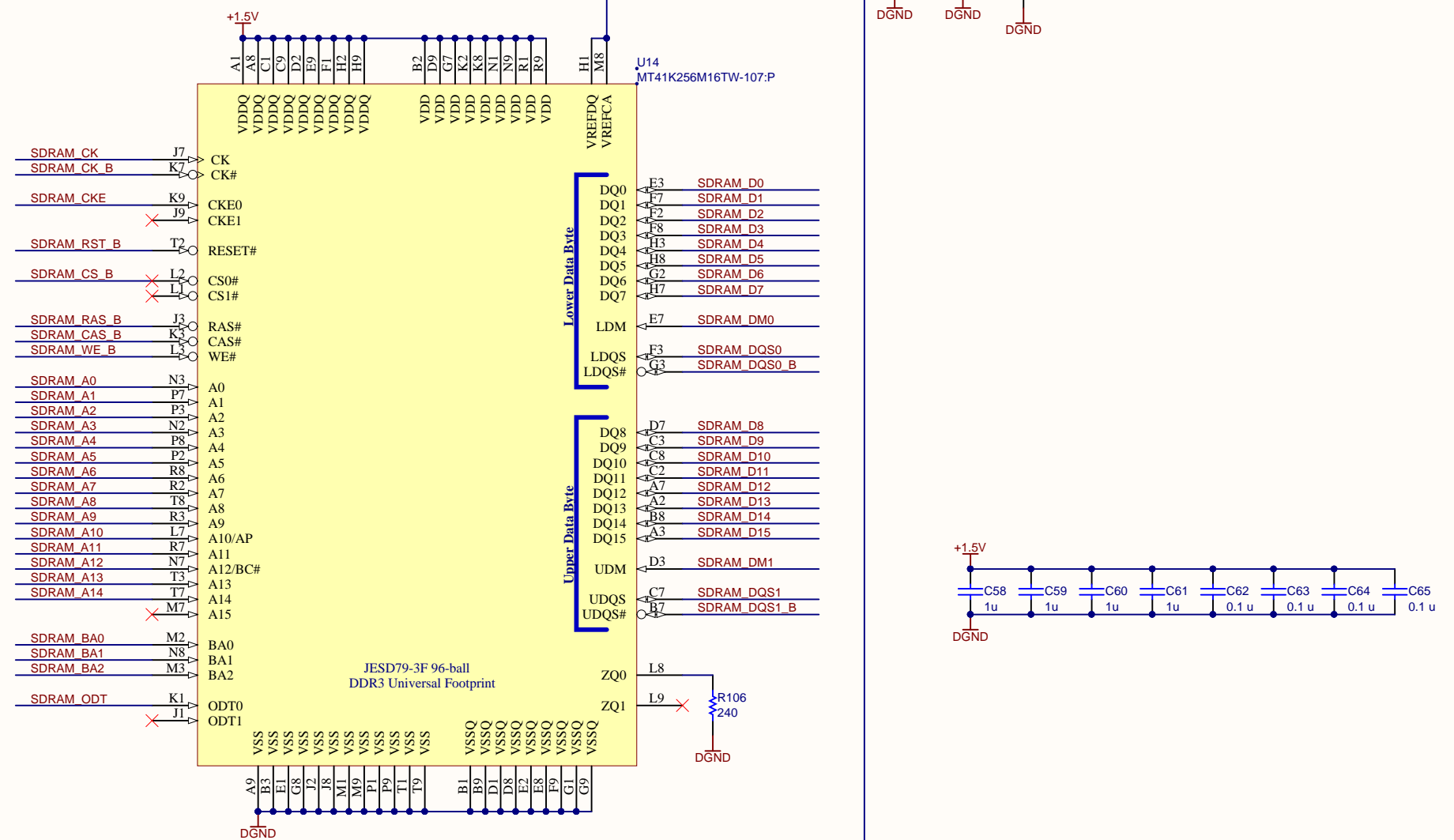
## User Buttons



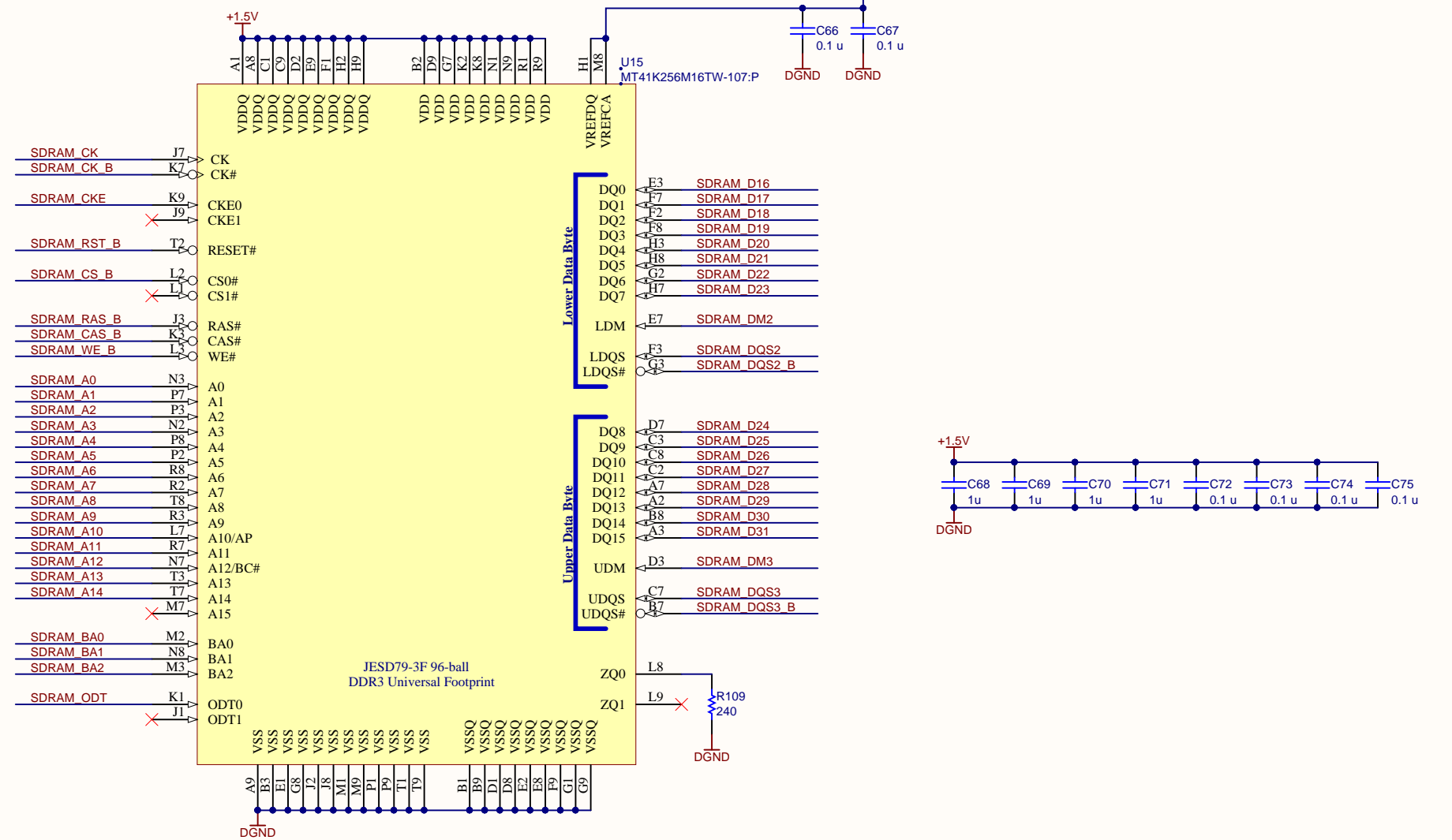
## Zynq DDR Interface



DDR3 4Gb 256Mx16

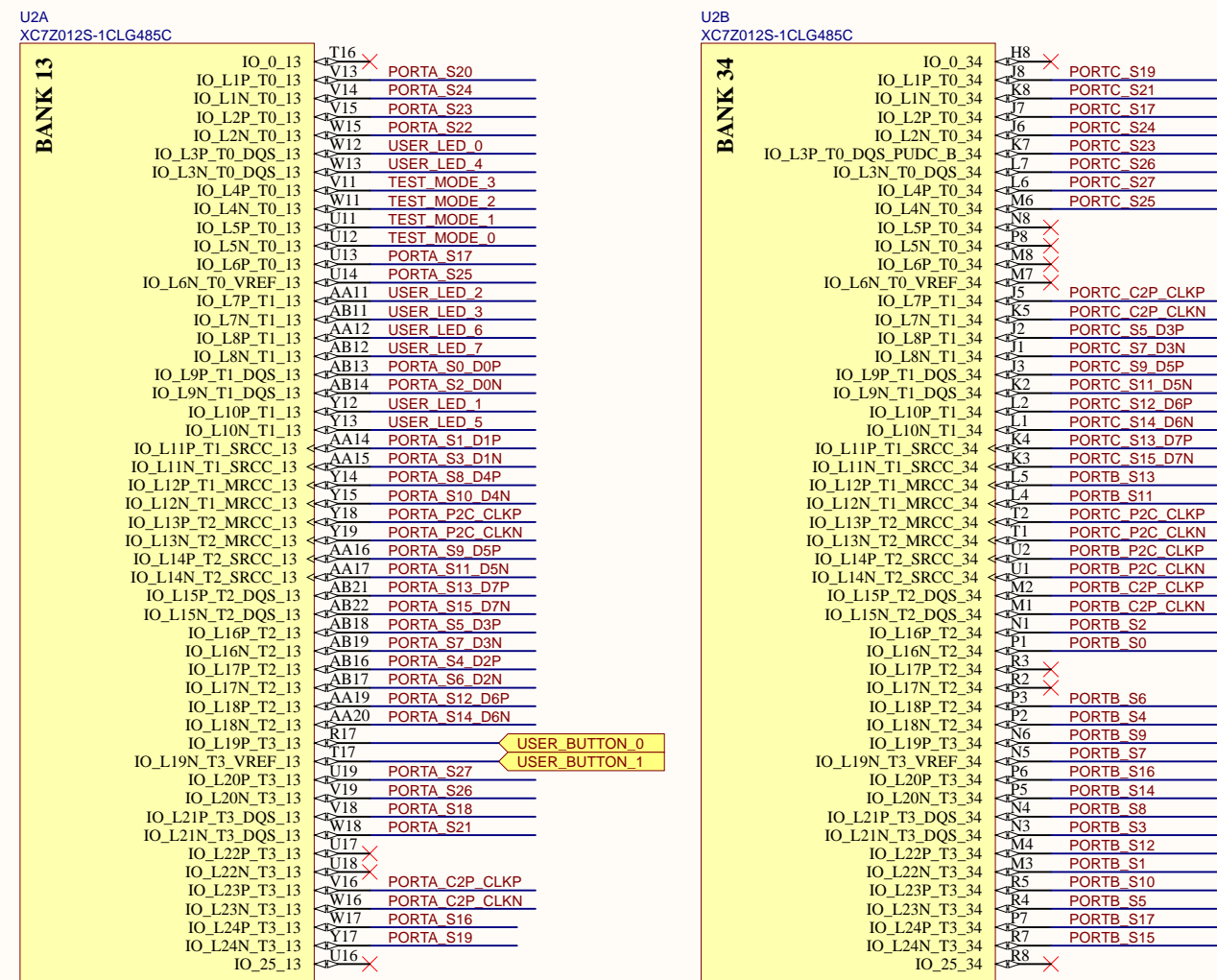


DDR3 4Gb 256Mx16

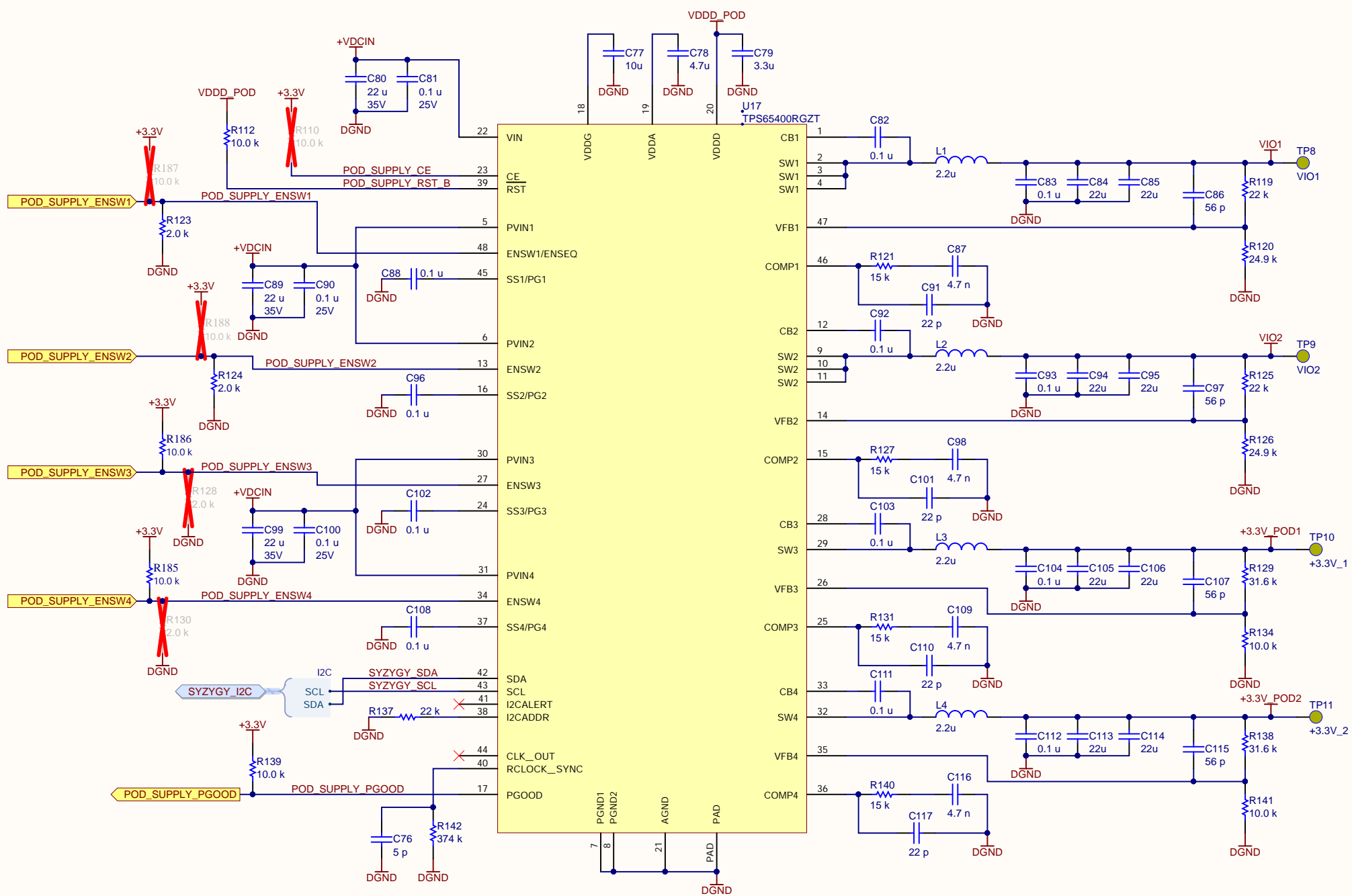




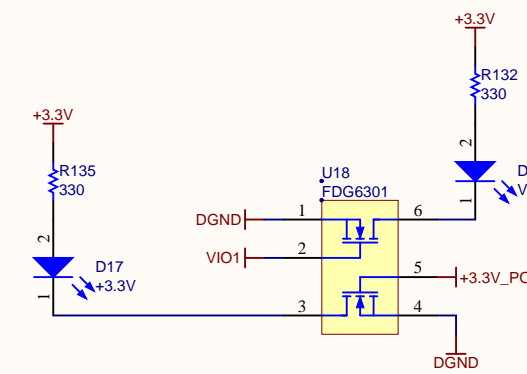
## Zynq Logic I/O



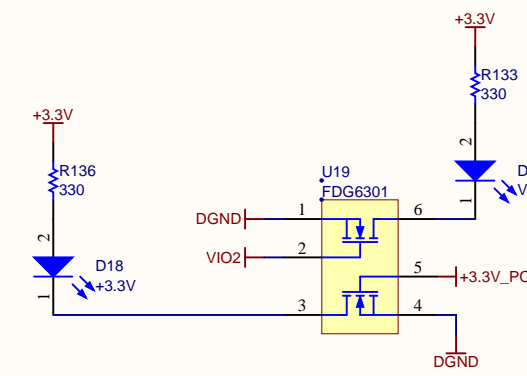
## Pod Supply



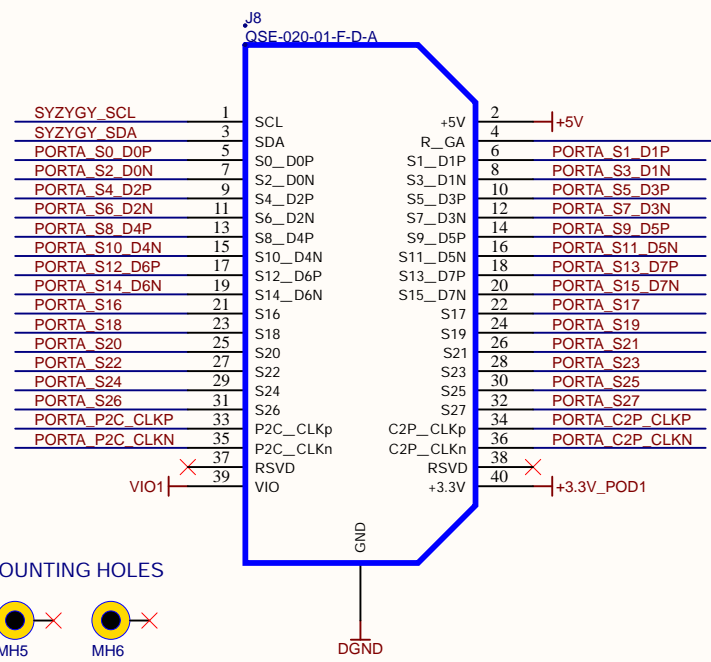
## Port Group 1 Power Indicators



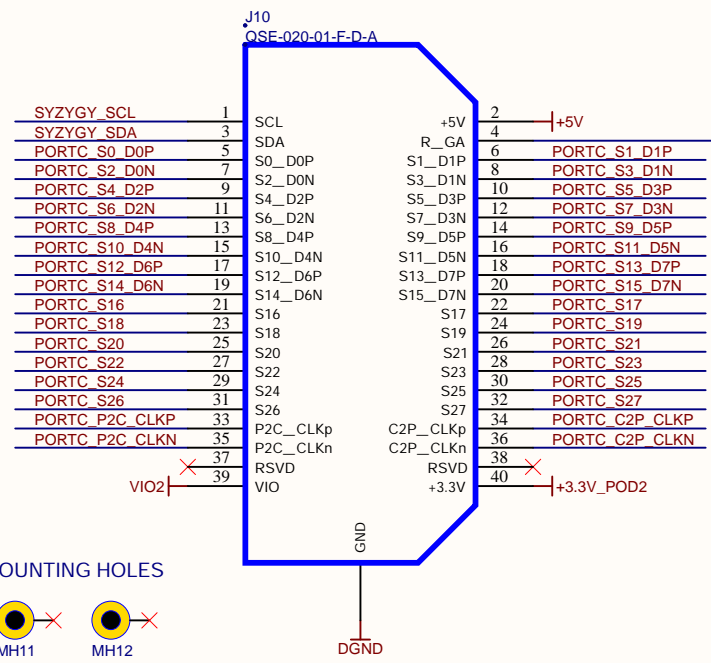
## Port Group 2 Power Indicators



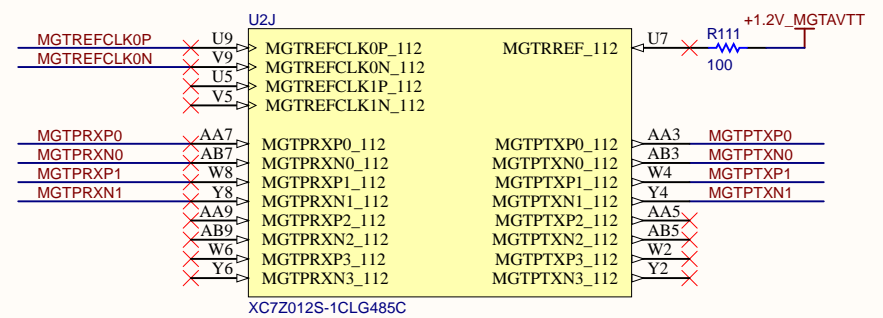
## PORT A (VIO1)



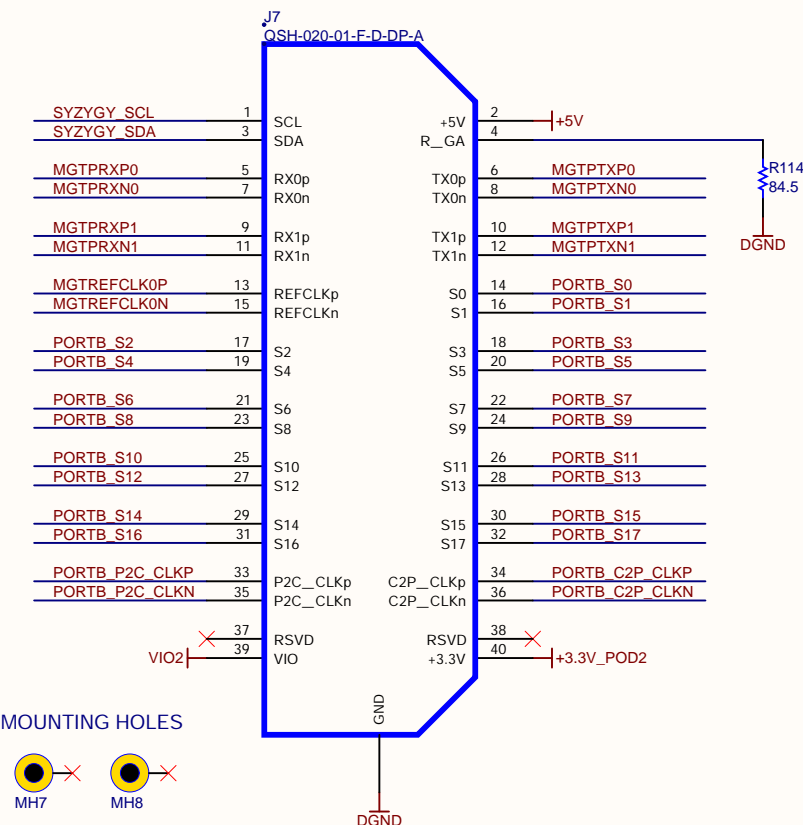
## PORT C (VIO2)



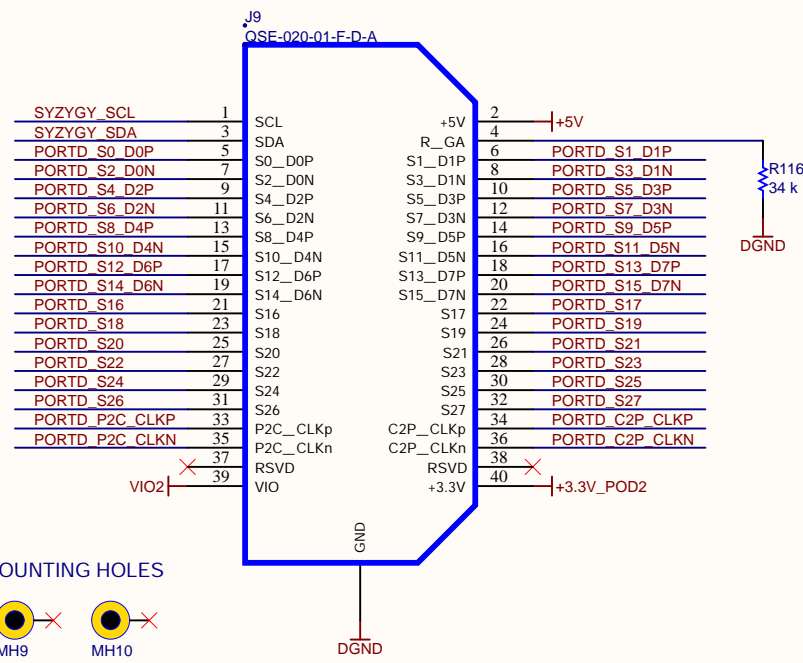
## Zynq Transceivers



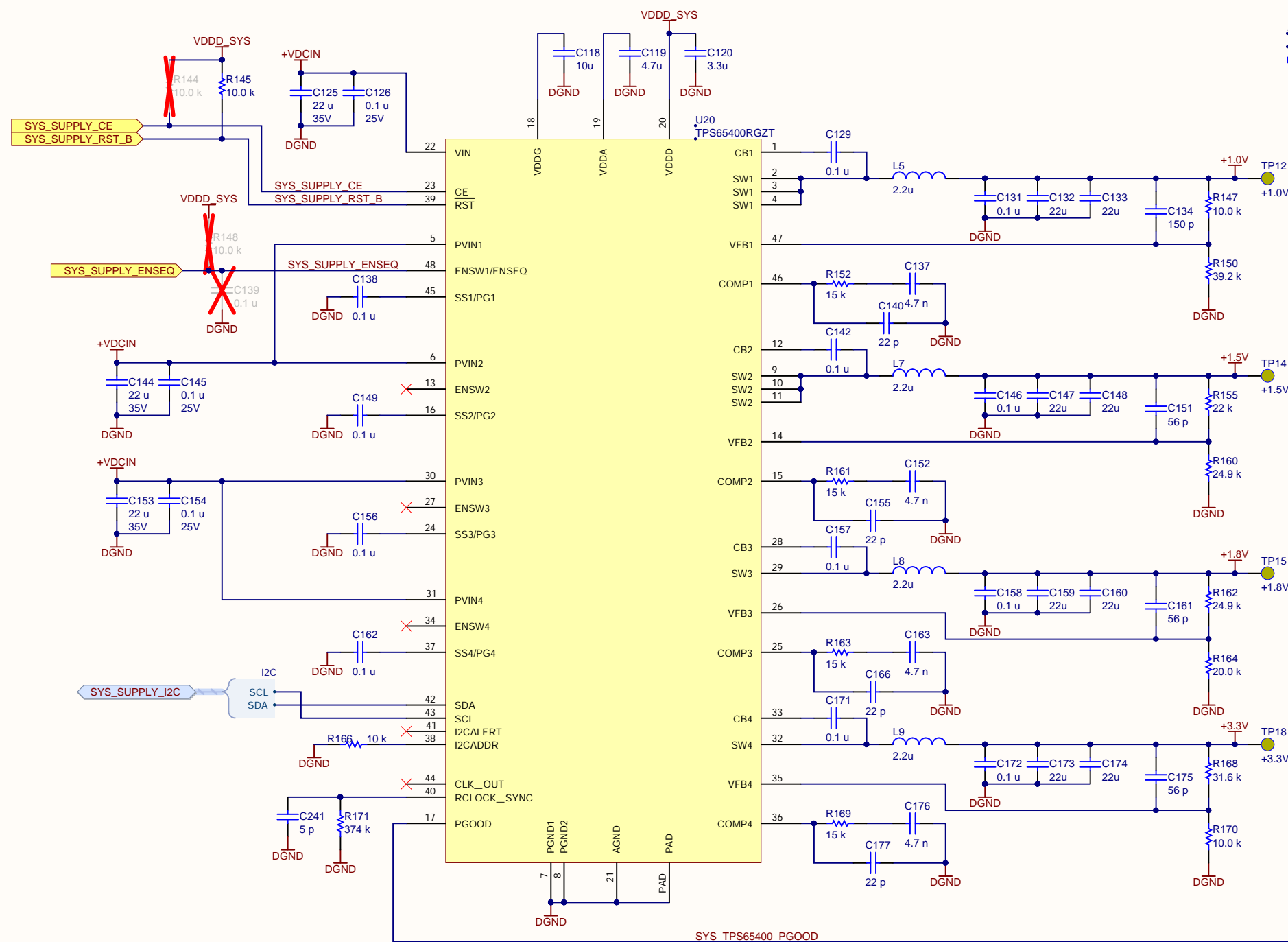
## PORT B (VIO2)



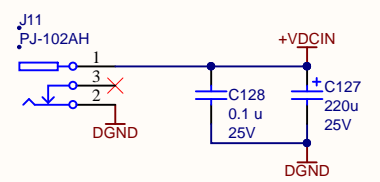
## PORT D (VIO2)



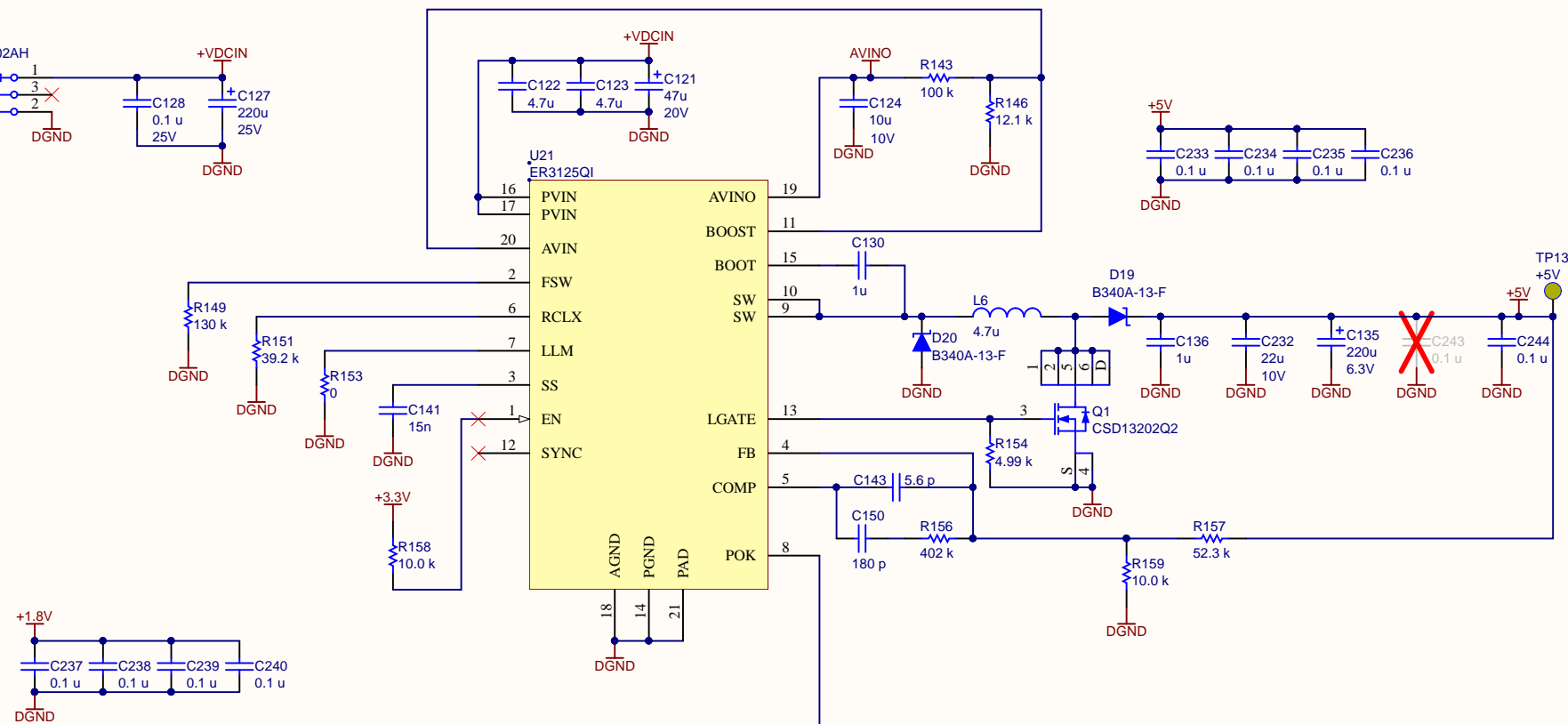
## System Supply



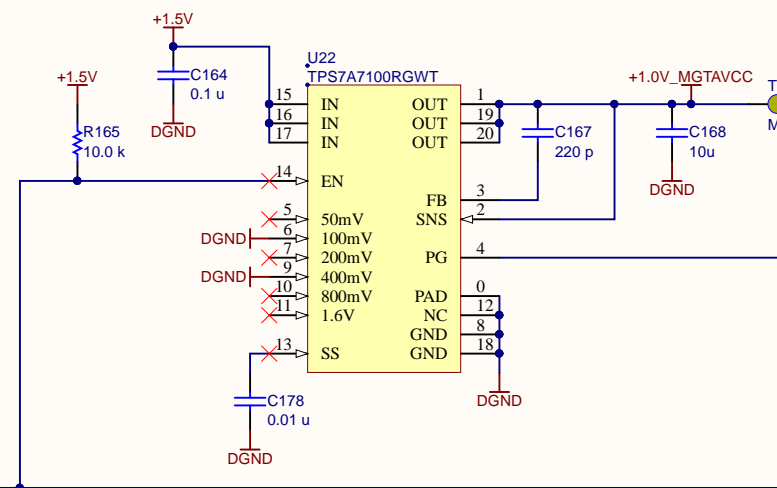
## DC Power Jack



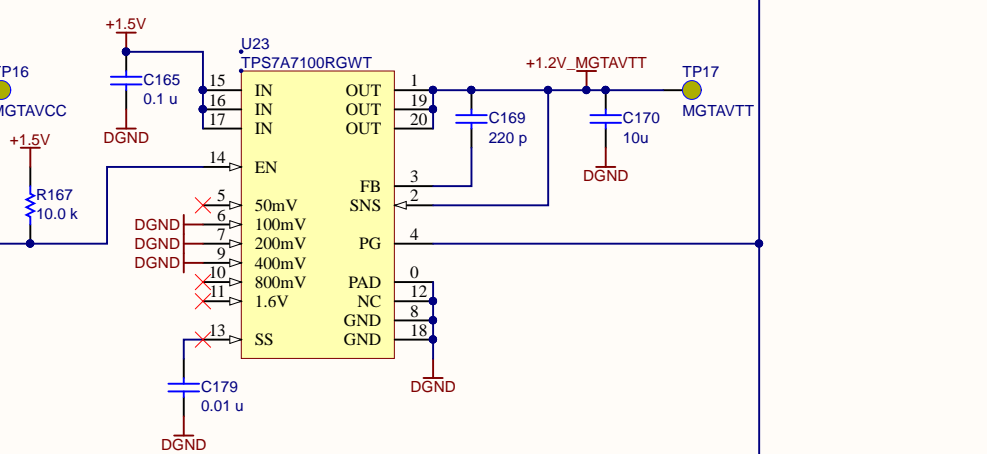
## +5V Buck-Boost



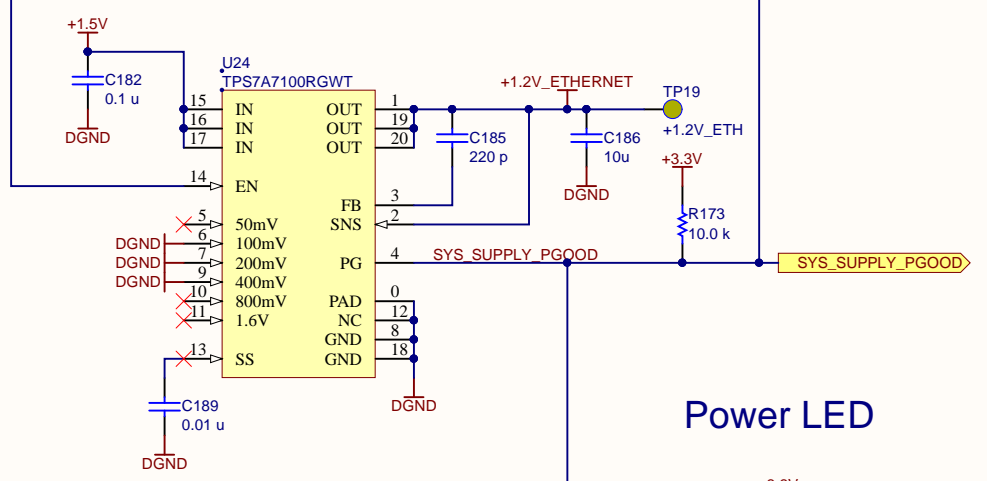
## +1.0V MGTAVCC LDO



## +1.2V MGTAVTT LDO



### +1.2V Ethernet PHY LDO



## Power LED

