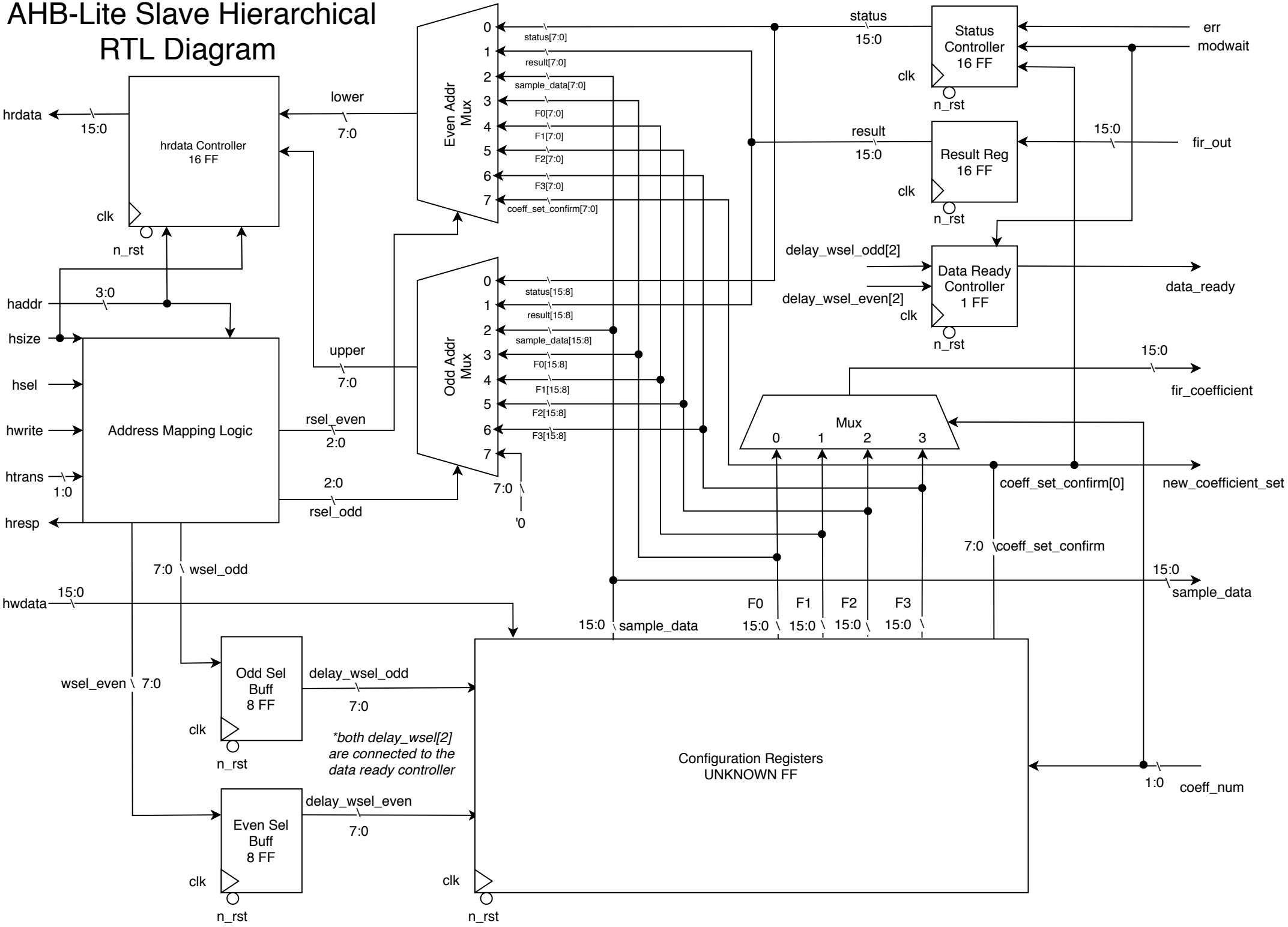
AHB-Lite Slave Hierarchical RTL Diagram

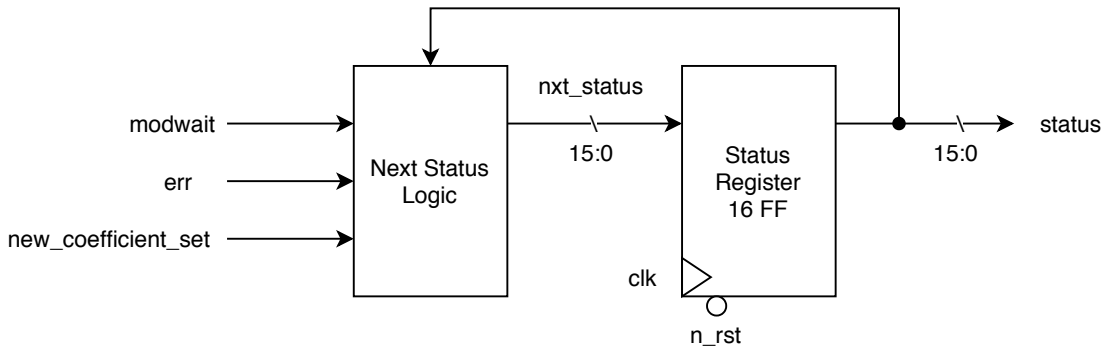


AHB-Lite Slave Hierarchical RTL Diagram

Address Mapping Logic

```
hresp = 0;
rsel_even = '0;
rsel_odd = '0;
wsel_even = '0;
wsel_odd = '0;
if (hsel && !hwrite && htrans == NON_SEQ) begin
    if (hsize == 0 && haddr == 4'hf)
        hresp = 1;
    else if (hsize == 1) begin
        rsel_even = haddr[3:1];
        rsel_odd = haddr[3:1];
    end
end
else if (hsel && hwrite && htrans == NON_SEQ) begin
    if (hsize == 0 && haddr == 4'hf || haddr < 4)
        hresp = 1;
    else if (haddr == 4'hf)
        wsel_even[haddr[3:1]] = 1;
    else if (hsize == 1) begin
        wsel_even[haddr[3:1]]= 1;
        wsel_odd[haddr[3:1]] = 1;
    end
    else if (hsize == 0 && haddr[0] == 0)
        wsel_even[haddr[3:1]] = 1;
    else if (hsize == 0 && haddr[0] == 1)
        wsel_odd[haddr[3:1]] = 1;
end
```

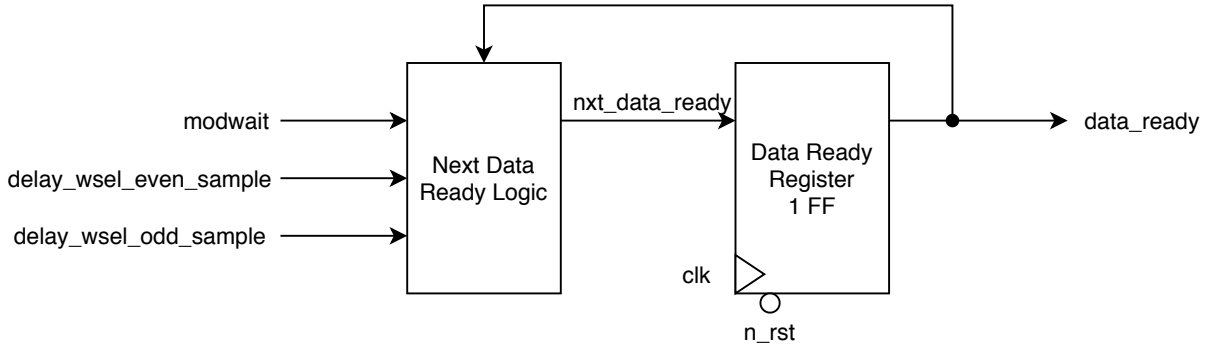
Status Controller (16 FF)



Next Status Logic

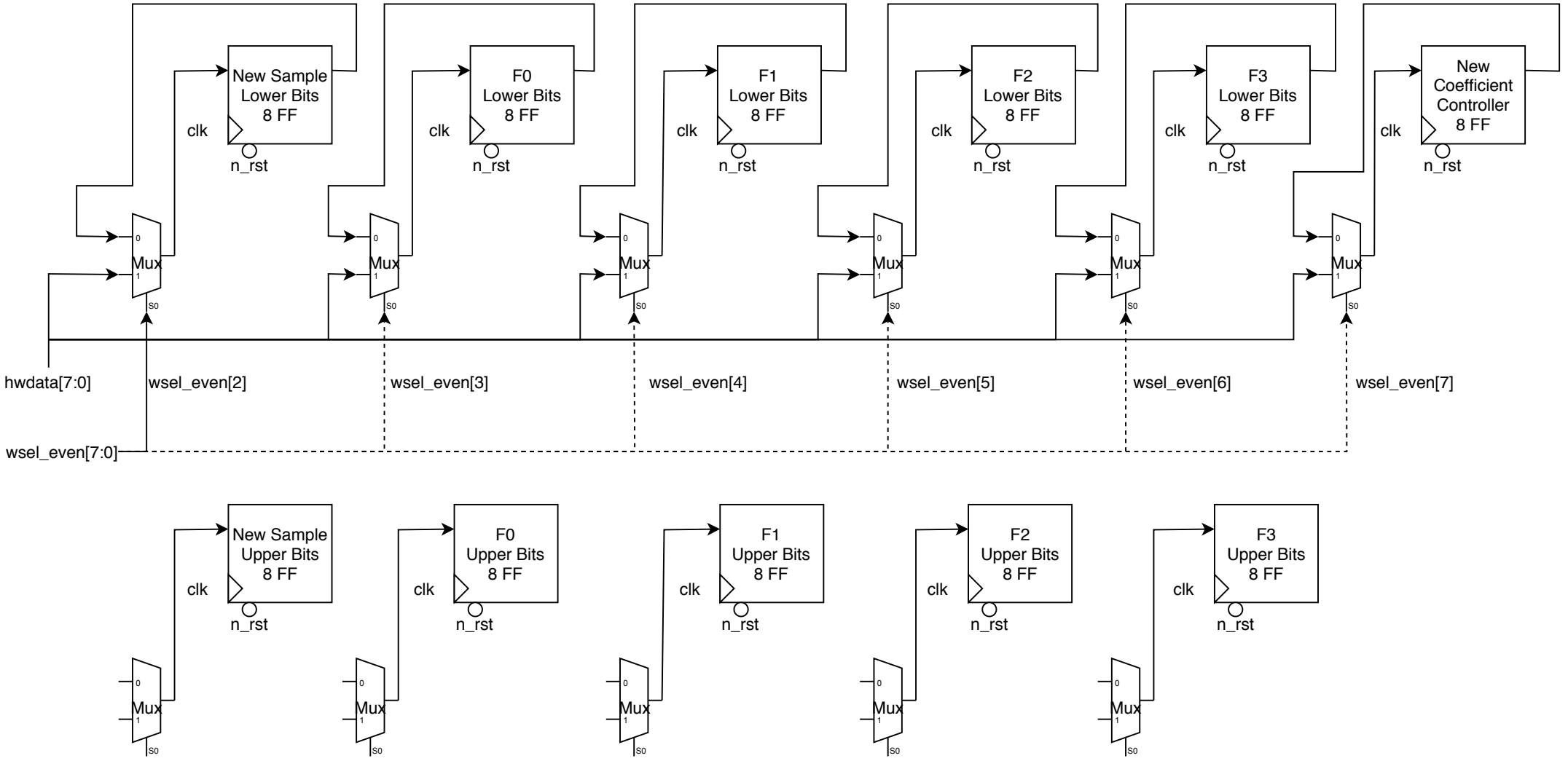
```
nxt_status = '0;
if (modwait || new_coefficient_set)
    nxt_status[0] = 1;
else if (err)
    nxt_status[8] = 1;
```

Data Ready Controller (1 FF)



Next Data Ready Logic

```
nxt_data_ready = data_ready;
if (delay_wsel_even_sample == 1 || delay_wsel_odd_sample == 1)
    nxt_data_ready = 1;
else if (modwait)
    nxt_data_ready = 0;
```



Configuration Registers