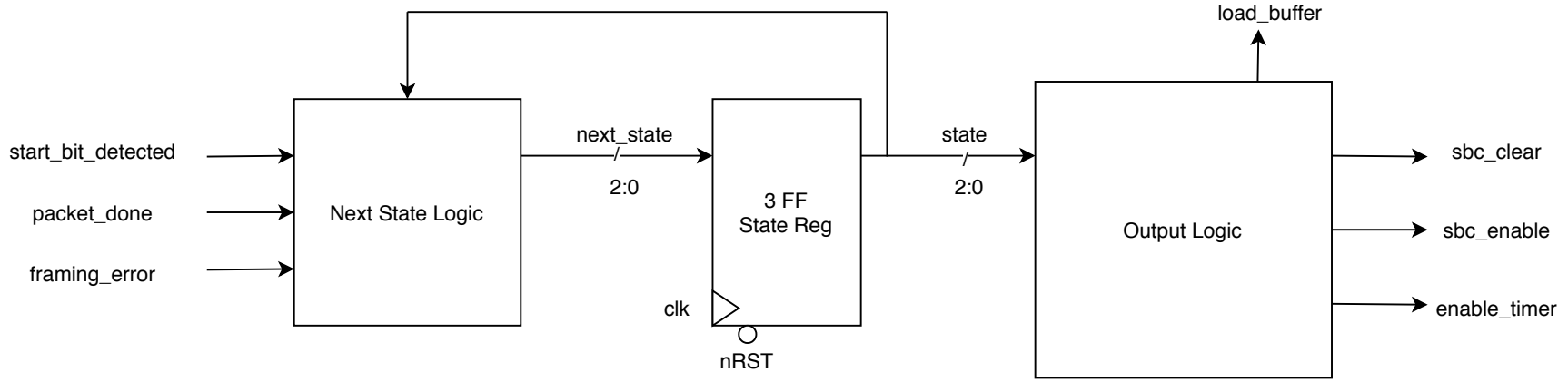
RCU RTL Diagram



NEXT STATE LOGIC

```
next_state = state;
case (state)
    IDLE:     if (start_bit_detected) next_state = CLEAR;
    CLEAR:    next_state = READ;
    READ:     if (packet_done) next_state = SBC_EN;
    SBC_EN:   next_state = CHCK_ERR;
    CHCK_ERR: if (framing_error) next_state = IDLE;
              else next_state = LOAD;
    LOAD:     next_state = IDLE;
    default:  next_state = IDLE;
endcase
```

OUTPUT LOGIC

```
load_buffer  = state == LOAD;
sbc_clear    = state == CLEAR;
sbc_enable   = state == SBC_EN;
enable_timer = (state == READ) ||
               (state == SBC_CLR);
```