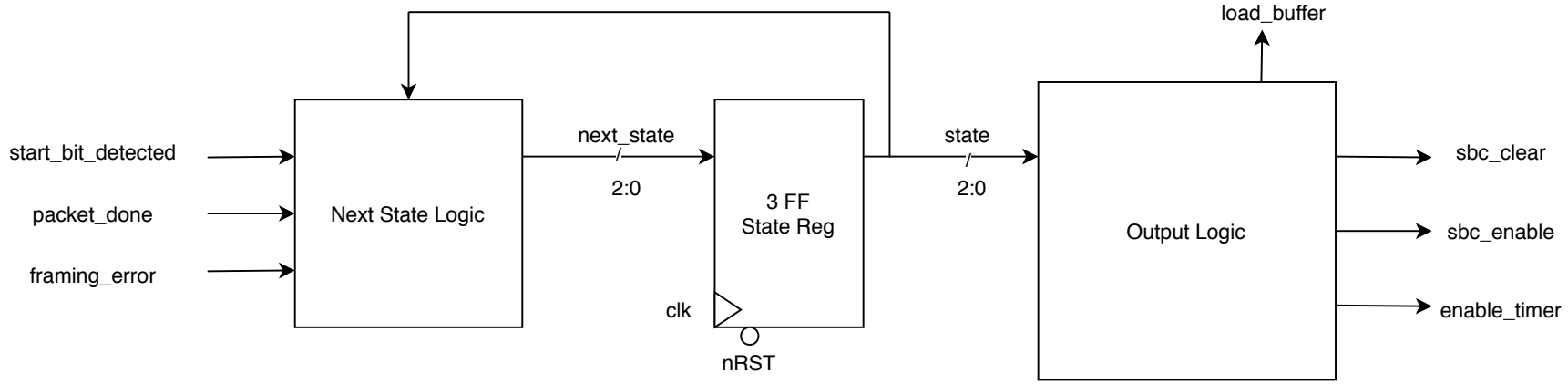
RCU RTL Diagram



NEXT STATE LOGIC

```
next_state = state;
case (state)
    IDLE:     if (start_bit_detected) next_state = CLEAR;
    CLEAR:    next_state = READ;
    READ:     if (packet_done) next_state = SBC_EN;
    SBC_EN:   next_state = CHCK_ERR;
    CHCK_ERR: if (framing_error) next_state = IDLE;
              else next_state = LOAD;
    LOAD:     next_state = IDLE;
    default:  next_state = IDLE;
endcase
```

OUTPUT LOGIC

```
sbc_clear = 0;
sbc_enable = 0;
enable_timer = 0;
load_buffer = 0;

case (state)
    CLEAR:    begin
              sbc_clear = 1;
              enable_timer = 1;
              end
    READ:     enable_timer = 1;
    SBC_EN:   sbc_enable = 1;
    LOAD:     load_buffer = 1;
endcase
```