FMCW Radar module in Self driving Cars

Basic Project Overview

Swadeshi Microprocessor Challenge

- Novel system development using
  - Shakti Processor (IIT Madras)
  - VEGA Processor (C-DAC)

- Choose the appropriate processor as per the application and augment with COTS (Commercial-off-the-shelf) components to build a prototype.

Shakti Microprocessors

- **Pinaka (E32-A35) and Parashu (E32-A100)** **[E-CLASS]**
  - These SoCs employ a 3 stage, 32-bit in-order E-class processor core
  - FPGA Board : Artix7-35T
  - Core has been completely developed using BSV (Bluespec System Verilog)
  - Designed for low power/area constraints
  - Suitable for smart-cards, IoT, Embedded platforms, motor-controls and robotic platforms, etc.
  - The SoCs include a wide variety of devices like: PWMs, SPIs, UARTs, I2Cs, GPIOs, XADC, Timers, PLICs, PMP
  - Pin Mux enabled and Arduino compatible

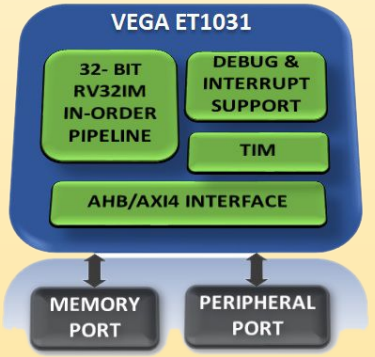
➔ Vajra (C64-A100): [C-CLASS]

- 64-bit, linux capable, 6-stage, in-order C-class processor core.
- FPGA Boards : Artix7-100T
- Core is implemented in Bluespec System Verilog (BSV)
- Features like branch predictors, caches, operand bypass, etc., thereby delivering substantial performance at minimal area/power overheads.
- Can be useful for high performance applications like networking, gateways, storage, etc.
- Targets compute/control applications in the 0.5-1.5 Ghz range.

VEGA Processors

➔ VEGA ET1031

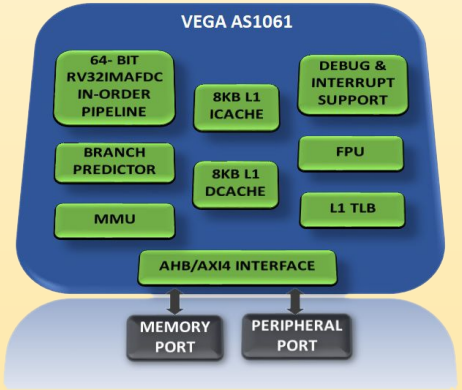
- 32 bit RISC-V (RV32IM) ISA, Linux Capable, 3-stage in-order pipeline
- FPGA Board - Artix7-35T
- Harvard architecture (separate instruction and data buses)
- High-performance multiply/divide unit (I-M extension)
- Configurable AXI4 or AHB external interface
- PLIC & Optional MPU
- Advanced Integrated Debug Controller



- **Applications like Sensor fusion, Remote sensor, Small IoT devices, Wearable devices etc.**

➔ VEGA AS1061

- a 64-bit processor, linux capable, 6-stage in-order pipeline optimized for high performance.
- Efficient branch predictor and Instruction & Data caches.
- The peripherals available are GPIO, Interrupt Controller, Timers, DDR3 RAM, SPI, UART, I2C, PWM, ADC and 10/100 Ethernet.
- FPGA Board - Artix7-100T
- Additional MMU and PMP Units
- Integer multiplication and division(I-M) and Atomic operation support(A)
- 16/32-bit mix instruction format for compacting code density
- **Applications like IoT devices, motor control, wearable devices, high-performance embedded, consumer electronics and industrial automation.**



FMCW Radar

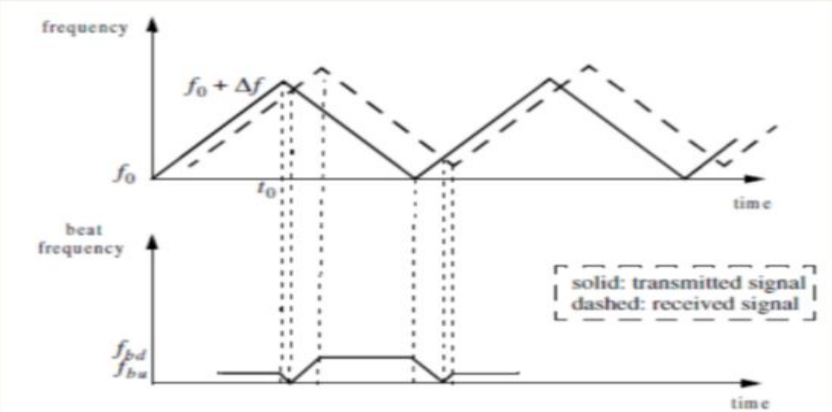


Figure 3.6. Transmited and received LFM signals and beat frequency, for a moving target.

$$f_{bu} = \frac{2R}{c}\dot{f} - \frac{2\dot{R}}{\lambda}$$

$$f_{bd} = \frac{2R}{c}\dot{f} + \frac{2\dot{R}}{\lambda}$$

Adding above two eqns., Range can be obtained

$$R = \frac{c}{4\dot{f}}(f_{bu} + f_{bd})$$

Subtracting above two eqns., Range rate can be obtained

$$\dot{R} = \frac{\lambda}{4}(f_{bd} - f_{bu})$$

Reference: *Mahafza, Bassem R, "Radar signal analysis and processing using MATLAB", CRC Press, 2016*

Transceiver Specs

Three FMCW transceivers

➔ **AWR1243**

- High performance, low power radar.
- 76 to 81-GHz coverage with 4 GHz available bandwidth(Chirp Bandwidth).
- Low noise.
- Four Receiver and Three Transmitter channels.
- Requires external clock(40 MHz) and ADC.
- Can act as LRR and MRR with maximum unambiguous range of 250m and 170m(approx.) respectively.

➔ AWR1642

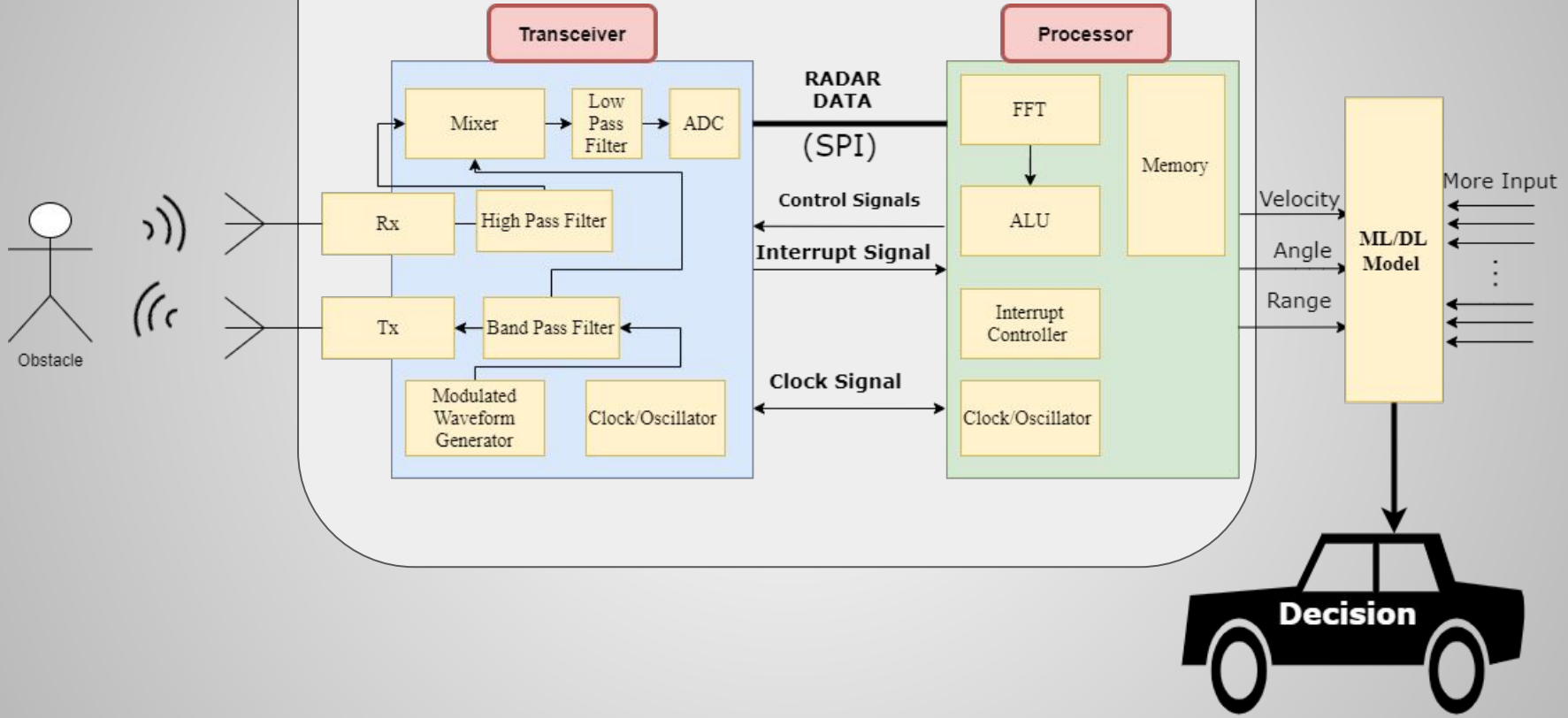
- Small, low power radar module in single chip.
- 76 to 81-GHz coverage with 4 GHz available bandwidth(Chirp Bandwidth).
- Low noise.
- Four Receiver and Two Transmitter channels.
- Requires external clock(40 MHz) and ADC.
- Can act as SRR and USRR with maximum unambiguous range of 250m and 170m(approx.) respectively.

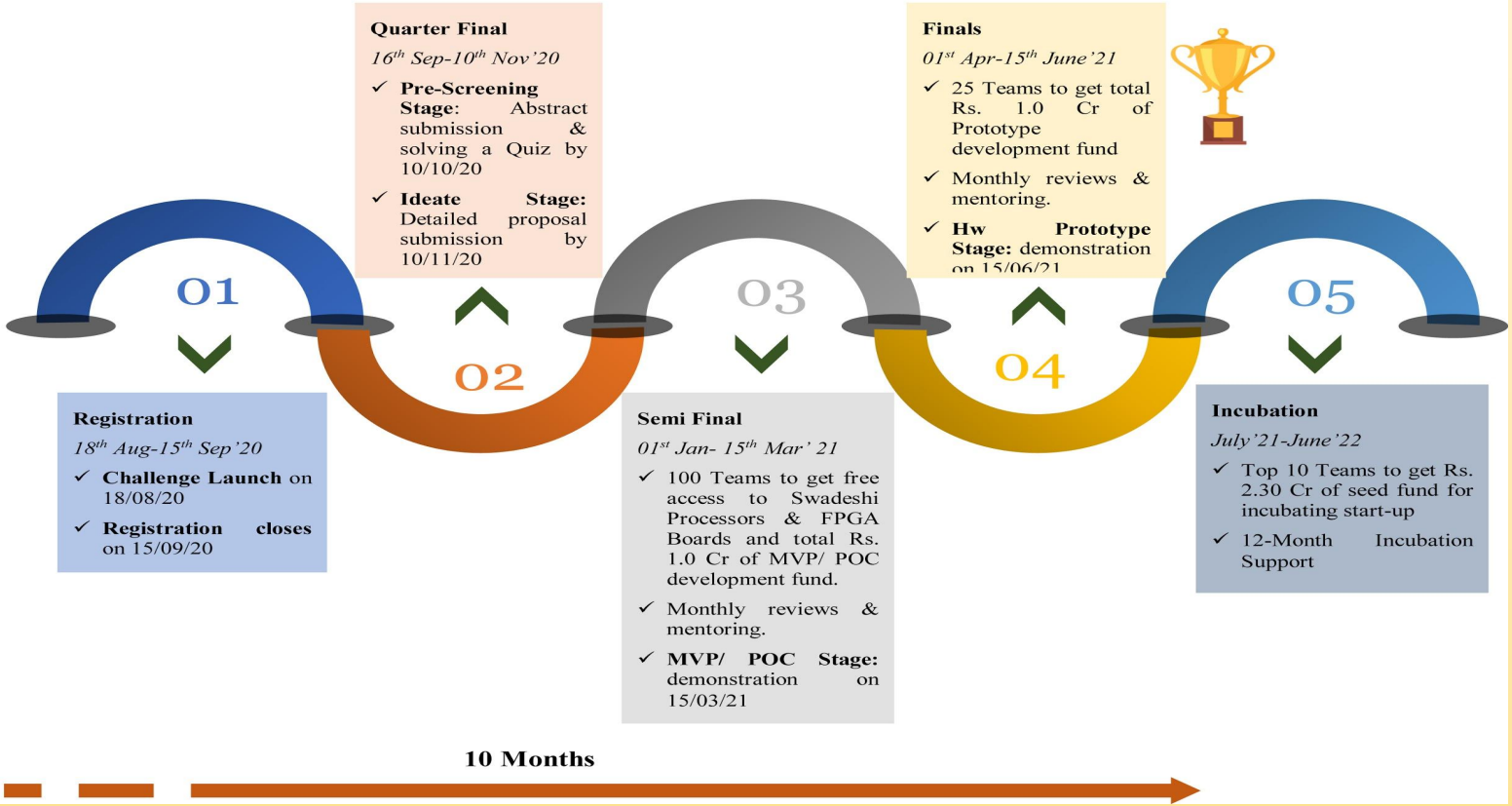
➔ TEF810X

- High performance, low power radar.
- 76 to 81-GHz coverage with 2 GHz available bandwidth(Chirp Bandwidth).
- Low noise(Lower compared to other two Transceiver).
- Four Receiver and Three Transmitter channels.
- Inbuilt clock(40 MHz) and ADC(gives digital output).
- Each receive chain contains programmable high-pass filters for suppression of strong low frequency signals.
- Can act as MRR,SRR,USRR with maximum unambiguous range of 200m, 80m and 20m(approx.) respectively.

High Level Block Diagram Overview

FMCW Radar module in Self driving Cars




01
Registration
18th Aug-15th Sep'20
✓ Challenge Launch on 18/08/20
✓ Registration closes on 15/09/20
02
Quarter Final
16th Sep-10th Nov'20
✓ Pre-Screening Stage: Abstract submission & solving a Quiz by 10/10/20
✓ Ideate Stage: Detailed proposal submission by 10/11/20
03
Semi Final
01st Jan- 15th Mar' 21
✓ 100 Teams to get free access to Swadeshi Processors & FPGA Boards and total Rs. 1.0 Cr of MVP/ POC development fund.
✓ Monthly reviews & mentoring.
✓ MVP/ POC Stage: demonstration on 15/03/21
04
Finals
01st Apr-15th June'21
✓ 25 Teams to get total Rs. 1.0 Cr of Prototype development fund
✓ Monthly reviews & mentoring.
✓ Hw Prototype Stage: demonstration on 15/06/21
05
Incubation
July'21-June'22
✓ Top 10 Teams to get Rs. 2.30 Cr of seed fund for incubating start-up
✓ 12-Month Incubation Support
10 Months

THANK YOU!

Team Members

1. Kothadiya Prince
2. Akash Ganguly
3. Sri Aditya Deevi
4. Aditya Amrit
5. Kshitij Singh