EE 16A HW 7

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I worked alone for 5 hours then met up with the other two to discuss our approaches to each problem.

2) a)

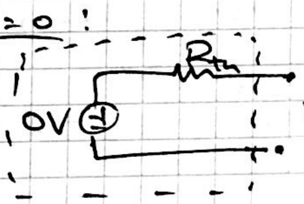
k	0	1	2	3
V_{DAC}	0 V	1 V	2 V	3 V

b)

k	0	1	2	3
V_{DAC}	0 V	$\frac{3}{5}$ V	$\frac{6}{5}$ V	3 V

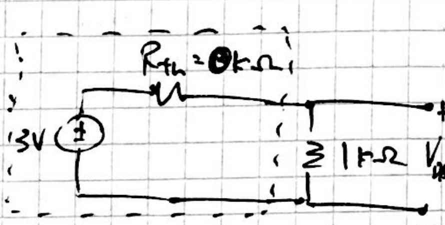
Thevenin Equivalents:

$k=0$:



$V_{DAC}=0$

$k=3$:



$V_{DAC}=3V$ for any R_{load}.

$k=1$:

V_{th}:

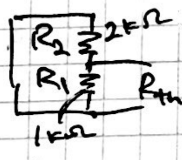
$V_{th}=1V$

$k=2$:

V_{th}:

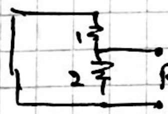
$V_{th}=2V$

R_{th}:

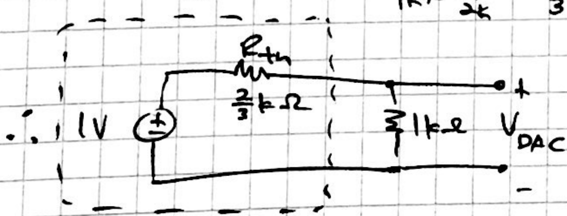


$R_{th} = (R_1 \| R_2) = \frac{1}{\frac{1}{1k}+\frac{1}{2k}} = \frac{2}{3}k\Omega$

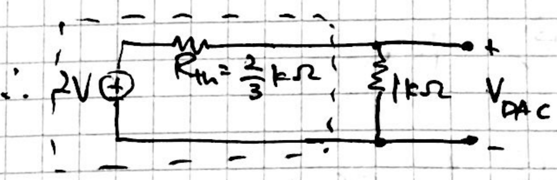
R_{th}:



$R_{th}=\frac{2}{3}k\Omega$



$V_{DAC}=\frac{1}{\frac{5}{3}}(1V)=\frac{3}{5}V$



$V_{DAC}=\frac{1}{\frac{5}{3}}(2V)=\frac{6}{5}V$

c) Only two entries ($k=1$ & $k=2$) are different those are the positions of a voltage divider. Because of this, R_{load} affects the ideal V_{DAC} @ only those places.

d) Since the R_{load} of $1k\Omega$ altered @ $k=1$ & $k=2$ (switches 1 & 2), first try modifying those circuits only.

Looking back @ my thevenin equivalents from part b), one way of achieving the ideal V_{DAC}'s is to modify the design so that $R_{th} \to 0$ (Case 1). Another way would be to modify the design so that the value of R_{load} becomes very large so that in the calculation for V_{DAC}, the R_{th} is negligible (Case 2).

Case 1 seems easily achievable if we assume that R_{load} will always be $1\,k\Omega$, for we can just modify so that R_{th} is just significantly smaller than $1\,k\Omega$ — to make the ratio of voltage divider $\left(\frac{R_{load}}{R_{load}+R_{th}}\right) \approx 1$.

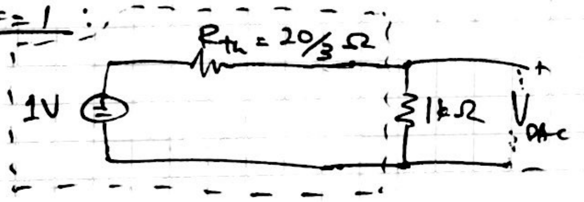
We can do this simply by setting the three $1k\Omega$ resistors in a series to $\boxed{10\,\Omega}$ (or anything small but equal to each other so that the voltage differences are kept).

When the three resistors are now 10Ω,

$$V_{DAC}\big|_{k=0} = 0V, \quad V_{DAC}\big|_{k=3} = 3V,$$

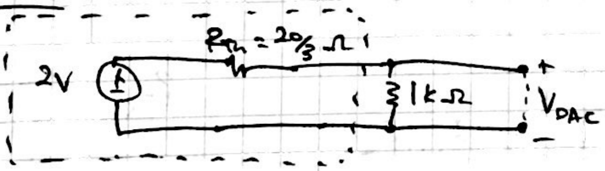
and the thevenin equivalents for $k=1$, $k=2$ are drawn like:

k=1 :



$$V_{DAC} = \frac{1k\Omega}{(1k\Omega + \frac{20}{3}\Omega)}(1V) \approx 1V$$

k=2 :



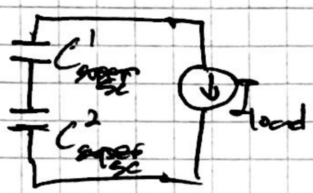
$$V_{DAC} = \frac{1k\Omega}{(1k\Omega + \frac{20}{3}\Omega)}(2V) \approx 2V$$

e) Nope

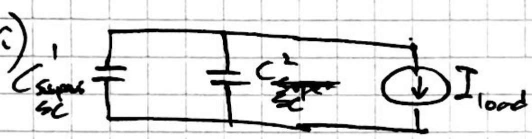
f) Nope.

3) a) i)

ii)



iii)



b) i) $Q_{sc} = C_{sc} V_{init} \rightarrow V_{init} = \frac{Q_{sc}}{C_{sc}}$

$$\boxed{\frac{dV}{dt} = \frac{1}{C_{sc}} \frac{dQ_{sc}}{dt} = \frac{-I_{load}}{C_{sc}}}$$

$$dV = \frac{-I_{load}}{C_{sc}} dt$$

$$\therefore V = \int_{t_0}^{t} dV = \int_{t_0}^{t} \frac{-I_{load}}{C_{sc}} dt = \frac{-I_{load}}{C_{sc}} t + V(t_0)$$

$$\therefore \boxed{V_1(t) = \frac{-I_{load}}{C_{sc}} t + V_{init}}$$

iii) Since C in parallel, $C_{eff} = 2C_{sc}$

$V_3(t)$ is just $\boxed{\frac{-I_{load}}{2C_{sc}} t + V_{init}}$

b) ii) $C_{eff} = \frac{C_{sc}^2}{2C_{sc}}$

$Q_{sc} = C_{eff} V_{init}$

$$V = \frac{Q_{sc}}{C_{eff}} \rightarrow \frac{dV}{dt} = -\frac{I_{load}}{C_{eff}} \rightarrow dV = -\frac{I_{load}}{C_{eff}} dt$$

$$V(t) = \int dV + V(0) = -\frac{I_{load}}{C_{eff}} dt + V_{init}$$

$$\therefore \boxed{V_2(t) = -\frac{2C_{sc} I_{load}}{C_{sc}^2} t + V_{init}} = -2\frac{I_{load}}{C_{sc}} t + V_{init}$$

c) i) $V_1(t) = V_{init} - \frac{I_{load}}{C_{sc}} t = V_{min} \rightarrow V_{init} - V_{min} = \frac{I_{load}}{C_{sc}} t$

$$\boxed{t = \frac{C_{sc}}{I_{load}} (V_{init} - V_{min})}$$

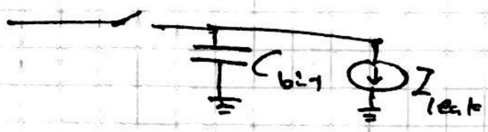
ii) $V_2(t) = V_{min}$: $\boxed{t = \frac{C_{sc}}{2I_{load}} (V_{init} - V_{min})}$

iii) $V_3(t) = V_{min}$: $\boxed{t = \frac{2C_{sc}}{I_{load}} (V_{init} - V_{min})}$

d) I pick Config 3, because its lifetime is longer than the others.

4) DRAM

a)



$Q_{init} = C_{bit} V_{init} = 18(10^{-15})(1.2) = \cancel{1.2}\ 21.6 \times 10^{-15}$

$Q_{min} = C_{bit} V_{min} = \cancel{0.8}\ 14.4 \times 10^{-15}$

$C_{bit} = 18 \times 10^{-15} F$

$V_{init} = 1.2\ V$

$V_{min} \geq 0.8\ V$

$V = \frac{Q_{init}}{C_{bit}} \rightarrow \frac{dV}{dt} = -\frac{I_{leak}}{C_{bit}} \rightarrow dV = -\frac{I_{leak}}{C_{bit}} dt$

$V(t) = V_{init} - \frac{I_{leak}}{C_{bit}} t$

$V(10^{-3} s) = V_{min}$

$V_{init} - \frac{I_{leak}}{C_{bit}} t \Big|_{10^{-3} s} = V_{min}$

$\cancel{1.2V} \ V_{init} - V_{min} = \frac{I_{leak}}{C_{bit}} t \rightarrow \cancel{t = \frac{C_{bit}}{I_{leak}}} (V_{init} - V_{min})$

$I_{leak} = \frac{C_{bit}}{t} (V_{init} - V_{min})$

$I_{leak} = 18 \times \frac{10^{-15} F}{10^{-3} s} (0.4 V)$

$I_{leak} = \cancel{4 \times 10^{-13}}\ A$

$\boxed{72 \times 10^{-12} A}$

b) 1024 DRAM CELLS :

$L_{col} = 1024 (0.5 \times 10^{-6} m)$, $H_{wire} = 0.5 \times 10^{-6} m$

$S = 0.1 \times 10^{-6} m$

$C = \frac{\varepsilon A}{d}$, $\varepsilon = 8.854 \times 10^{-12} \frac{F}{m}$, $A = L_{col} \times H_{wire}$

$\therefore C = \frac{(8.854 \times 10^{-12} \frac{F}{\cancel{m}})(1024)(0.5 \times \cancel{10^{-6} m})(0.5 \times 10^{-6} \cancel{m})}{0.1 \times \cancel{10^{-6} m}}$

$= \boxed{2.2666 \times 10^{-14} F} = 22.666\ fF$

4) c) Part 1: DRAM cell has 0 stored — $V_{bit} = 0V$

Since $Q_{bit} = C_{bit} \cancel{V_{bit}}^{0} = 0$,
no charge is present, and $\boxed{V_{column} = 0}$

Part 2: DRAM cell has a 1 stored — $V_{bit} = 1.2V$

$Q_{before} = Q_{after}$

$0 + V_{bit} C_{bit} = V_{col} C_{wire} + V_{col} C_{bit} = V_{col}(C_{wire} + C_{bit})$

$$V_{col} = \frac{C_{bit}}{C_{wire} + C_{bit}} V_{bit}$$

$$= \frac{(18 \times 10^{-15} \cancel{F})}{(20 \times 10^{-15} \cancel{F}) + (18 \times 10^{-15} \cancel{F})} \times (1.2V) = \boxed{0.5684 V}$$

d) Assuming $V_{bit} = 1.2V$,
the minimum V_{col} of $0.4V$ is achieved for some C_{wire}

$$C_{wire} = \frac{C_{bit} V_{bit}}{V_{col}} - C_{bit} = C_{bit}\left(\frac{V_{bit}}{V_{col}} - 1\right)$$

$$C_{wire} = (18 \times 10^{-15} F)\left(\frac{1.2 V}{0.4 V} - 1\right) = \cancel{9.02 \times} \; \cancel{522}\; 36 \; fF$$

$$C = \varepsilon \frac{A}{d} = \varepsilon \frac{H_{wire} \times L_{col}}{s}$$, where $H_{wire} = 0.5 \mu m$,
$s = 0.1 \mu m$,
$L_{col} = \#$ of DRAM cells $\times H_{wire}$,
$\varepsilon = 8.854 \times 10^{-12} \frac{F}{m}$

$$C = \varepsilon \frac{(H_{wire})^2 \, n}{s}$$

$$n = \frac{s \cdot C}{\varepsilon \cdot H_{wire}^2} = \frac{(0.1 \times 10^{-6} m)(\cancel{522}\; 36 \times 10^{-15} F)}{(8.854 \times 10^{-12} F/m)(0.5 \times 10^{-6} m)^2}$$

~~n = 11791.28 DRAM cells or 11791 cells~~

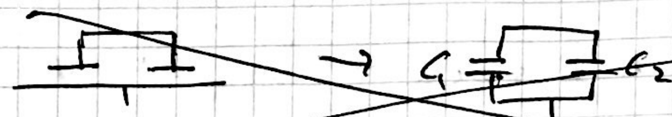
~~n = 23582.56 DRAM cells~~

$\boxed{n = 1626.38 \rightarrow 1626 \text{ DRAM cells}}$

5) MAG-LEV

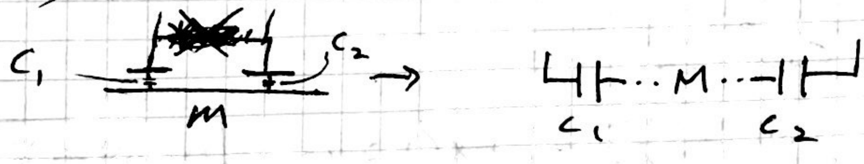
a) Btwn T_1 & M: $\boxed{C_1 = \varepsilon \frac{L_{train} \times W}{h}}$, $\varepsilon = 8.854 \times 10^{-12} \frac{F}{m}$

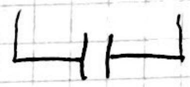
" T_2 & M : $\boxed{C_2 = \varepsilon \frac{L_{train} \times W}{h}}$, $C_1 = C_2$

b) 

$\cancel{C_{eff} = C_1 + C_2}$

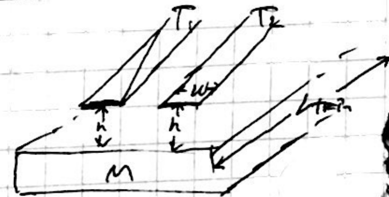
$\cancel{\boxed{C_{eff} = 2\varepsilon \frac{L_{train} \times W}{h}}}$





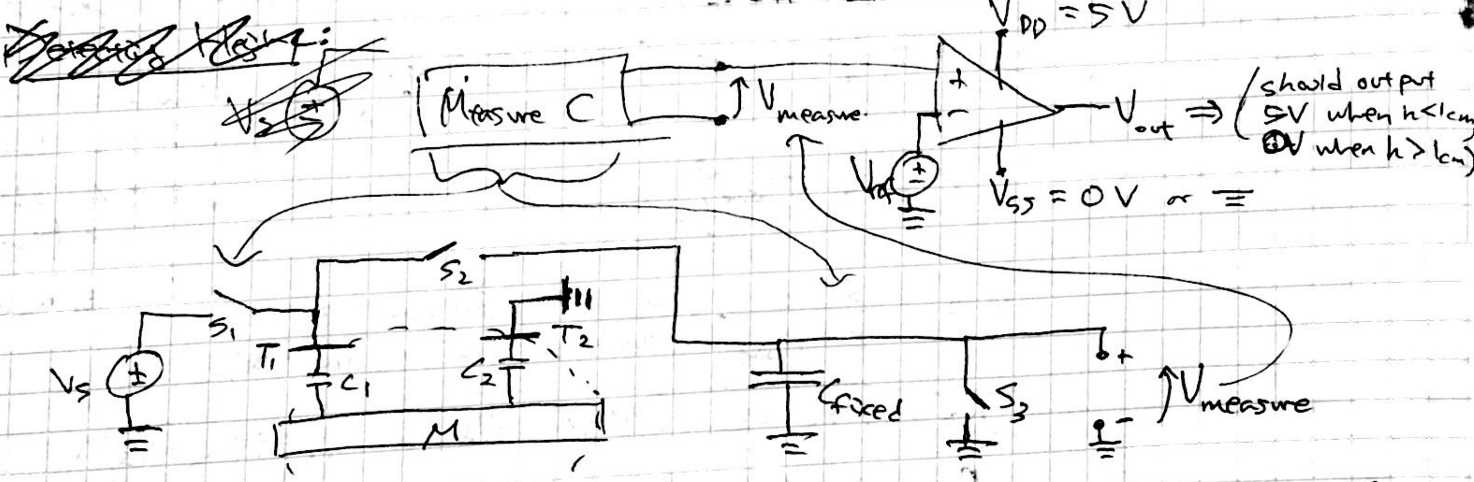
$C_{eff} = \frac{C_1 C_2}{C_1 + C_2}$

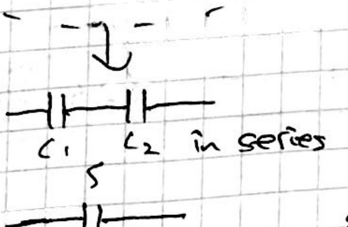
c) $C_{eff} = \dfrac{\frac{\cancel{\varepsilon^2} L_{train}^{\cancel{2}} W^{\cancel{2}}}{h^{\cancel{2}}}}{\frac{2\cancel{\varepsilon} \cancel{L_{train} \times W}}{\cancel{h}}} = \boxed{\frac{\varepsilon}{2} \frac{L_{train} \cdot W}{h}}$



d) 5V - Increase height
0V - Decrease height

$L_{train} = 100m$
$W = 0.01m$
$\therefore C_{eff} = \frac{\varepsilon}{2h}$





C_{eff}, where $C_{eff} = \frac{\varepsilon_0}{2h}$

meaning, bigger the h, smaller C_{eff}
and
smaller the h, bigger C_{eff}

Find V_{ref} s.t. h is @ the ideal height of 0.01 m:
@ h = 0.01 m, $C_{eff} = 50\varepsilon_0$

$\therefore \boxed{V_{ref} = \frac{C_{eff}}{C_{eff} + C_{fixed}} V_s}$, for any C_{fixed} and $C_{eff} = 50\varepsilon$ F
$= 4.42 \times 10^{-10}$ F

Redrawing with specific component parts, where we choose

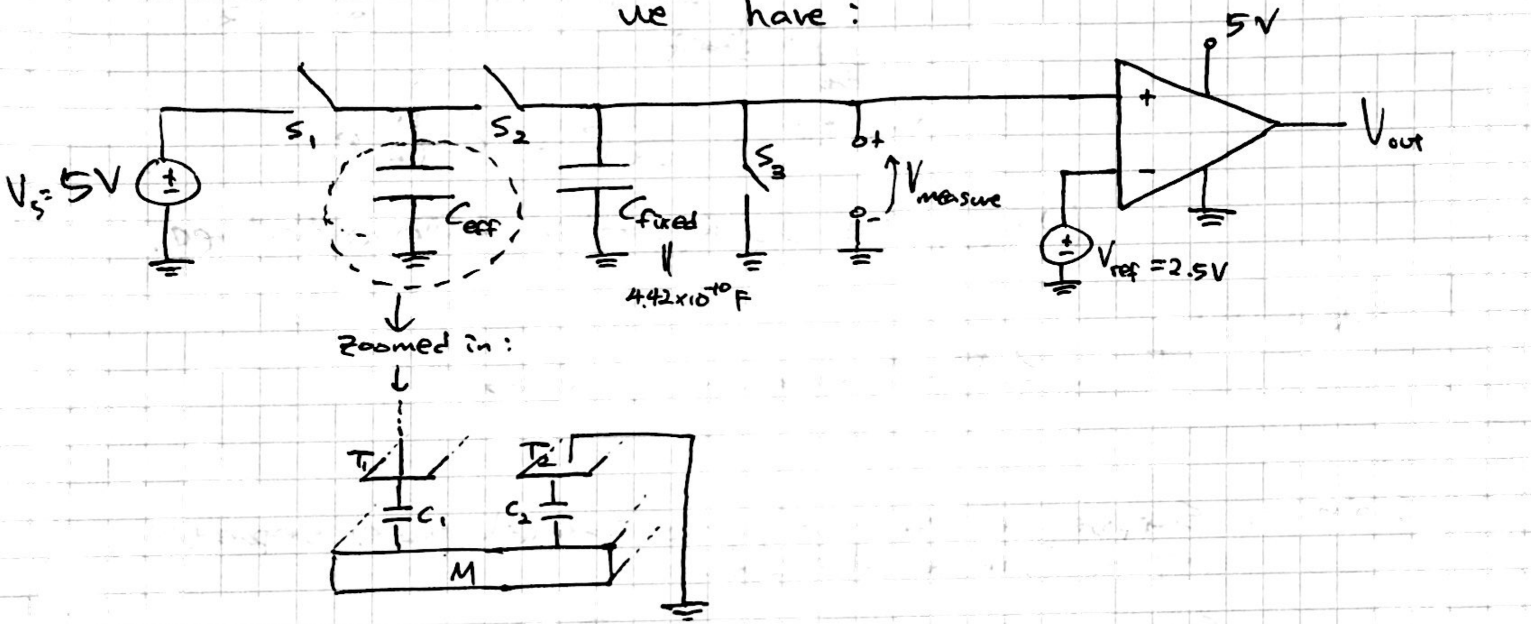
1) $C_{fixed} = 50\varepsilon F$ ($\approx 4.42\times10^{-10}$ F), something relatively similar in magnitude to C_{eff}, so that the ~~ent~~ different $V_{measure}$'s are noticeable.

2) $V_S = 5V$.

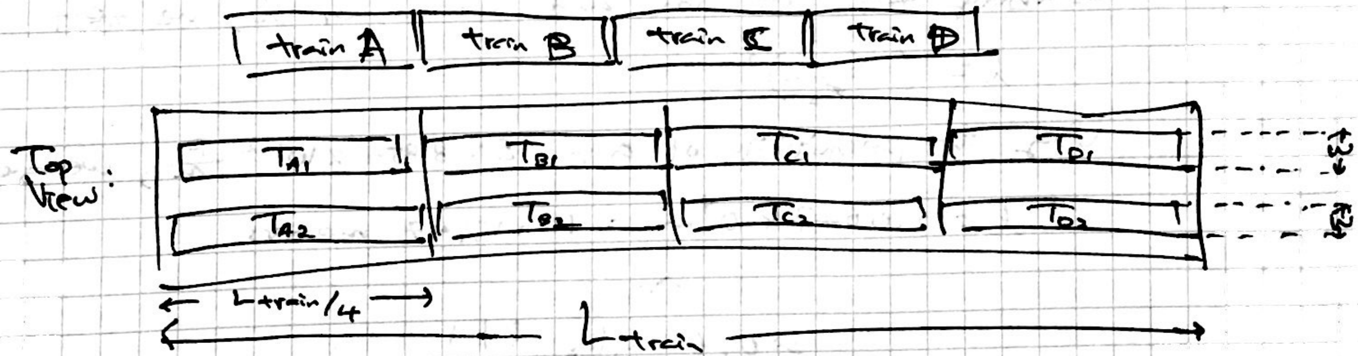
Then $V_{ref} = \left(\dfrac{C_{eff}|_{h=0.01m}}{C_{eff}|_{h=0.01m} + C_{fixed}} \right) V_S$

$$V_{ref} = \left(\frac{50\varepsilon F}{100\varepsilon F}\right)V_S = \frac{1}{2}V_S = 2.5V,$$

we have:



e) Separate T_1 & T_2 into 4 different trains.



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6) Question: Let there be a circuit consisting of a capacitor & a resistor. The capacitor is charged to an initial voltage V_{init} and has a capacitance of $C = 1\,F$. Find an expression for its voltage over time.

Solution: $Q = CV \rightarrow V = \frac{Q}{C}$.

$\frac{dV}{dt} = \frac{1}{C}\frac{dQ}{dt}$, since $I = \frac{dQ}{dt} = \cancel{\frac{V}{CR}}$

$V = IR = \frac{dQ}{dt}R = C\frac{dV}{dt}R$

Nope, not solving this differential eq.

New Q:

Is a 1 Farad capacitor reasonable?

Solution: Suppose we have two square parallel plates separated by a distance $d = 1\,mm$.

Capacitance is given by $C = \varepsilon \frac{A}{d}$.

For a square plate of length l, $A = l^2$.

Combining those relations and solving for l, we get

$$l = \left(\frac{Cd}{\varepsilon_0}\right)^{\frac{1}{2}}$$

Using the permittivity of air $\varepsilon = 8.854 \times 10^{-12}\,\frac{F}{m}$, we get

$$l = 1.0627 \times 10^{4}\,m = 10627.47 \text{ meters}$$

or

≈ 6.6 miles !!!

Very reasonable.