AX88178A

USB 2.0 to 10/100/1000M Gigabit Ethernet Controller

Features

Document No: AX88178A/V1.32/04/08/21

- Single chip USB 2.0 to 10/100/1000M Gigabit Ethernet controller with Energy Efficient Ethernet (EEE) base on digital signal processing (DSP) technology with low dissipation

- **USB Device Controller**
  - Integrates on-chip USB 2.0 PHY and controller compliant to USB Spec 2.0 and 1.1
  - Supports USB High/Full Speed modes with Bus-power or Self-power device auto-detect capability
  - High performance packet transfer rate over USB bus using proprietary burst transfer mechanism (US Patent Approval)

- **Gigabit Ethernet Controller**
  - Supports IEEE 802.3az (Energy Efficient Ethernet)
  - IEEE 802.3, 802.3u, and 802.3ab compatible
  - Integrates 10/100/1000Mbps Gigabit Ethernet MAC/PHY
  - Supports dynamic cable length detection and dynamic power adjustment Green Ethernet (Gigabit mode only)
  - Supports parallel detection and automatic polarity correction
  - Supports crossover detection and auto-correction
  - Supports IPv4/IPv6 packet Checksum Offload Engine (COE) to reduce CPU loading, including IPv4 IP/TCP/UDP/ICMP/IGMP & IPv6 TCP/UDP/ICMPv6 checksum check & generation
  - Supports TCP Large Send Offload V1
  - Supports full duplex operation with IEEE 802.3x flow control and half duplex operation with back-pressure flow control.
  - Supports IEEE 802.1P Layer 2 Priority Encoding and Decoding
  - Supports IEEE 802.1Q VLAN tagging and 2 VLAN ID filtering; received VLAN Tag (4 bytes) can be stripped off or preserved
  - Supports Jumbo frame up to 4KB
  - PHY loop-back diagnostic capability

- **Support Wake-on-LAN Function**
  - Supports suspend mode and remote wakeup via link-change, Magic Packet, Microsoft wakeup frame and external wakeup pin
  - Supports Bonjour wake-on-demand

- **Advanced Power Management Features**
  - Supports power management offload (ARP & NS)
  - Supports dynamic power management to reduce power dissipation during idle or light traffic
  - Supports AutoDetach power saving. Soft-disconnected from USB host when Ethernet cable is unplugged
  - Supports advanced link down power saving during Ethernet cable is unplugged

- Supports optional serial EEPROM (93c56/66) for storing USB Descriptors, Node-ID, etc

- Supports embedded eFuse (64-byte) to store USB Device Descriptors, Node-ID, etc. to save external EEPROM
- Supports automatic loading of USB Device Descriptors, Node-ID, etc. from embedded eFuse or external EEPROM after power-on initialization
- Single 25MHz clock input from either crystal or oscillator source
- Integrates on-chip power-on reset circuit
- Integrates pipelined RISC (System on a Chip, SoC) for handling protocol and control functions
- 68-pin QFN 8mm x 8mm RoHS/REACH compliant package
- Operating over 0°C to 70°C temperature range

Target Applications

- USB Dongle
- Docking Station
- USB Port Replicator
- Network Printer
- POS, Card Reader
- UMPC, MID, Netbook
- Ultrabook
- Game Console
- IP STB, IP TV
- Embedded system

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Released Date: 04/08/2021

Typical System Block Diagrams

- **Hosted by USB to operate with internal Ethernet PHY only**

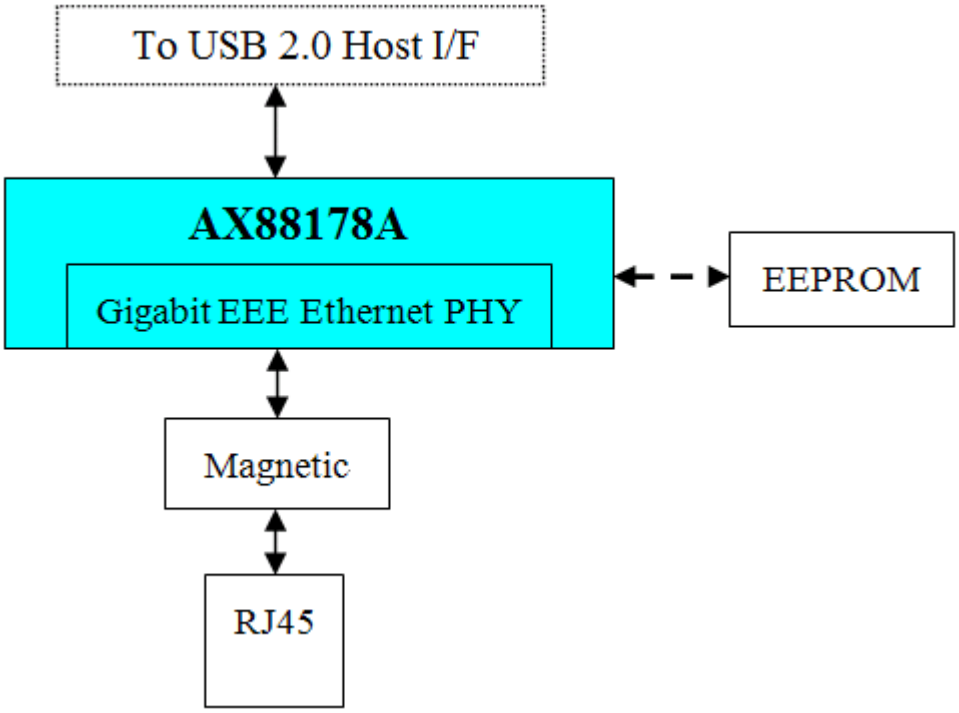

Figure 1 : USB 2.0 to Gigabit LAN Adaptor

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1 Introduction

1.1 General Description

The AX88178A USB 2.0 to 10/100/1000M Gigabit Ethernet controller is a high performance and highly integrated ASIC which enables low cost, small form factor, and simple plug-and-play Gigabit Ethernet network connection capability for desktops, notebook PC's, Ultrabook's, docking stations, game consoles, digital-home appliances, and any embedded system using a standard USB port.

The AX88178A features a USB interface to communicate with a USB Host Controller and is compliant with USB specification V2.0, and V1.1. It implements a 10/100/1000Mbps Ethernet LAN function based on IEEE802.3, IEEE802.3u, and IEEE802.3ab standards with embedded SRAMs for packet buffering. And, it also integrates an on-chip 10/100/1000Mbps EEE-compliant Ethernet PHY to simplify system design.

1.2 Block Diagram

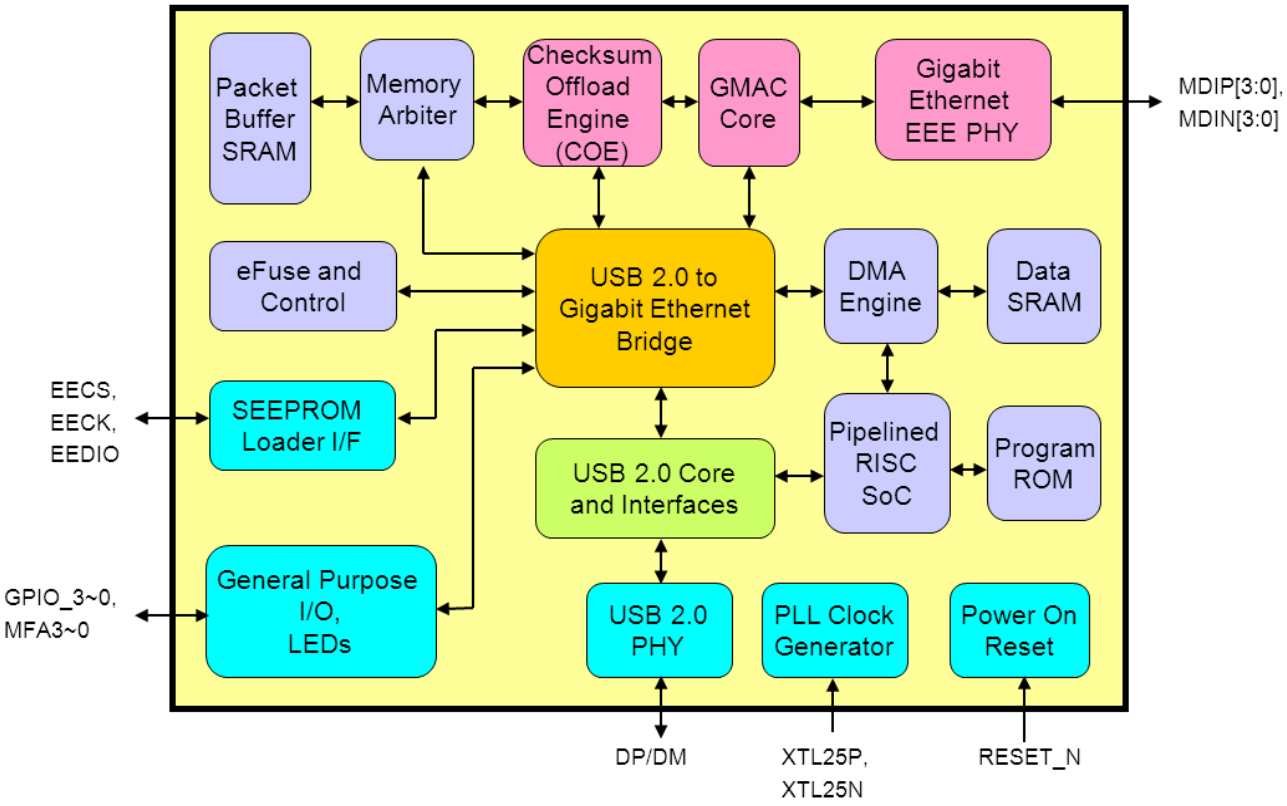


Figure 2 : Block Diagram

1.3 Pinout Diagram

- 68-pin QFN package

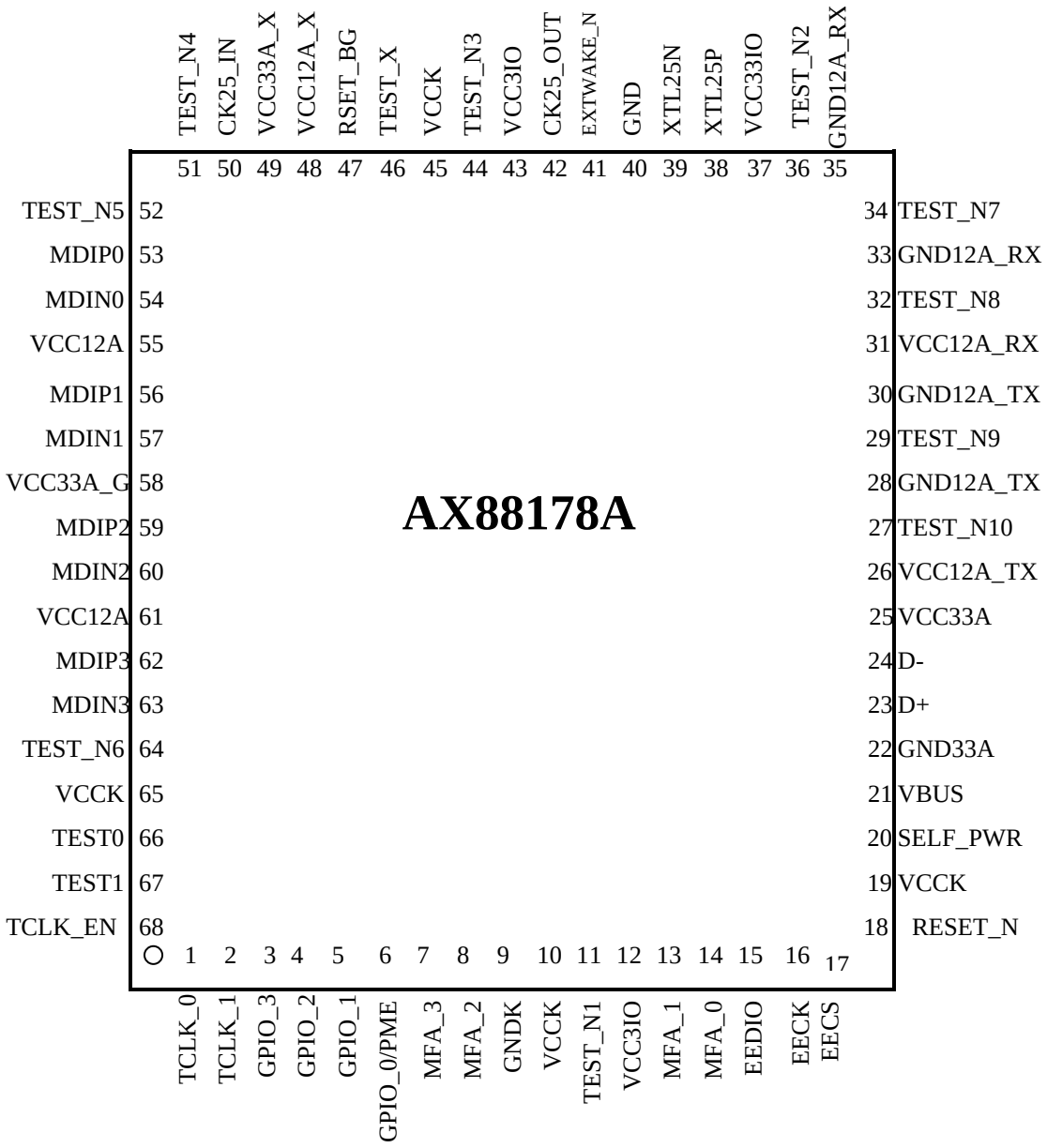


Figure 3 : Pinout Diagram

2 Signal Description

The following abbreviations apply to the following pin description table.

I12	**Input, 1.2V**	**AI**	**Analog Input**
I3	**Input, 3.3V**	**AO**	**Analog Output**
I5	**Input, 3.3V with 5V tolerant**	**AB**	**Analog Bi-directional I/O**
O3	**Output, 3.3V**	**PU**	**Internal Pull Up (75K ohm)**
B5	**Bi-directional I/O, 3.3V with 5V tolerant**	**PD**	**Internal Pull Down (75K ohm)**
B3	**Bi-directional I/O, 3.3V**	**S**	**Schmitt Trigger**
P	**Power/GND**	**T**	**Tri-stateable**

2.1 68-pin Pinout Description

Pin Name	Type	Pin No	Pin Description
USB Interface			
D+	AB	23	USB 2.0 data positive pin.
D-	AB	24	USB 2.0 data negative pin.
VBUS	I5/PD/S	21	VBUS pin input. Please connect to USB bus power.
Gigabit EEE Ethernet PHY Interface			
RSET_BG	AO	47	For Ethernet PHY's internal biasing. Please connect to GND through a 2.49Kohm ±1% resistor.
MDIP0	AB	53	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIN0	AB	54	
MDIP1	AB	56	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDIN1	AB	57	
MDIP2	AB	59	In MDI mode, this is the third pair in 1000Base-T, i.e., the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDIN2	AB	60	
MDIP3	AB	62	In MDI mode, this is the fourth pair in 1000Base-T, i.e., the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.
MDIN3	AB	63	
Clock Pins			
XTL25P	I3	38	25Mhz ± 0.005% crystal or oscillator clock input.
XTL25N	O3	39	25Mhz crystal or oscillator clock output.
CK25_OUT	O3	42	A controllable 25Mhz clock output. Please connect it to CK25_IN pin with a 22 Ohm termination resistor near to CK25_OUT pin.
CK25_IN	I3	50	25Mhz clock input. Please connect it to CK25_OUT pin with a 22 Ohm termination resistor.
Serial EEPROM Interface			
EECK	B5/PD/T	16	EEPROM Clock. EECK is an output clock to EEPROM to provide timing reference for the transfer of EECS, and EEDIO signals. EECK only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-down. Note: Please pull high this EECK signal on circuit for normal operation.
EECS	B5/PD/T	17	EEPROM Chip Select. EECS is asserted high synchronously with respect to rising edge of EECK as chip select signal. EECS only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-down.
EEDIO	B5/PU/T	15	EEPROM Data. EEDIO is the serial output data to EEPROM's data input pin and is synchronous with respect to the rising edge of EECK. EEDIO only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-up.
Misc. Pins			

RESET_N	I5/PU/S	18	Chip reset input. Active low. This is the external reset source used to reset this chip. This input feeds to the internal power-on reset circuitry, which provides the main reset source of this chip.
EXTWAKE_N	I3/PU/S	41	Remote-wakeup trigger from external pin. EXTWAKE_N should be asserted low for more than 2 cycles of 25MHz clock to be effective.
SELF_PWR	I5/PD/S	20	Self_power Indication Input. 0: will respond to Host that this device is a bus-power-device when Host query device. 1: will respond to Host that this device is a self-power-device when Host query device.
GPIO_3	B3/PD	3	General Purpose Input/ Output Pin 3.
GPIO_2	B3/PD	4	General Purpose Input/ Output Pin 2. Note that please keep this signal at logic '0' (pull down) during hardware reset for normal operation.
GPIO_1	B3/PD	5	General Purpose Input/ Output Pin 1. Please refer to section 2.2.
GPIO_0/PME	B3/PD	6	General Purpose Input/ Output Pin 0 or PME (Power Management Event). This pin is default as input pin after power-on reset. GPIO_0 also can be defined as PME output to indicate wake up event detected.
MFA_3	B3	7	It is a multi-function pin but can only work as a GPIO pin. Please refer to Table 2 for details.
MFA_2	B3	8	It is a multi-function pin. The default is an Ethernet PHY LED indicator (Link 10/100/1000+Active) and programmable. It also can be a GPIO pin. Please refer to Table 2 for details.
MFA_1	B3	13	It is a multi-function pin. The default is an Ethernet PHY LED indicator (Link 10/100/1000) and programmable. It also can be a GPIO pin. Please refer to Table 2 for details.
MFA_0	B3	14	It is a multi-function pin. The default is an Ethernet PHY LED indicator (Active) and programmable. It also can be a GPIO pin. Please refer to Table 2 for details.
TCLK_EN	I3/PD/S	68	Test pin. User can keep this pin NC.
TCLK_0	I3/PD	1	Test pin. User can keep this pin NC.
TCLK_1	I3/PD	2	Test pin. User can keep this pin NC.
TEST0	I3/S	66	Test pin. For normal operation, user should pull down this pin.
TEST1	I3/S	67	Test pin. For normal operation, user should pull down this pin.
TEST_X	I3	46	Test pin. For normal operation, user should pull down this pin.
TEST_N1, 2, 3, 4, 5, 6, 7, 8, 9, 10	O3	11, 36, 44, 51, 52, 64, 34, 32, 29, 27	Test pin. No connection
Power and Ground Pins			
VCC33A	P	25	Analog Power for USB transceiver. 3.3V.
GND33A	P	22	Analog Ground for USB transceiver.
VCC12A_TX	P	26	Analog Power for USB transceiver. 1.2V.
GND12A_TX	P	28,30	Analog Ground for USB transceiver.
VCC12A_RX	P	31	Analog Power for USB transceiver. 1.2V.
GND12A_RX	P	33,35	Analog Ground for USB transceiver.
VCC12A_X	P	48	Analog Power for Ethernet PHY. 1.2V.
VCC33A_X	P	49	Analog Power for Ethernet PHY. 3.3V.
VCC12A	P	55,61	Analog Power for Ethernet PHY. 1.2V.
VCC33A_G	P	58	Analog Power for Ethernet PHY. 3.3V.
VCC33IO	P	37	Digital I/O Power for Clock pins. 3.3V.
GND	P	40	Digital Ground for clock pins.
VCCK	P	10, 19, 45, 65	Digital Core Power. 1.2V.
GNDK	P	9	Digital Ground to E-pad
VCC3IO	P	12, 43	Digital I/O Power. 3.3V.

Table 1 : Pinout Description

2.2 Hardware Setting For Operation Mode and Multi-Function Pins

The following hardware settings define the desired operation mode and some multi-function pins. The logic level shown on setting pin below is loaded from the chip I/O pins during power on reset based on the setting of the pin's pulled-up (as logic '1') or pulled-down (as logic '0') resister on the schematic.

- EEPROM Offset 05h or eFuse Offset 18h, Flag[4]: Defines the multi-function pin GPIO_0 / PME

GPIO_0 is a general purpose I/O normally controlled by vendor commands. Users can change this pin to operate as a PME (Power Management Event) for remote wake up purpose. Please refer to Section 4.1.2 "Flag" of bit 4 (PME_PIN).

- GPIO_1 pin: Determines whether this chip will go to Default WOL Ready Mode after power on reset. The WOL stands for Wake-On-LAN.

GPIO_1	Description
0	Normal operation mode (default, see Note 1).
1	Enable Default WOL Ready Mode. Notice that the external pulled-up resistor must be 4.7Kohm. For more details, please refer to APPENDIX A. Default Wake-On-LAN (WOL) Ready Mode

Note 1: This is the default with internal pulled-down resistor and doesn't need an external one.

- MFA_3 ~ MFA_0 pins: There are 4 multi-function pins. The MFA_2 ~ MFA_0 support the LED indication or GPIO functionality, but the MFA_3 only supports the GPIO functionality that can be controlled by vendor command PIN Control Register MFA_EN.

PIN Name	Default definition	Section 4.1.5	MFA Control Register
MFA_3	-	-	MFAIO_3
MFA_2	Programmable LED (Link 10/100/1000+Active)	LED_2	MFAIO_2
MFA_1	Programmable LED (Link 10/100/1000)	LED_1	MFAIO_1
MFA_0	Programmable LED (Active)	LED_0	MFAIO_0

Table 2 : MFA_3 ~ MFA_0 pin configuration

3 Function Description

3.1 USB Core and Interfaces

The USB core and interfaces contains USB 2.0 transceiver interface (UTMI) and a USB 2.0 SIE
The USB 2.0 transceiver (or PHY) processes USB 2.0/1.1 Physical layer signals. And, the USB 2.0 SIE is interfacing with USB 2.0 transceiver by UTMI bus and it processes USB packets. Also, The USB 2.0 SIE contains Bulk IN and Bulk OUT buffers for handling Bulk transfer traffic, a FIFO for Interrupt IN transfers, and control transfer handling.

The USB core and interfaces are used to communicate with a USB host controller and is compliant with USB specification V2.0, and V1.1.

3.2 Energy Efficient Ethernet (EEE)

It supports IEEE 802.3az also known as Energy Efficient Ethernet (EEE) at 10Mbps, 100Mbps and 1000Mbps. And also supports EEE specified a negotiation method to enable link partner to determine whether EEE is supported and to select the best set of parameters common to both device. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode, most of the circuits are disabled; however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

3.3 10/100/1000M Ethernet PHY

The 10/100/1000M Ethernet PHY is compliant with 10Base-T, 100Base-TX, and 1000Base-T IEEE 802.3 standards. It provides all the necessary physical layer functions to transmit and receive Ethernet packets over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. It uses state-of-the-art DSP technology and an Analog Front End (AFE) to enable high-speed data transmission and reception over UTP cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented.

3.4 GMAC Core

The MAC core supports IEEE 802.3, IEEE 802.3u and IEEE 802.3ab MAC sub-layer functions, such as basic MAC frame receive and transmit, CRC checking and generation, filtering, forwarding, flow-control in full-duplex mode, and collision-detection and handling in half-duplex mode, etc. It supports virtual local area network (VLAN)-tagged frames according to IEEE 802.1Q specification in both transmit and receive functions, CRC-32 checking at full speed using a multi-stage, cyclic redundancy code (CRC) calculation architecture with optional forwarding of the frame check sequence (FCS) field to the user application CRC-32 generation and append on transmit.

3.5 Checksum Offload Engine (COE)

The Checksum Offload Engine (COE) supports IPv4, IPv6, layer 4 (TCP, UDP, ICMP, ICMPv6 and IGMP) header processing functions and real time checksum calculation in hardware

The COE supports the following features in layer 3:

- IP header parsing, including IPv4 and IPv6
- IPv6 routing header type 0 supported
- IPv4 header checksum check and generation (There is no checksum field in IPv6 header)
- Detecting on RX direction for IP packets with error header checksum

The COE supports the following features in layer 4:

- TCP and UDP checksum check and generation for non-fragmented packet
- TCP Large Send Offload V1
- ICMP, ICMPv6 and IGMP message checksum check and generation for non-fragmented packet

3.6 Memory Arbiter

The memory arbiter block is responsible for storing received MAC frames into on-chip SRAM (packet buffer) and then forwarding it to the USB bus upon request from the USB host via Bulk IN transfer. It also monitors the packet buffer usage in full-duplex mode for triggering PAUSE frame (or in half-duplex mode to activate Backpressure jam signal) transmission out on transmit (TX) direction. The memory arbiter block is also responsible for storing MAC frames received from the USB host via Bulk OUT transfer and scheduling transmission out towards Ethernet network.

3.7 USB to Ethernet Bridge

The USB to Ethernet bridge block is responsible for converting Ethernet MAC frame into USB packets or vice-versa. This block supports proprietary burst transfer mechanism (US Patent Approval) to offload software burden and to offer very high packet transfer throughput over USB bus.

This USB to Ethernet bridge block not only co-work with “eFuse and Control”, “SEEPROM Loader I/F”, and General Purpose I/Os and LEDs, but also handle USB Control transfers of Endpoint 0.

3.8 eFuse and Control

The eFuse (64-byte) and Control supports user to program USB descriptions and some device information. The data format is shown at Section 4.

3.9 SEEPROM Loader Interface

The SEEPROM loader interface is responsible for reading configuration data automatically from the external serial EEPROM or eFuse after power-on reset.

If the content of EEPROM offset 05h (low byte) was equal to (0xFF - SUM [EEPROM offset 03h ~ 04h]), the EEPROM is the first candidate for SEEEPROM loader. If failed checksum checking the eFuse will be the second candidate.

If this SEEPROM Loader checks the 1st byte data of efuse is not equal to 0xFF and the eFuse Checksum [7:0] of eFuse offset 19h is correct, the content of eFuse is valid for SEEPROM loader. If eFuse Checksum [7:0] is incorrect, the chip’s internal default setting will be brought up to configure the corresponding valus and respond to USB standard commands, etc.

3.10 General Purpose I/O and LED

There are 4 general-purpose I/O pins (named GPIO_0/1/2/3) and 4 multi-function pins group A (named MFA_0/1/2/3) provided by this chip. The MFA_0/1/2 pins are also used for LED indication. Please refer to Section 4.1.5 for details.

3.11 PLL Clock Generator

The AX88178A integrates internal oscillator circuits for 25 MHz, respectively, which allow the chip to operate cost effectively with just external 25 MHz crystals.

The external 25 MHz crystal or oscillator, via pins XTL25P/XTL25N, provides the reference clock to internal oscillation circuit to generate clock source for the embedded Ethernet PHY, embedded USB PHY, and base clock for ASIC use.

The external 25MHz Crystal spec is listed in below table. For more details on crystal timing, please refer to Section 6.5.1 "Clock Timing" and AX88178A demo board reference schematic.

Parameter	Symbol	Typical Value
Nominal Frequency	Fo	25.000000MHz
Oscillation Mode		Fundamental
Frequency Tolerance (@25℃)		±30ppm
Frequency Stability Over Operating Temperature Range		±30ppm
Equivalent Series Resistance	ESR	70 Ohm max.
Load Capacitance	CL	12pF
Drive Level		350uW
Operation Temperature Range		0℃ ~ +70℃
Aging		±3ppm/year

Table 3 : The external 25MHz Crystal Units specifications

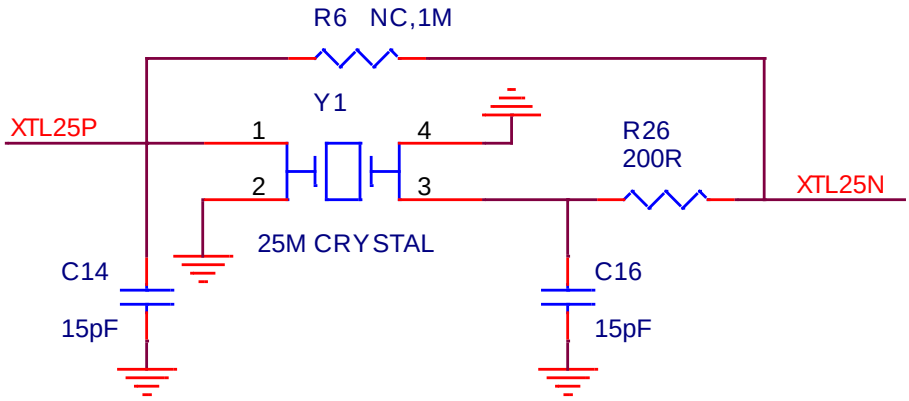


Figure 4 : 25MHz Crystal Reference Circuit

3.12 Reset Generation

The AX88178A integrates an internal power-on-reset circuit, which can simplify the external reset circuitry on PCB design. The power-on-reset circuit generates a reset pulse to reset chip logic after 1.2V core power ramping up to 0.72V (typical threshold). The external hardware reset input pin, RESET_N, is fed directly to the input of the power-on-reset circuit and can also be used as additional hardware reset source to reset the system logic. For more details on RESET_N timing, please refer to Reset Timing

.

4 Serial EEPROM/eFuse Memory Map

EEPROM OFFSET	HIGH BYTE	LOW BYTE
00h	Node ID 1	Node ID 0 (Note_1)
01h	Node ID 3	Node ID 2
02h	Node ID 5	Node ID 4
03h	PID_HB	PID_LB
04h	VID_HB	VID_LB
05h	Flag	EEPROM Checksum (Note_2)
06h	Reserved	Reserved
07h	Max. Power for Self Power	Max. Power for Bus Power
08h	EndPoint1 for HS	EndPoint1 for FS
09h	Language ID High Byte	Language ID Low Byte
0Ah	Length of Product String (bytes)	Offset of Product String (0Eh)
0Bh	Length of Manufacturer String (bytes)	Offset of Manufacturer String (1Ah)
0Ch	Length of Serial Number String (bytes)	Offset of Serial Number String (26h)
0Dh	Reserved	
19~0Eh	Product String: (Max.) 24 bytes	
25~1Ah	Manufacturer String: (Max.) 24 bytes	
2C~26h	Serial Number String: (Max.) 14 bytes	
3C~2Dh	Reserved	
41~3Dh	Fixed_pattern (10 bytes)	
42h	LED_Mode_HB	LED_Mode_LB

Table 4 : Serial EEPROM Memory Map

Note_1: The Node ID 0 value cannot be set to 0xFF and 1st bit of Node ID 0 can not be set to "1" (i.e. cannot be set to multicast MAC address).

Note_2: The value of EEPROM Checksum field located at EEPROM offset 05h (low byte). The correct value must be equal to (0xFF - SUM [EEPROM offset 03h ~ 04h]). If SUM [EEPROM offset 03h ~ 04h] has carry, please add '1' to its result.

Note_3: Total usage is about 134 bytes.

eFuse OFFSET	HIGH BYTE	LOW BYTE
00h	Node ID 1	Node ID 0 (Note_1)
01h	Node ID 3	Node ID 2
02h	Node ID 5	Node ID 4
03h	PID_HB	PID_LB
04h	VID_HB	VID_LB
05h	Reserved	Max. Power for Bus Power
06h	EndPoint1 for HS	EndPoint1 for FS
07h	Language ID High Byte	Language ID Low Byte
08h	Length of Product String (bytes)	Offset of Product String (0Bh)
09h	Length of Manufacturer String (bytes)	Offset of Manufacturer String (11h)
0Ah	Reserved	Reserved
10~0Bh	Product String: (Max.) 12 bytes	
15~11h	Manufacturer String: (Max.) 10 bytes	
17~16h	Reserved	
18h	Flag	Reserved
19h	LED_Mode_LB	eFuse Checksum[7:0] (Note_2)
1Ah	Fixed_pattern (First byte)	LED_Mode_HB
1E~1Bh	Fixed_pattern (9^{th}~2^{nd} bytes)	
1Fh	Max. Power for Self Power [3:0] and Reserved [7:4]	Fixed_pattern (10^{th} byte)

Table 5 : eFuse (64-byte) Memory Map

Note_1: The Node ID 0 value cannot be set to 0xFF and 1^{st} bit of Node ID 0 can not be set to "1" (i.e. cannot be set to multicast MAC address).

Note_2: The correct value of eFuse Checksum field must be equal to (0xFF - SUM [eFuse offset 00h ~ 1Fh excluding eFuse Checksum field]). If SUM [eFuse offset 00h ~ 1Fh excluding eFuse Checksum field] has carry, please add '1' to its result.

4.1 Detailed Description

The following sections provide detailed descriptions for some of the fields in memory maps of serial EEPROM and eFuse. Please refer to **AX88178A EEPROM User Guide** for more details.

4.1.1 Node ID (00~02h)

The Node ID 0 to 5 bytes represent the MAC address of the device, for example, if MAC address = 04-23-45-67-89-AB, then Node ID 0 = 04h, Node ID 1 = 23h, Node ID 2 = 45h, Node ID 3 = 67h, Node ID 4 = 89h, and Node ID 5 = ABh.

Default values: Node ID {0, 1, 2, 3, 4, 5} = 00-0E-C6-81-78-01.

4.1.2 Flag (EEPROM: 05h, eFuse:18h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PME_IND	PME_TYPE	PME_POL	PME_PIN	SNT	0	WOLLP	RWU

RWU: Remote Wakeup support.

1: Indicate that this device supports Remote Wakeup (default).

0: Not support.

WOLLP: Wake-On-LAN Low Power function.

1: Enabled (default).

0: Disabled.

SNT: Serial Number Type. (Only valid for eFuse)

When SEEPROM loader selected EEPROM:

Please set this bit to '0' for EEPROM. The Serial Number String will refer to **Table 4** EEPROM offset 26h ~2Ch.

When SEEPROM loader selected eFuse:

1: Serial Number String is fixed to "00000000000001".

0: Use Node ID as Serial Number String (default).

For example, when Node ID {0, 1, 2, 3, 4, 5} = 00-0E-C6-81-78-01,

Serial Number String = "00000EC6817801".

PME_PIN: PME / GPIO_0.

1: Set GPIO_0 pin as PME (default).

0: GPIO_0 pin is controlled by vendor command.

PME_POL: PME pin active Polarity.

1: PME active high (default).

0: PME active low.

PME_TYP: PME I/O Type.

1: PME output is a Push-Pull driver (default).

0: PME output to function as an open-drain buffer.

PME_IND: PME indication.

1: A 1.363ms pulse active when detecting wake-up event.

0: A static signal active when detecting wake-up event (default).

4.1.3 Max. Power for Self/Bus Power (07h)

They are Max power values' setting of powerd device for EEPROM at offset 07h. Bus power setting for eFuse is at offset 05h (Low Byte), and Self power setting for eFuse at offset 1Fh (High Byte) [3:0].

The default value of Bus Power is 3Eh: For USB 2.0, the power value is 248mA (Unit = 4mA).

Self power setting follows conversion above.

4.1.4 EndPoint1 for HS/FS (EEPROM:08h, eFuse: 06h)

It's Interval (named "bInterval") for polling Interrupt IN endpoint 1 for data transfers of High-Speed/Full-Speed. Expressed in frames or microframes depending on the device operating speed (i.e. either 1 millisecond or 125 μs units).

The default "bInterval" value is 0Bh for High-Speed (the polling time of endpoint 1= $2^{(11-1)}$ * 125 μs=128ms) and is 80h for Full-Speed (the polling time of endpoint 1= 128 * 1ms=128ms).

Keep this field as the recommended default values (0Bh for High-Speed & 80h for Full-Speed).

4.1.5 LED Mode (EEPROM: 42h, eFuse: 19h~1Ah)

It's to define the indication setting for LED_0/1/2 function of MFA_0/1/2 pins.

Bit 7~Bit 0: LED_Mode_LB; Bit 15~Bit 8: LED_Mode_HB

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LED1_100	LED1_10	LED1_Active	LED0_Duplex	LED0_1000	LED0_100	LED0_10	LED0_Active
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
1	LED2_Duplex	LED2_1000	LED2_100	LED2_10	LED2_Active	LED1_Duplex	LED1_1000

Note: Bit 15 must be '1' to enable the LED_mode setting; otherwise, it will work at default LED mode.

The LED mode table is as below:

bit	4	3	2	1	0	Description of indication
LED_0	Full duplex	Link speed(Mbps)			Active (TX/RX)	
		1000	100	10		
	0	0	0	0	0	Reserved.
	0	0	0	0	1	Active (Default)
	0	0	0	1	0	Link 10
	0	0	0	1	1	Link 10+Active
	0	0	1	0	0	Link 100
	0	0	1	0	1	Link 100+Active
	0	0	1	1	0	Link 100/10
	0	0	1	1	1	Link 100/10+Active
	0	1	0	0	0	Link 1000
	0	1	0	0	1	Link 1000+Active
	0	1	0	1	0	Link 1000/10
	0	1	0	1	1	Link 1000/10+Active
	0	1	1	0	0	Link 1000/100
	0	1	1	0	1	Link 1000/100+Active
	0	1	1	1	0	Link 1000/100/10
	0	1	1	1	1	Link 1000/100/10+Active
	1	0	0	0	0	Full duplex
bit	9	8	7	6	5	Description of indication
LED_1	Full duplex	Link speed(Mbps)			Active (TX/RX)	
		1000	100	10		
	0	0	0	0	0	Reserved.
	0	0	0	0	1	Active
	0	0	0	1	0	Link 10
	0	0	0	1	1	Link 10+Active
	0	0	1	0	0	Link 100
	0	0	1	0	1	Link 100+Active
	0	0	1	1	0	Link 100/10
	0	0	1	1	1	Link 100/10+Active
	0	1	0	0	0	Link 1000
	0	1	0	0	1	Link 1000+Active
	0	1	0	1	0	Link 1000/10
	0	1	0	1	1	Link 1000/10+Active
	0	1	1	0	0	Link 1000/100
	0	1	1	0	1	Link 1000/100+Active
	0	1	1	1	0	Link 1000/100/10 (Default)
	0	1	1	1	1	Link 1000/100/10+Active
	1	0	0	0	0	Full duplex

bit	14	13	12	11	10	Description of indication
LED_2	Full duplex	Link speed(Mbps)			Active (TX/RX)	
		1000	100	10		
	0	0	0	0	0	Reserved.
	0	0	0	0	1	Active
	0	0	0	1	0	Link 10
	0	0	0	1	1	Link 10+Active
	0	0	1	0	0	Link 100
	0	0	1	0	1	Link 100+Active
	0	0	1	1	0	Link 100/10
	0	0	1	1	1	Link 100/10+Active
	0	1	0	0	0	Link 1000
	0	1	0	0	1	Link 1000+Active
	0	1	0	1	0	Link 1000/10
	0	1	0	1	1	Link 1000/10+Active
	0	1	1	0	0	Link 1000/100
	0	1	1	0	1	Link 1000/100+Active
	0	1	1	1	0	Link 1000/100/10
	0	1	1	1	1	Link 1000/100/10+Active (Default)
	1	0	0	0	0	Full duplex

Table 6 : LED Mode Setting Table

4.1.6 Fixed_pattern (EEPROM: 41~3Dh, eFuse: 1F~1Ah)

Please write these 10 bytes of fixed_pattern with hexadecimal (from low bytes to high bytes) = “40 4A 40 00 40 30 0D 49 90 41”.

4.2 Internal ROM Default Settings

AX88178A supports internal ROM default settings inside chip hardware to enable it to communicate with USB host controller during enumeration when the AX88178A EEPROM is blank (prior to being programmed) or the value of EEPROM Checksum field is wrong or the 1st byte data of EEPROM is 0xFF. The default settings inside chip facilitate users to update the EEPROM content through a Windows PC during R&D validation process or program a blank EEPROM/eFuse during manufacturing process.

Below table shows AX88178A's internal ROM default settings being used in the case of blank EEPROM or EEPROM with wrong checksum value or 1st byte data is 0xFF on board. Each of the address offset contains 16-bit data from left to right representing the low-byte and high-byte, respectively. For example, in offset address 0x01, the 'C6' is low-byte data and the '81' is high-byte data.

Offset Address	0 8	1 9	2 A	3 B	4 C	5 D	6 E	7 F
0x00 0x08	**00 0E** 80 0B	**C6 81** 09 04	**78 01** 0E **08**	**8A 17** 1A **10**	**95 0B** 26 **0E**	**BD 73** 2D 16	00 E0 **41 58**	**3E 01** **38 38**
0x10 0x18	**31 37** 00 00	**38 41** 00 00	00 00 **41 53**	00 00 **49 58**	00 00 **20 45**	00 00 **6C 65**	00 00 **63 2E**	00 00 **20 43**
0x20 0x28	**6F 72** **30 30**	**70 2E** **30 30**	00 00 **30 30**	00 00 **30 30**	00 00 **30 31**	00 00 05 0F	**30 30** 16 00	**30 30** 02 07
0x30 0x38	10 02 00 00	02 00 00 00	00 00 00 00	0A 10 00 00	03 00 F3 FF	0E 00 40 42	01 0A 40 00	FF 07 40 30
0x40 0x48	0D 49 FF FF	90 41 FF FF	00 40 FF FF	00 80 FF FF	20 08 FF FF	FF FF FF FF	FF FF FF FF	FF FF FF FF
0x50 0x58	FF FF FF FF	FF FF FF FF	FF FF FF FF	FF FF FF FF	FF FF FF FF	FF FF FF FF	FF FF FF FF	FF FF FF FF
0x60 0x68	FF FF FF FF	FF FF FF FF	FF FF FF FF	FF FF FF FF	FF FF FF FF	FF FF FF FF	FF FF FF FF	FF FF FF FF
0x70 0x78	FF FF FF FF	FF FF FF FF	FF FF FF FF	FF FF FF FF	FF FF FF FF	FF FF FF FF	FF FF FF FF	FF FF FF FF
0x80~FF	FF FF	FF FF	FF FF	FF FF	FF FF	FF FF	FF FF	FF FF

Note: The 6 bytes from Internal ROM memory offset 42h to offset 44h are unused.

Table 7 : Internal ROM Memory Map

4.2.1 Internal ROM Description

The internal ROM is a fixed value. **User can't modify it.**

Field Definition	Address Offset	Default Values	Description
Node ID	00h ~02h	00 0E C6 81 78 01	Node ID 0 ~ 5
Product ID (PID)	03h	8A 17	The PID of AX88178A is 0x178A
Vender ID (VID)	04h	95 0B	ASIX's VID is 0x0B95
Checksum	05h (Low byte)	BD	0xFF - SUM [EEPROM offset 03h ~ 04h]
Flag - Remote Wakeup and PME setting, etc.	05h (High byte)	73	Enable the "remote wakeup" and Low Power WOL function, (Note 1)
Max Power for Bus Power	07h (Low byte)	3E	248mA for USB 2.0 (Note 2)
Max Power for Self Power	07h (High byte)	01	4mA for USB 2.0 (Note 2)
Length of Product String	0Ah (High byte)	08	Product String Length (Note 3)
Length of Manufacturer String	0Bh (High byte)	10	Manufacturer String Length (Note 3)
Length of Serial Number String	0Ch (High byte)	0E	Serial Number String Length (Note 3)
Product String (Max. 24 bytes)	0Eh~19h	41 58 38 38 31 37 38 41 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	"AX88178A"
Manufacture String (Max. 24 bytes)	1Ah~25h	41 53 49 58 20 45 6C 65 63 2E 20 43 6F 72 70 2E 00 00 00 00 00 00 00 00	"ASIX Elec. Corp."
Serial Number String (Max. 14 bytes)	26h~2Ch	30 30 30 30 30 30 30 30 30 30 30 30 30 31	"00000000000001"

Table 8 : Internal ROM Description

Note 1: Remote Wakeup/PME Settings

The offset 05h field of AX88178A EEPROM is used to configure the Remote Wakeup and PME functions. Please refer to Section 4 "Serial EEPROM/eFuse Memory Map" for the detailed description of EEPROM offset 05h.

The RWU bit of AX88178A EEPROM offset 05h is used to configure the "bmAttributes" field of Standard Configuration Descriptor that will be reported to the USB host controller when the GET_DESCRIPTOR command with CONFIGURATION type is issued. Please refer to below table or "Section 9.6.3 Configuration" of Universal Serial Bus 2.0 Spec for the detailed description of the "bmAttributes" field of Standard Configuration Descriptor.

The power mode about Bus-powered or Self-powerd is decided by the SELF_PWR pin when chip powers on. This will updated to the "bmAttributes" field of Standard Configuration Descriptor.

Table 9-10. Standard Configuration Descriptor (Continued)

Offset	Field	Size	Value	Description
7	*bmAttributes*	1	Bitmap	Configuration characteristics D7: Reserved (set to one) D6: Self-powered D5: Remote Wakeup D4...0: Reserved (reset to zero) D7 is reserved and must be set to one for historical reasons. A device configuration that uses power from the bus and a local source reports a non-zero value in *bMaxPower* to indicate the amount of bus power required and sets D6. The actual power source at runtime may be determined using the GetStatus(DEVICE) request (see Section 9.4.5). If a device configuration supports remote wakeup, D5 is set to one.

Note 2: Max Power Setting

The low byte of AX88178A EEPROM offset 07h (for bus-powered) field and high byte of AX88178A EEPROM offset 07h (for self-powered) field are used to configure the "bMaxPower" field of Standard Configuration Descriptor that will be reported to the USB host controller when the GET_DESCRIPTOR command with CONFIGURATION type is issued. Please refer to below table or "Section 9.6.3 Configuration" of Universal Serial Bus 2.0 Spec for the detailed description of the "bMaxPower" field of Standard Configuration Descriptor. These fields are used to define the Maximum power consumption of the USB device drawn from the USB bus in this specific configuration when the device is fully operational.

Table 9-10. Standard Configuration Descriptor (Continued)

Offset	Field	Size	Value	Description
8	*bMaxPower*	1	mA	Maximum power consumption of the USB device from the bus in this specific configuration when the device is fully operational. Expressed in 2 mA units (i.e., 50 = 100 mA). Note: A device configuration reports whether the configuration is bus-powered or self-powered. Device status reports whether the device is currently self-powered. If a device is disconnected from its external power source, it updates device status to indicate that it is no longer self-powered. A device may not increase its power draw from the bus, when it loses its external power source, beyond the amount reported by its configuration. If a device can continue to operate when disconnected from its external power source, it continues to do so. If the device cannot continue to operate, it fails operations it can no longer support. The USB System Software may determine the cause of the failure by checking the status and noting the loss of the device's power source.

Note 3: Product/Manufacturer/Serial Number String Settings

The "Offset" fields of Product/Manufacturer/Serial Number String are fixed in AX88178A EEPROM/eFuse memory map. Please DON'T change the recommended values of these fields.

If you need to change the Product/Manufacturer/Serial Number strings on your AX88178A EEPROM/eFuse, please modify the "Length" fields of Product/Manufacturer/Serial Number String to meet the exact string length of your Product/Manufacturer/Serial Number strings.

4.2.2 External EEPROM Description

User can assign the specific VID/PID, Serial Number, Manufacture String, Product String, etc. user defined fields by external EEPROM or embedded eFuse. Please refer to **AX88178A EEPROM User Guide** document for more details about how to configure AX88178A EEPROM/eFuse content.

Note the EEPROM checksum field should be changed together with the VID/PID fields.

5 USB Configuration Structure

5.1 USB Configuration

The AX88178A supports 1 Configuration.

5.2 USB Interface

The AX88178A supports 1 interface.

5.3 USB Endpoints

The AX88178A supports following 4 endpoints:

- Endpoint 0: Control endpoint. It is used for configuring the device.
- Endpoint 1: Interrupt endpoint. It is used for reporting network Link status.
- Endpoint 2: Bulk IN endpoint. It is used for receiving Ethernet Packet.
- Endpoint 3: Bulk OUT endpoint. It is used for transmitting Ethernet Packet.

6 Electrical Specifications

6.1 DC Characteristics

6.1.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VCCK	Digital core power supply	- 0.5 to 1.44	V
VCC12A_TX	Analog Power for USB Transceiver. 1.2V	- 0.5 to 1.6	V
VCC12A_RX	Analog Power for USB Transceiver. 1.2V	- 0.5 to 1.6	V
VCC12A_X	Analog Power for Ethernet PHY. 1.2V	- 0.1 to 1.26	V
VCC12A	Analog Power for Ethernet PHY.1.2V	- 0.1 to 1.26	V
VCC3IO	Power supply of 3.3V I/O	- 0.5 to 4.2	V
VCC33IO	Power supply of 3.3V for clock pin.	- 0.5 to 4.6	V
VCC33A	Analog Power 3.3V for USB Transceiver.	- 0.5 to 4.6	V
VCC33A_X	Analog Power for Ethernet PHY. 3.3V	- 0.4 to 3.7	V
VCC33A_G	Analog Power for Ethernet PHY. 3.3V	- 0.4 to 3.7	V
V_{IN3}	Input voltage of 3.3V I/O	- 0.5 to 4.2	V
	Input voltage of 3.3V I/O with 5V tolerant	- 0.5 to 5.8	V
T_{STG}	Storage temperature	- 65 to 150	℃
I_{IN}	DC input current	50	mA
I_{OUT}	Output short circuit current	50	mA

Note: 1.Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the optional sections of this datasheet. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

2. The input and output negative voltage ratings may be exceeded if the input and output currents under ratings are observed.

6.1.2 Recommended Operating Condition

Symbol	Parameter	Min	Typ	Max	Unit
VCCK	Digital core power supply	1.14	1.2	1.26	V
VCC12A_TX	Analog Power for USB Transceiver. 1.2V	1.14	1.2	1.26	V
VCC12A_RX	Analog Power for USB Transceiver. 1.2V	1.14	1.2	1.26	V
VCC12A_X	Analog Power for Ethernet PHY. 1.2V	1.14	1.2	1.26	V
VCC12A	Analog Power for Ethernet PHY.1.2V	1.14	1.2	1.26	V
VCC3IO	Power supply of 3.3V I/O	3.13	3.3	3.47	V
VCC33IO	Power supply of 3.3V for clock pin.	3.13	3.3	3.47	V
VCC33A	Analog Power 3.3V for USB Transceiver.	3.13	3.3	3.47	V
VCC33A_X	Analog Power for Ethernet PHY. 3.3V	2.97	3.3	3.63	V
VCC33A_G	Analog Power for Ethernet PHY. 3.3V	2.97	3.3	3.63	V
T_j	Maximum junction operating temperature	-	-	125	℃
T_a	Ambient operating temperature	0	-	70	℃

6.1.3 Leakage Current and Capacitance

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IN}	True 3.3 V I/O input leakage current	V_{in} = 3.3 V or 0 V	-	≤±1	-	µA
	3.3 V with 5 V tolerance I/O Input leakage current	V_{in} = 5 V or 0 V	-	<±1	-	pF
C_{IN}	Input capacitance	3.3V I/O cells	-	2.25	-	pF
		3.3V with 5V tolerant I/O cells	-	3.6	-	pF

Note: C_{IN} includes the cell layout capacitance and pad capacitance (Estimated to be 0.5 pF).

6.1.4 DC Characteristics of 3.3V I/O Pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vil	Input low voltage	LVTTL	-	-	0.8	V
Vih	Input high voltage		2.0	-	-	V
Vt-	Schmitt trigger negative going threshold voltage	LVTTL	0.8	1.1	-	V
Vt+	Schmitt trigger positive going threshold voltage		-	1.6	2.0	V
Vol	Output low voltage	|Iol| = 4~8mA	-	-	0.4	V
Voh	Output high voltage	|Ioh| = 4~8mA	2.4	-	-	V
Vopu[1]	Output pull-up voltage for 5 V tolerance I/O cells	PU = VCC3IO, PD = 0V, E = 0, $\|I_{pu}\|$ = 1 µA	VCC3IO – 0.9	-	-	V
Rpu	Input pull-up resistance	PU = VCC3IO, PD = 0V	40	75	190	KΩ
Rpd	Input pull-down resistance	PU = 0V, PD = VCC3IO	40	75	190	KΩ

[1] This parameter indicates that the pull-up resistor for the 5 V tolerance I/O cells cannot reach the VCC3IO DC level even without the DC loading current.

6.2 Thermal Characteristics

Description	Symbol	Rating	Units
Thermal resistance of junction to case	Θ_{JC}	8.3	°C/W
Thermal resistance of junction to ambient	Θ_{JA}	21.4	°C/W

Note: θ_{JA} , θ_{JC} defined as below

$$\theta_{JA} = \frac{T_J - T_A}{P},\ \theta_{JC} = \frac{T_J - T_C}{P}$$

T_J: maximum junction temperature (°C) T_A: ambient or environment temperature (°C)
T_C: the top center of compound surface temperature (°C) P: input power (watts)

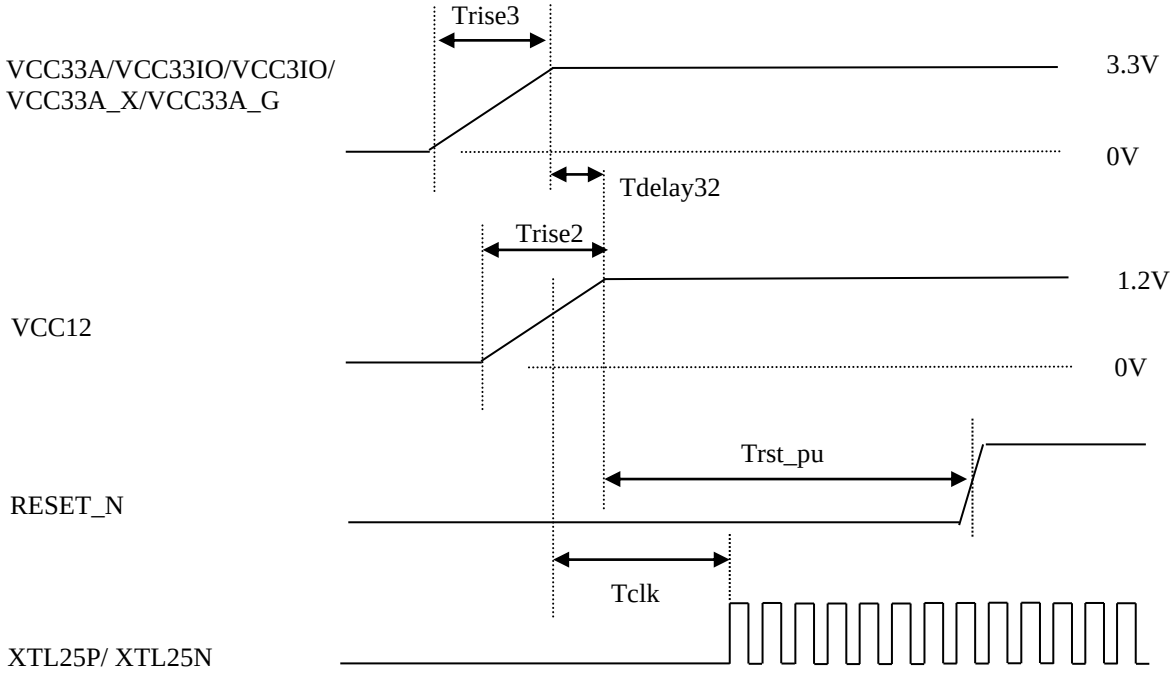
6.3 Power Consumption

Symbol	Description	Conditions	Min	Typ	Max	Unit
IVCC12	Current Consumption of 1.2V	Operating at Ethernet 1GMbps(full duplex) mode and USB High Speed mode		228		mA
IVCC33	Current Consumption of 3.3V			79		mA
IVCC12	Current Consumption of 1.2V	Operating at Ethernet 100Mbps full duplex mode and USB High Speed mode		85		mA
IVCC33	Current Consumption of 3.3V			50		mA
IVCC12	Current Consumption of 1.2V	Operating at Ethernet 10Mbps half duplex mode and USB High Speed mode		48		mA
IVCC33	Current Consumption of 3.3V			53		mA
IVCC12	Current Consumption of 1.2V	Operating at Ethernet 1Gbps(full duplex) mode and USB Full Speed mode		216		mA
IVCC33	Current Consumption of 3.3V			63		mA
IVCC12	Current Consumption of 1.2V	Operating at Ethernet 100Mbps full duplex mode and USB Full Speed mode		77		mA
IVCC33	Current Consumption of 3.3V			40		mA
IVCC12	Current Consumption of 1.2V	Operating at Ethernet 10Mbps half duplex mode and USB Full Speed mode		42		mA
IVCC33	Current Consumption of 3.3V			46		mA
AutoDetach Ethernet Unlink/WOLLP Suspend						
IVCC12	Current Consumption of 1.2V	Ethernet unlink (Disable AutoDetach) and USB High Speed mode		46		mA
IVCC33	Current Consumption of 3.3V			28		mA
IVCC12	Current Consumption of 1.2V	Ethernet unlink (Enable AutoDetach)		23		mA
IVCC33	Current Consumption of 3.3V			12		mA
IVCC12	Current Consumption of 1.2V	USB Suspend and Ethernet is 1GMbps: enable Remote WakeUp and disable WOLLP (WOL Low Power)		200		mA
IVCC33	Current Consumption of 3.3V			47		mA
IVCC12	Current Consumption of 1.2V	USB Suspend and enable Remote WakeUp and enable WOLLP to 10Mbps		25		mA
IVCC33	Current Consumption of 3.3V			13		mA
IVCC12	Current Consumption of 1.2V	Suspend and disable Remote WakeUp (Refer to below $I_{SYSTEM\ (Suspend)}$ item for total power consumption at Suspend mode)		1.5		mA
IVCC33	Current Consumption of 3.3V			1.7		mA
IDLE Power Consumption For Etherent Linked in EEE /non-EEE						
IVCC12	Current Consumption of 1.2V	Operating at Ethernet 1GMbps mode and USB High Speed mode without traffic (Ethernet linked in EEE)		74		mA
IVCC33	Current Consumption of 3.3V			31		mA
IVCC12	Current Consumption of 1.2V	Operating at Ethernet 1GMbps mode and USB High Speed mode without traffic (Ethernet linked in non-EEE)		216		mA
IVCC33	Current Consumption of 3.3V			65		mA
IVCC12	Current Consumption of 1.2V	USB Suspend and enable Remote WakeUp (Ethernet linked in EEE 1GMbps mode)		56		mA
IVCC33	Current Consumption of 3.3V			0.4		mA
IDLE Green Etherent Cable-Length Power Saving (GEPS)						
IVCC12	Current Consumption of 1.2V	Operating at Ethernet 1GMbps mode @ 1.5 meters and USB High Speed mode (Enable GEPS)		216		mA
IVCC33	Current Consumption of 3.3V			65		mA
IVCC12	Current Consumption of 1.2V	Operating at Ethernet 1GMbps mode @ 1.5 meters and USB High Speed mode (Disable GEPS)		227		mA
IVCC33	Current Consumption of 3.3V			71		mA
Total Power Consumption						
I_{DEVICE}	1.2V/3.3V power consumption at full loading (chip only)	1.2V (Operating at High Speed/1GMbps mode)		228		mA
		3.3V (Operating at High Speed/1GMbps mode)		79		mA
I_{SYSTEM}	Total power consumption at full loading (demo board)	VBUS of 5.0V (Operating at High Speed/1GMbps mode) (Using Switching regulator with dual VOUT 3.3/1.2V)		133.7		mA
$I_{SYSTEM\ (Suspend)}$	Total power consumption at Suspend mode (demo board)	VBUS of 5.0V (Disable Remote WakeUp) (Using Switching regulator with dual VOUT 3.3/1.2V)		1.75		mA

Table 9 : Power consumption

6.4 Power-up Sequence

At power-up, the AX88178A requires the VCC33A/VCC33IO/VCC3IO/VCC33A_X/VCC33A_G power supply to rise to nominal operating voltage within Trise3 and the VCC12 (Note) power supply to rise to nominal operating voltage within Trise2.



Note: The VCC12 includes VCCK, VCC12A, and VCC12A_X/TX/RX.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{rise3}	3.3V power supply rise time	From 0V to 3.3V	-	-	10	ms
T_{rise2}	1.2V power supply rise time	From 0V to 1.2V	-	-	10	ms
$T_{delay32}$	3.3V rise to 1.2V rise time delay		-5	-	5	ms
T_{clk}	25MHz crystal oscillator stable time	From VCC3IO = 3.3V to stable clock period of XTA25P or XTAL25N	-	1 *2	-	ms
T_{rst_pu}	RESET_N low level interval time from power-up	From VCC12 = 1.2V and VCC3IO = 3.3V to RESET_N going high	0 *1	-	10	ms

*Note 1 : When the VCC12 power-up, the internal power-on-reset circuit will generate a few us (micro second) of hardware reset to chip and will start operation after the XTL25P/N 25MHz clock signals are stable.

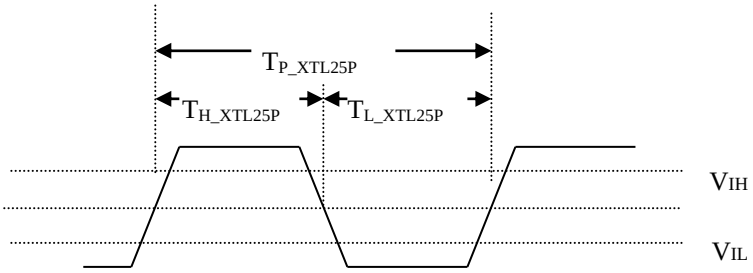
*Note 2 : The T_{clk} timing is depended on the 25MHz crystal circuit. The 1ms T_{clk} timing is reference timing based on the AX88178A reference 25MHz crystal circuit. Please refer to AX88178A reference schematic for details.

6.5 AC Timing Characteristics

Notice that the following AC timing specifications for output pins are based on C_L (Output load) equal to 50pF.

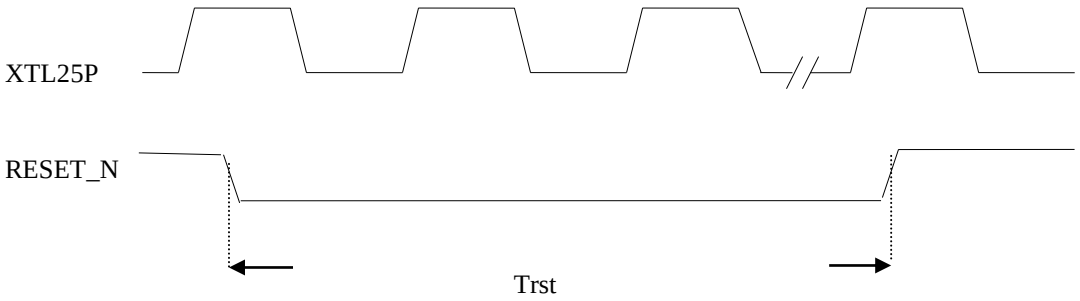
6.5.1 Clock Timing

XTL25P



Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{P_XTL25P}	XTL25P clock cycle time		-	40.0	-	ns
T_{H_XTL25P}	XTL25P clock high time		-	20.0	-	ns
T_{L_XTL25P}	XTL25P clock low time		-	20.0	-	ns

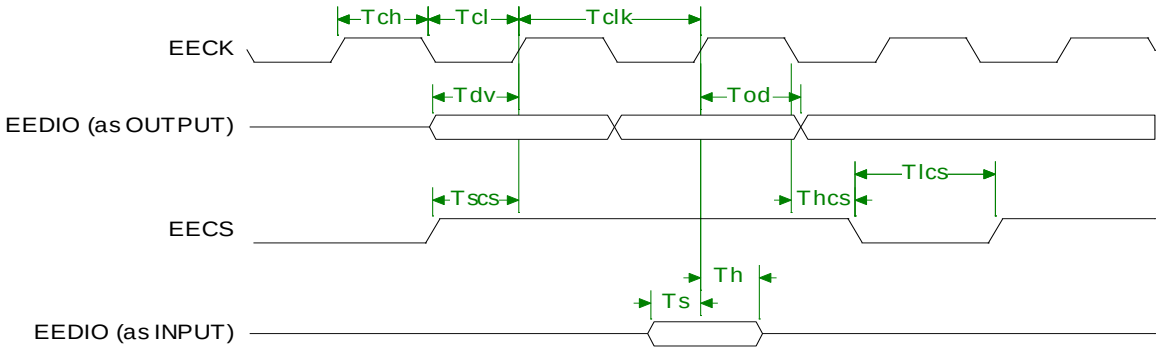
6.5.2 Reset Timing



Symbol	Description	Min	Typ	Max	Unit
Trst	Reset pulse width after XTL25P is running	125	-	250000	XTL25P clock cycle (Note)

Note: If the system applications require using hardware reset pin, RESET_N, to reset AX88178A during device initialization or normal operation after VBUS pin is asserted, the above timing spec (Min=5 μs, Max=10ms) of RESET_N should be met.

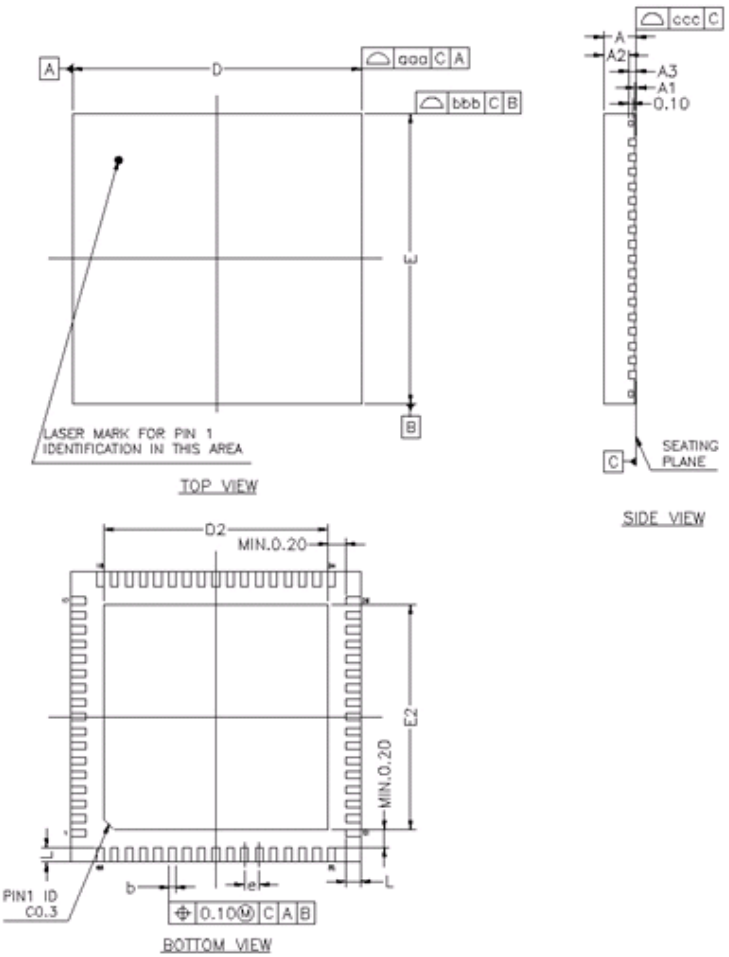
6.5.3 Serial EEPROM Timing



Symbol	Description	Min	Typ	Max	Unit
Tclk	EECK clock cycle time	-	5120	-	ns
Tch	EECK clock high time	-	2560	-	ns
Tcl	EECK clock low time	-	2560	-	ns
Tdv	EEDIO output valid to EECK rising edge time	2560	-	-	ns
Tod	EECK rising edge to EEDIO output delay time	2562	-	-	ns
Tscs	EECS output valid to EECK rising edge time	2560	-	-	ns
Thcs	EECK falling edge to EECS invalid time	7680	-	-	ns
Tlcs	Minimum EECS low time	23039	-	-	ns
Ts	EEDIO input setup time	20	-	-	ns
Th	EEDIO input hold time	0	-	-	ns

7 Package Information

7.1 68-pin QFN 8x8 package

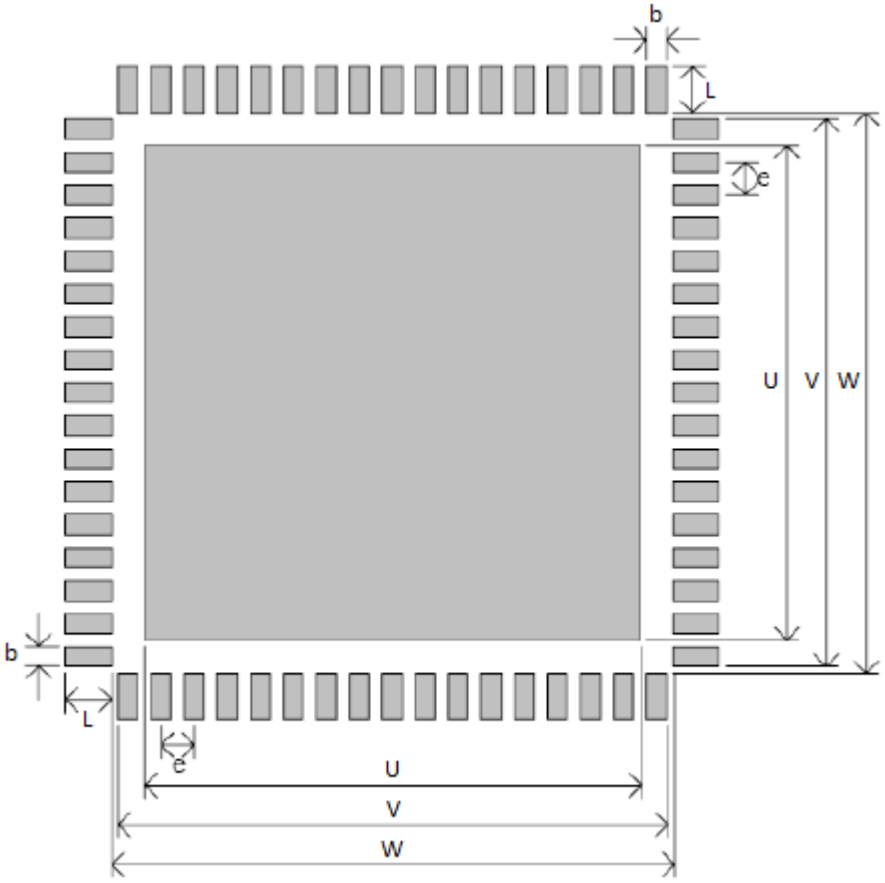


* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.035	0.05	0.00	0.001	0.002
A2	---	0.65	0.67	---	0.026	0.026
A3	0.203 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	7.90	8.00	8.05	0.311	0.315	0.317
D2	6.10	6.20	6.30	0.240	0.244	0.248
E	7.90	8.00	8.05	0.311	0.315	0.317
E2	6.10	6.20	6.30	0.240	0.244	0.248
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.40 bsc			0.016 bsc		
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6.PACKAGE WARPAGE MAX 0.08 mm.
7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8.APPLIED ONLY TO TERMINALS.

7.2 Recommended PCB Footprint for 68-pin QFN 8x8 package



Symbol	Description	Typical Dimension
e	Lead pitch	0.40 mm
b	Pad width	0.23 mm
L	Pad length	0.80 mm
U	-	6.30 mm
V	-	6.63 mm
W	-	7.20 mm

8 Ordering Information

Part Number	Description
AX88178AQF	68 PIN, QFN Package, Commercial Grade Temperature Range 0°C to +70 °C (Green, Lead-Free)

9 Revision History

Revision	Date	Comment
V0.10	2012/07/02	Prelimiary release.
V1.00	2012/07/18	1. Modified some descriptions in Section 4.1.6, 6.1 and 7.3.
V1.01	2012/08/07	1. Added Section 7.2 “Thermal Characteristics”. 2. Modified some descriptions in Section 3.11, 3.12, 7.4, 7.5.
V1.02	2012/09/05	1. Modified some descriptions in the Features page.
V1.03	2012/09/20	1. Modified some descriptions in the Features page. 2. Updated the block diagram in Figure 2.
V1.04	2013/01/08	1. Modified some descriptions in the Features page, Section 2.1, 3.11, 7.1.2.
V1.10	2013/05/06	1. Removed Section 6. 2. Modified some descriptions in the Section 2.2, 5.
V1.11	2013/11/05	1. Modified some descriptions in Section 6.4.
V1.20	2013/11/18	1. Added more information and modified some descriptions in Section 6.4.
V1.21	2014/06/05	1. Modified some descriptions in Section 6.1.2.
V1.22	2015/01/21	1. Modified some descriptions in the Feature page.
V1.30	2016/03/09	1. Modified some descriptions in Section 6.1.
V1.31	2016/04/11	1. Modified some descriptions in Section 6.1.
V1.32	2021/04/08	Corrected some descriptions in Section 8.

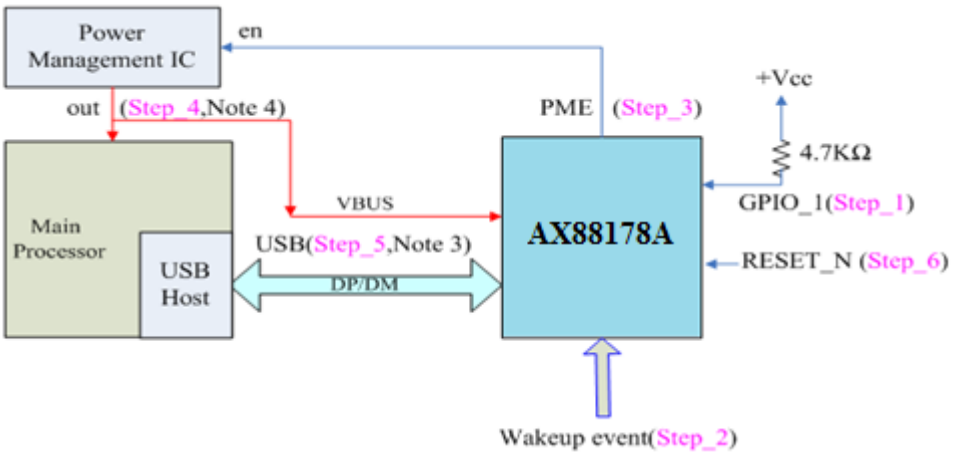
APPENDIX A. Default Wake-On-LAN (DWOL) Ready Mode

This Default WOL Ready Mode application is different from normal operation where AX88178A Suspend/Resume state usually has to be configured by software driver during normal system operation. This application applies to a system that needs to use a predefined remote wakeup event to turn on the power supply of the system processor and its peripheral circuits without having any system software running in the beginning. This is quite useful when a system has been powered down already and a user needs to power on the system from a remote location.

The AX88178A can be configured to support Default WOL Ready Mode, where no system driver is required to configure its WOL related settings after power on reset. A system design usually partitions its power supply into two or more groups and the AX88178A is supplied with an independent power separated from the system processor. The power supply of AX88178A is usually available as soon as power plug is connected. The power supply of system processor remains off initially when power plug is connected and is controlled by AX88178A's PME pin, which can be activated whenever AX88178A detects a predefined wakeup event such as valid Magic Packet reception or the EXTWAKE_N pin trigger. To conserve power consumption, initially the USB host controller communicating with AX88178A can also be unpowered as the system processor.

The PME pin of AX88178A can control the power management IC to power up the system processor along with the USB host controller, which will perform USB transactions with AX88178A after both have been initialized. The pin polarity of PME is configured as high active when enabling Default WOL Ready Mode (see following **A.1** Note 2). Note that the AX88178A must be in self-power (via setting EEPROM Flag [0]) mode for this function.

A.1 Procedure to Enable Default WOL Ready Mode



To enable Default WOL Ready Mode, a user needs to configure GPIO_0 pin definition as PME (via setting EEPROM Flag [12]) and have GPIO_1 pulled-up with a 4.7Kohm resistor. After power on reset, AX88178A will disable most functions including USB transceiver (see Note 3) but enable Magic Packet detector logic and internal Ethernet PHY and its auto-negotiation function to be ready to receive Magic Packet. When a valid Magic Packet is received, AX88178A will assert the PME pin to indicate to system processor the wakeup event. The PME pin, when being configured as static level output signal (via setting EEPROM Flag [15], see Note 2), can be used to control the power management IC to enable system power supply. After asserting the PME pin, AX88178A will also exit from the Default WOL Ready Mode and revert back to normal operation mode to start normal USB device detection, handshaking, and enumeration.

The PME pin, when being configured as static level output signal, maintains its signal level until RESET_N is asserted again. If asserting RESET_N to AX88178A with GPIO_1 pulled-up, the Default WOL Ready Mode will be re-entered. Otherwise (GPIO_1 being pulled-down), it will be entered normal operation mode and the normal USB device detection, handshaking and enumeration process should take place right after RESET_N negation.

Note 1: For complete truth table of wakeup events supported, please refer to below **Remote Wakeup Truth Table** on the "GPIO_1 = 1" setting.

Note 2: Please refer to Section 4.1.2 "Flag". The bit [15:12] of Flag (PME_IND, PME_TYP, PME_POL, PME_PIN) = 0111.

Note 3: When the Default WOL Ready Mode is enabled, the D+/D- pins ofAX88178A will be in tri-state.

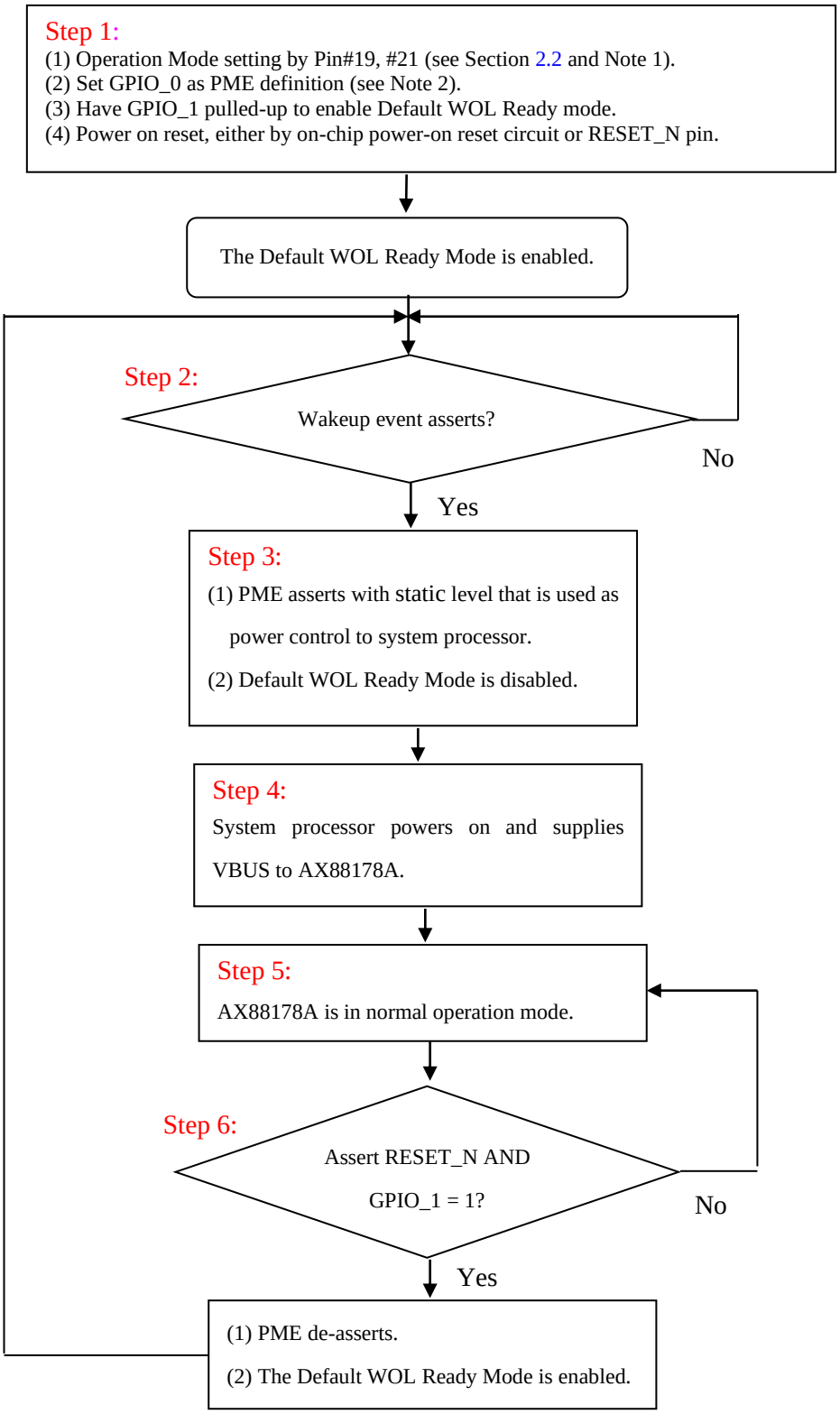
Note 4: It is recommended that VBUS pin be connected to system power group directly. This way the VBUS will become logic high when power management IC enables the system power supply.

Waken Up by	Setting						Wakeup Event					Device wakes up
	RWU bit of Flag byte in EEPROM	Set_Feature standard command	RWWF	RWMP	RWLC	GPIO_1 (*)	Host sends resume signal	Receiving a Wakeup Frame	Receiving a Magic Packet	Link status change detected On PHY	EXTWAKE_N pin	
USB Host	X	X	X	X	X	0	J → K					Yes
Device	0	0	X	X	X	0		X	X	X	X	No
Device	1	1	1	0	0	0		Yes				Yes
Device	1	1	0	1	0	0			Yes			Yes
Device	1	1	0	0	1	0				Yes		Yes
Device	1	1	0	0	1	0						Yes
Device	1	1	X	X	X	0					Low-pulse	Yes
Device	X	0	0	0	0	1			Yes		Low-pulse	Yes

*: About Default WOL Ready Mode, please refer to section 2.2 GPIO_1 Settings.

Table 10 : Remote Wakeup Truth Table

A.2 Flow Chart of Default WOL Ready Mode



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