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PROJECT REPORT

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Development of USB to Fiber Optic adapter

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Contents

1 Abstract

This report presents the development of a USB to SFP fiber optic adapter using 1 gigabit SFP modules and the Asix AX88772b IC. The aim of this project was to create a cost-effective and reliable solution for converting USB data to optical signals. The adapter was designed to operate at a data rate of 1 Gbps and supports full duplex communication.The hardware design of the adapter includes a USB connector, a power regulator, the Asix AX88772b IC, and the 1 gigabit SFP module. The adapter was tested using standard optical testing equipment to evaluate its performance in terms of signal integrity and transmission distance. The design and implementation of this adapter offer several advantages, such as the ability to use off-the-shelf components, cost-effectiveness, and reliability. This adapter can be used in various applications, such as in data centers, communication networks, and industrial environments. The adapter's ability to convert USB data to optical signals offers a solution for extending the distance of USB connections beyond the limitations of copper cables.In conclusion, this project demonstrates the feasibility of using 1 gigabit SFP modules and the Asix AX88772b IC to develop a USB to SFP fiber optic adapter that offers a cost-effective, reliable, and high-speed data transmission solution.

2 Introduction

The rapid development of data communication technology has led to the increasing demand for high-speed data transmission solutions. Fiber optic technology offers a reliable and high-speed data transmission option, but it has typically been more expensive and difficult to implement than traditional copper cable solutions. As a result, there is a need for cost-effective and reliable fiber optic solutions that can be easily implemented.

One solution to this problem is the use of USB to SFP fiber optic adapters. These adapters provide a way to convert USB data to optical signals, which can be transmitted over long distances without experiencing significant signal loss. The availability of 1 gigabit SFP modules and the Asix AX88772b IC has made it possible to develop a cost-effective and reliable USB to SFP fiber optic adapter.

The aim of this project is to develop a USB to SFP fiber optic adapter using 1 gigabit SFP modules and the Asix AX88772b IC. The adapter is designed to provide a cost-effective and reliable solution for converting USB data to optical signals. The adapter is expected to offer a high-speed data transmission solution that can operate at a data rate of 1 Gbps and support full duplex communication.

The hardware design of the adapter includes a USB connector, a power regulator, the Asix AX88772b IC, and the 1 gigabit SFP module. The software for the adapter was developed by ASIX electronics who offer the libusb library, which provides a user-friendly interface for configuring the adapter.The design and implementation of this adapter offer several advantages, such as the ability to use off-the-shelf components, cost-effectiveness, and reliability. This adapter can be used in various applications, such as in home servers, communication networks, and industrial environments. The adapter's ability to convert USB data to optical signals offers a solution for extending the distance of USB connections beyond the limitations of copper cables.

In conclusion, the development of a USB to SFP fiber optic adapter using 1 gigabit SFP modules and the Asix AX88772b IC offers a cost-effective, reliable, and high-speed data transmission solution for converting USB data to optical signals. This project demonstrates the feasibility of using off-the-shelf components to develop a USB to SFP fiber optic adapter suitable for various applications in the field of telecommunications and data communication.

3 List of Components Used

3.1 SFP Transceiver Module

SFP Transceiver modules have both optical transceiver and receiver built into them on one side and SFP plug on other side.The SFP modules used here is Agilent HFBR-5701L, 100Base-SX.This is a SFP module that supports a data rate of 100 Mbps. It provides an interface for connecting the adapter to the optical network. The HFBR-5701L is designed to be hot-swappable, which means it can be inserted and removed from the adapter while the power is on. The module is also equipped with an LC connector, which is a small, square-shaped connector commonly used in fiber optic networks. The 100Base-SX standard is used to transmit data over fiber optic cables and has a maximum distance of 275 meters. The Block diagram of HFBR-5701L is provided below:

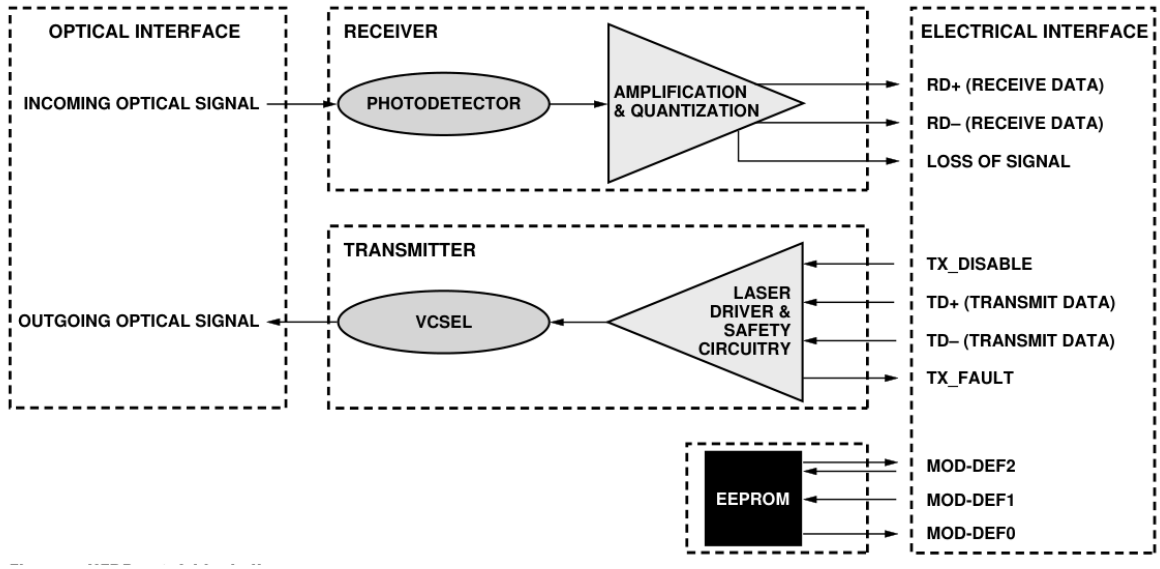

Figure 1: Block diagram of HFBR-5701L. [5]

The SFP modules have 20 pins each pin having different function.The function of each pin of HFBR-5701L is described in the table below:

Pin	Name	Function/Description
1	VeeT	Transmitter Ground
2	TX Fault	Transmitter Fault Indication
3	TX Disable	Transmitter Disable - Module disables on high or open
4	MOD-DEF2	Module Definition 2 - Two wire serial ID interface
5	MOD-DEF1	Module Definition 1 - Two wire serial ID interface
6	MOD-DEF0	Module Definition 0 - Grounded in module
7	Rate Select	Not Connected
8	LOS	Loss of Signal
9	VeeR	Receiver Ground
10	VeeR	Receiver Ground
11	VeeR	Receiver Ground
12	RD-	Inverse Received Data Out
13	RD+	Received Data Out
14	VeeR	Receiver Ground
15	VccR	Receiver Power - 3.3 V ±5%
16	VccT	Transmitter Power - 3.3 V ±5%
17	VeeT	Transmitter Ground
18	TD+	Transmitter Data In
19	TD-	Inverse Transmitter Data In
20	VeeT	Transmitter Ground

Figure 2: Pin out description of HFBR-5701L. [5]

3.2 USB to Ethernet controller

USB to Ethernet controllers are specifically designed to enable USB devices to connect to Ethernet networks. They provide a way to convert USB data signals into Ethernet packets that can be transmitted over an Ethernet network.The controller we used here is ASIX AX88772B.It is a high-performance and low-power USB 2.0 to 10/100/1000 Gigabit Ethernet controller designed for a wide range of applications. It is a highly integrated controller that features a built-in 10/100/1000 Ethernet MAC and PHY, and supports full-duplex with flow control and half-duplex operation.It interfaces with the host system via a USB 2.0 Hi-Speed device port, which supports high-speed data transfer rates of to 480Mbps.[4]

AX88772B supports following operation modes:

- 1. MAC mode
- 2. PHY mode

Below provides a detailed description for the mentioned operation modes:

- In MAC mode, the AX88772B Ethernet block is configured as an Ethernet MAC. From a system application standpoint, AX88772B can be used as a USB 2.0 to LAN Adaptor or a USB 2.0 to Fast Ethernet and Home PNA Combo. In MAC mode, the AX88772B internal Datapath can work with internal Ethernet PHY or RMII interface by setting.[4]
- In PHY mode, the AX88772B Ethernet block is configured as an Ethernet PHY interface. In this case, an external microcontroller with Ethernet MAC can interface with AX88772B as if it were to interface with an Ethernet PHY chip, and AX88772B can act as a USB to Reverse-RMII bridge chip for the microcontroller or PC to provide USB-2.0. Device interface for some system application as figure 1.[4]
  Detailed pinout description of AX88772B is given below

Pin Name	Type	Pin No	Pin Description
USB Interface			
DP	AB	56	USB 2.0 data positive pin.
DM	AB	57	USB 2.0 data negative pin.
V_BUS	I5/PD/S	50	VBUS pin input. Please connect to USB bus power.
RREF	AI	58	For USB PHY's internal biasing. Please connect to analog GND through a resistor (12.1Kohm ±1%).
Serial EEPROM Interface			
EECK	B5/PD/T	38	EEPROM Clock. EECK is an output clock to EEPROM to provide timing reference for the transfer of EECS, and EEDIO signals. EECK only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-down.
EECS	B5/PD/T	39	EEPROM Chip Select. EECS is asserted high synchronously with respect to rising edge of EECK as chip select signal. EECS only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-down.
EEDIO	B5/PU/T	40	EEPROM Data In. EEDIO is the serial output data to EEPROM's data input pin and is synchronous with respect to the rising edge of EECK. EEDIO only drive high / low when access EEPROM otherwise keep at tri-state and internal pull-up.
Ethernet PHY Interface			
XTL25P	I18	2	25Mhz ± 0.005% crystal or oscillator clock input. This clock is needed for the embedded 10/100M Ethernet PHY to operate.
XTL25N	O18	3	25Mhz crystal or oscillator clock output.
RXIP	AB	9	Receive data input positive pin for both 10BASE-T and 100BASE-TX.
RXIN	AB	10	Receive data input negative pin for both 10BASE-T and 100BASE-TX.
TXOP	AB	12	Transmit data output positive pin for both 10BASE-T and 100 BASE-TX
TXON	AB	13	Transmit data output negative pin for both 10BASE-T and 100 BASE-TX
RSET_BG	AO	5	For Ethernet PHY's internal biasing. Please connect to GND through a 12.1Kohm ±1% resistor.
Misc. Pins			
RESET_N	I5/PU/S	45	Chip reset input. Active low. This is the external reset source used to reset this chip. This input feeds to the internal power-on reset circuitry, which provides the main reset source of this chip. After completing reset, EEPROM data will be loaded automatically.
EXTWAKEUP_N	I5/PU/S	23	Remote-wakeup trigger from external pin. EXTWAKEUP_N should be asserted low for more than 2 cycles of 25MHz clock to be effective.
GPIO_2	B5/PD	25	General Purpose Input/ Output Pin 2.
GPIO_1	B5/PD	26	General Purpose Input/ Output Pin 1. This pin is default as input pin after power-on reset. This pin is also for Default WOL Ready Mode setting;

Figure 3: Pinout description of the AX88772B Controller. [4]

GPIO_0/PME	B5/PD	27	General Purpose Input/ Output Pin 0 or PME (Power Management Event). This pin is default as input pin after power-on reset. GPIO_0 also can be defined as PME output to indicate wake up event detected.
MFB7	B5/PU I5 I5	28	This is a multi-function pin. MFB7: RMII : RXD0 Reverse_RMII : TXD0
MFB6	B5/PU I5 I5	29	This is a multi-function pin. MFB6: RMII : RXD1 Reverse_RMII : TXD1
MFB5/ REF50	B5/PU B5	30	This is a multi-function pin. MFB5: When RMII enable, The REF50 in/out direction is determined by EEPROM Flag [1] setting.
MFB4	B5/PU O3 O3	31	This is a multi-function pin. RMII : TXD0 Reverse_RMII : RXD0
MFB3	B5/PU O3 O3	32	This is a multi-function pin. RMII : TXD1 Reverse_RMII : RXD1
MFB2	B5/PU O3 O3	33	This is a multi-function pin. RMII : TXEN Reverse_RMII : CRSDV
MFB1	B5/PU I5 I5	34	This is a multi-function pin. RMII : CRSDV Reverse_RMII : TXEN
MFB0	B5/PU	35	This is a GPIO pin.
MFA3/ PHY_N	O3 I5/PU	21	It is a multi-function pin. The default is USB Speed indicator. When USB bus is in Full speed, this pin will tri-state continuously. When USB bus is in High speed, this pin drives low continuously. This pin tri-state and drive low in turn (blinking) to indicate TX data transfer going on whenever the host controller sends bulk out data transfer. MFB1~7 bus is determined by setting of this input pin when MFA2 sets 0: 0: Reverse_RMII (PHY mode). 1: RMII (MAC mode).
MFA2/ RMII_N	O3 I5/PU	19	It is a multi-function pin. The default is Link status LED indicator. This pin drives low continuously when the Ethernet link is up and drives low and high in turn (blinking) when Ethernet PHY is in receiving or transmitting state. MFB1~7 function is determined by setting of this input pin: 0: Reverse_RMII/RMII . 1: MFB bus as GPIO function.
MFA1/ MDIO	O3 B5/PU	18	It is a multi-function pin. The default is Ethernet speed LED indicator. This pin drives low when the Ethernet PHY is in 100BASE-TX mode and drives high when in 10BASE-T mode. This pin can perform as MDIO when enabling Reverse_RMII/RMII.

Figure 4: Pinout description of the AX88772B Controller. [4]

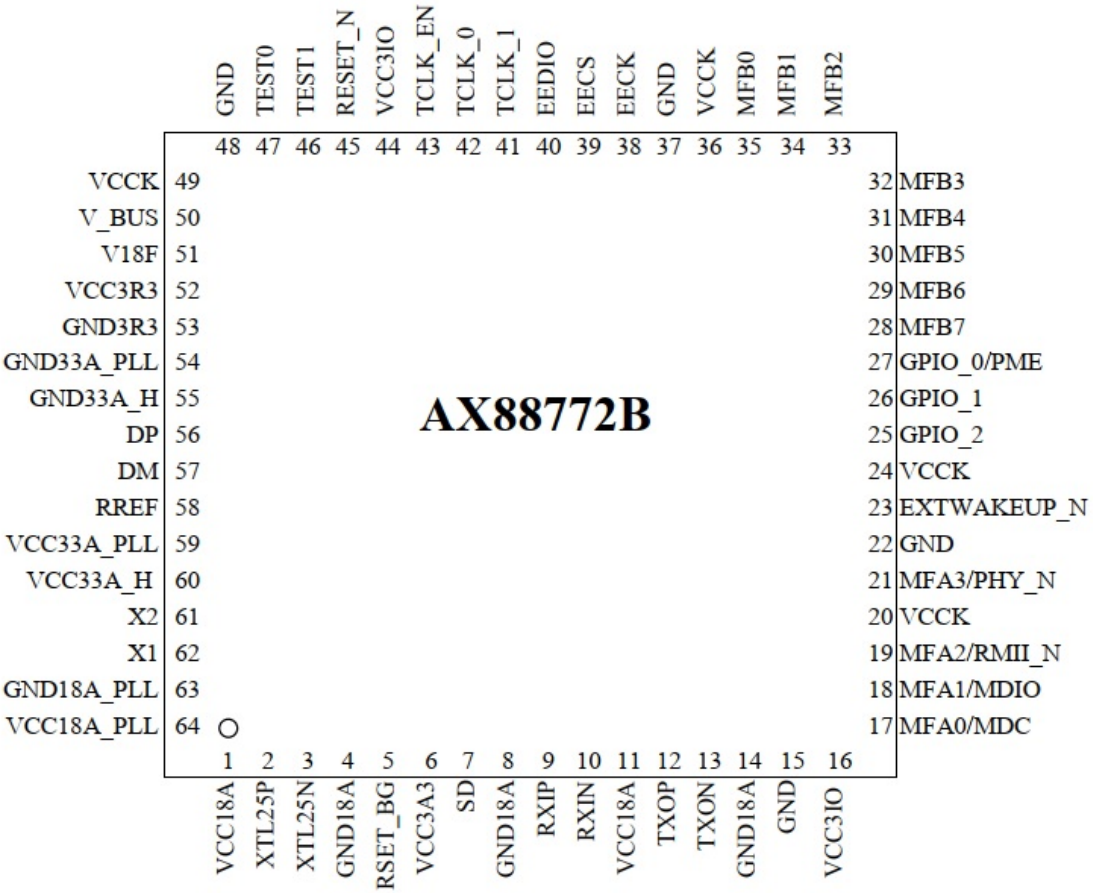

Figure 5: Pinout description of the AX88772B Controller. [4]

3.3 Voltage Regulator

Voltage regulator is necessary here to provide power to USB Ethernet controller and SFP module.The Voltage regulator used here is LM117 in SOT-23 package..The LM117 is a three-terminal positive voltage regulator that provides a fixed output voltage of 1.2V to 37V with up to 1.5A of output current. It is a linear regulator that operates by adjusting the voltage drop across a pass transistor to maintain a stable output voltage, and is designed to operate with a wide range of input voltages (up to 40V).The picture of LM117 with pin description is as follows:

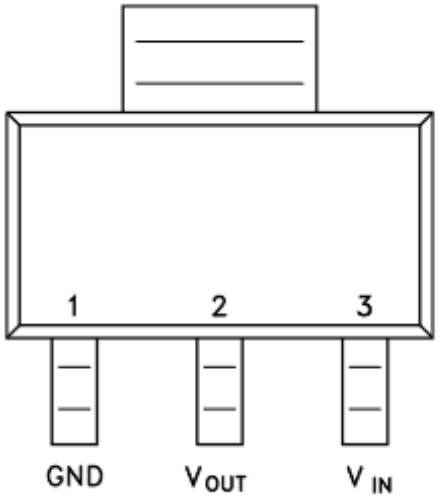

Figure 6: Pin out of LM117 (3.3V). [5]

The Model here used here has Vout fixed at 3.3V.Vin is supplied from USB header voltage pins which is 5V.This regulator coverts it to 3.3V required for components present on the board.The LM117 is widely used in a variety of applications that require a stable, regulated output voltage, including power supplies, battery chargers, and voltage references. It features built-in thermal overload protection, short circuit protection, and safe area protection, which help to ensure reliable operation even under harsh operating conditions.

3.4 EEPROM

The USB Ethernet controller operates by default in copper mode.We need an EEPROM to put the USB Ethernet controller in Fiber mode instead of Copper mode.Microchip 93C66LC in SOIC package is used here. Microchip 93C66LC is a low-power, 4K-bit serial electrically erasable programmable read-only memory that operates over a wide voltage range. It features a three-wire serial interface that supports high-speed data transfer rates of up to 3.4Mbps, and supports both byte and page write operations.The function of each pin of EEPROM is as follows:

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
NC	No internal connection
ORG	Memory Configuration
Vcc	Power Supply

Figure 7: Pin Function table of 93LC66. [1]

One of the key advantages of the 93C66LC EEPROM is its small form factor and low power consumption. The low power consumption of the device makes it an ideal choice for battery-powered applications, and its small form factor allows it to be used in applications with limited space.The package type used here is SOT23 and it Pin out is given in the figure below:

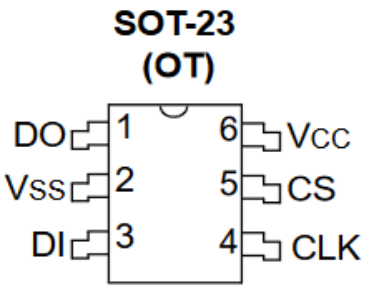

Figure 8: Pin out diagram of 93LC66. [1]

The EEPROM is programmed used EZP2019+ programmer.It can be used to program variety of EEPROM's.To make our USB-Ethernet IC work in fiber mode instead of copper mode(default) we need to make some changes to EEPROM.EEPROM configuration[2] is based on High Byte and Low Byte.The Flag 01h has the EPOM bit that controls operation in copper or fiber mode.Function of all bits in flag is given below:

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PME_IND	PME_TYP	PME_POL	PME_PIN	PHY_ISO	1	TDPE	CEM
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TACE	RDCE	EPOM	BOTM_EN	1	RWU	REF50_O	SP

Figure 9: Bit description of Flag 01h
[2]

EPOM: Embedded PHY copper/fiber Operation Mode.The working of EPOM bit is as follows:

- 1: Sets embedded PHY in copper mode (default)[2]
- 0: Sets embedded PHY in fiber mode[2]

The Bit is set to 0 for our use case here and that makes AX88772B work in Fiber mode and allows us to connect SFP terminals to AX88772b.

3.5 P-Channel MOSFET

In this project, the P-Channel Mosfet BSS138 is used to let the AX88772B IC know whenever there is loss of signal.It is connected between SD pin of IC and LOS(Loss of Signal) pin of SFP module.Whenever LOS is high, the SD pin is pulled down to ground, thus IC understands that there is loss of signal.

3.6 Fiber Optic Cable

The SFP modules on both adapters are connected by Fiber Optic cable.In this project, the Digitus D2533024 LWL Multimode Patchkabel is used to connect the Agilent HFBR-5701L 100Base-SX module on both ends of adapters. This cable has fiber diameter of 50/125µ.The Digitus D2533024 LWL Multimode Patchkabel is a high-quality fiber optic

patch cable that is used to connect optical devices over a short distance. It has a length of 2 meters and LC connectors on both ends. The cable is made of high-quality multimode fiber that provides a high data transfer rate and a low attenuation over the cable length.

3.7 Mini USB connector

The Mini USB connector is used to connect the IC to PC for data transmission and power delivery required for the board.The 5V and GND pins are used for power and D+ and D-.

3.8 Crystal Oscillator

The AX88772B integrates internal oscillator circuits for 25MHz, allowing the chip to cost-effectively work only with external 25MHz crystals. There are also three PLL circuits integrated into the chip to generate precise clocks. External 25MHz crystal oscillator is connected between pin 2 and pin 3 are between XTL 25P and XTL 25N pins on the controller, respectively. Pin 2 of the controller requires a 25 MHz ±0.005 percent crystal or oscillator clock input signal. This clock is required for the onboard 10/100M Ethernet and it causes PHY to operate.The crystal oscillator is connected between Pins 2 and 3 of IC as shown in figure below.[3]

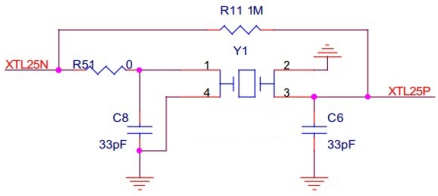

Figure 10: 25MHz Crystal Oscillator. [3]

4 Schematics of Circuit

The main reference schematic is made by ASIX electronics who make this AX88772B IC and it is available in their official website.All the connections between each component are present in the schematic.

The entire circuit schematic given by ASIX AX88772B is shown in 3 figures as follows:

4.1 Connections between USB,EEPROM and AX88772B

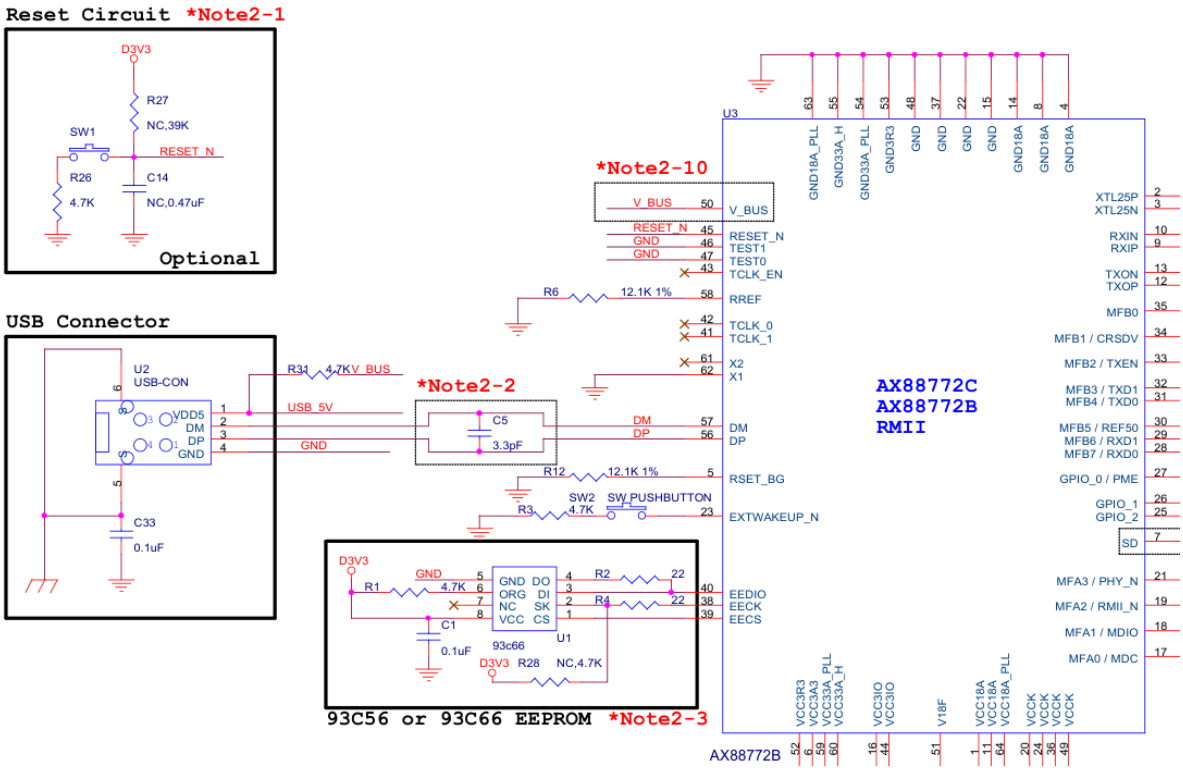

Figure 11: Connections between USB,EEPROM and AX88772B. [3]

4.2 Connections between SFP and AX88772B

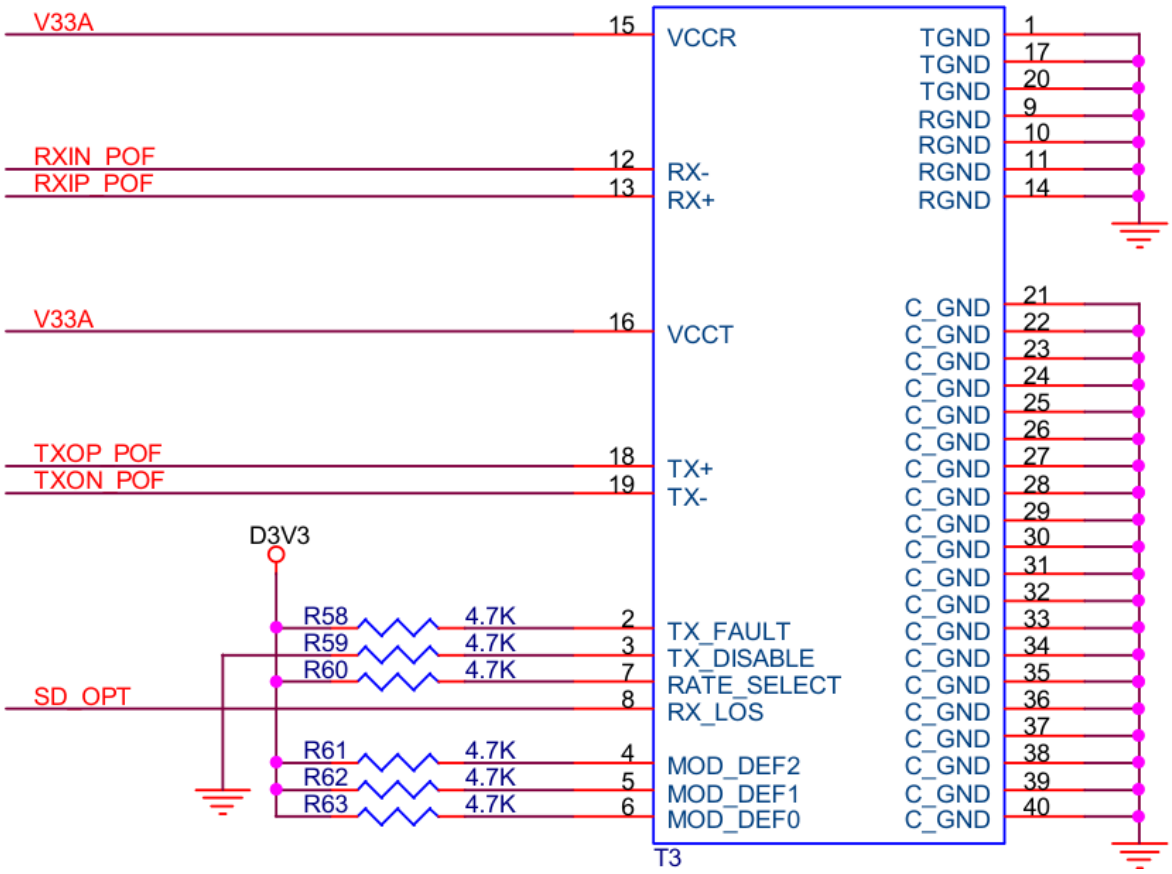

Figure 12: Connections between SFP and AX88772B. [3]

4.3 Connections between Crystal Oscillator,LED's and AX88772B

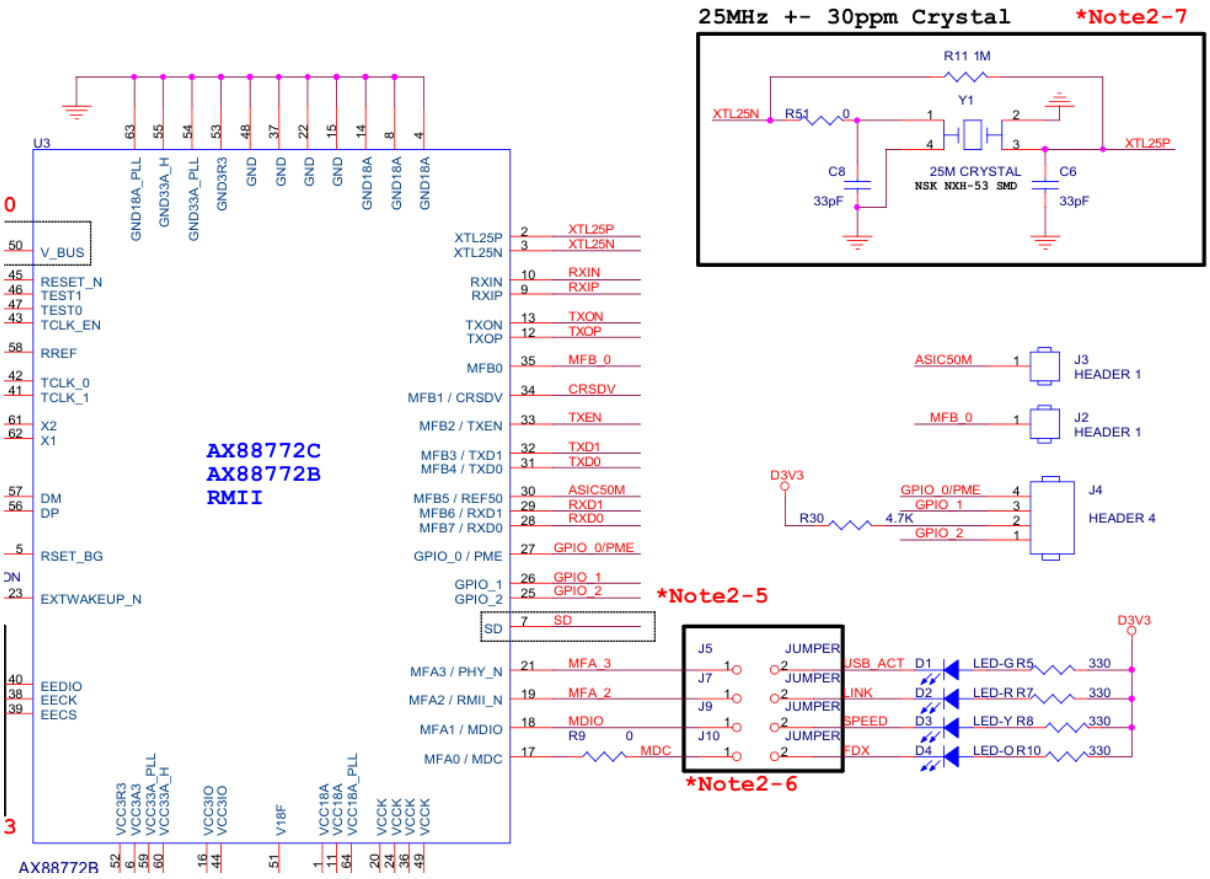

Figure 13: Connections between SFP and AX88772B. [3]

5 Design OF PCB using EAGLE

The schematic is made in EAGLE using reference circuit provided ASIX electronics.The connection having data transmission are kept short between components to prevent or reduce cross talk.Small capacitors are used on data lines to reduce noise in the signals.Ground planes is added to both top and bottom of board to further reduce noise in data signals. The schematic ,top and bottom side board file designed using EAGLE are provided below.

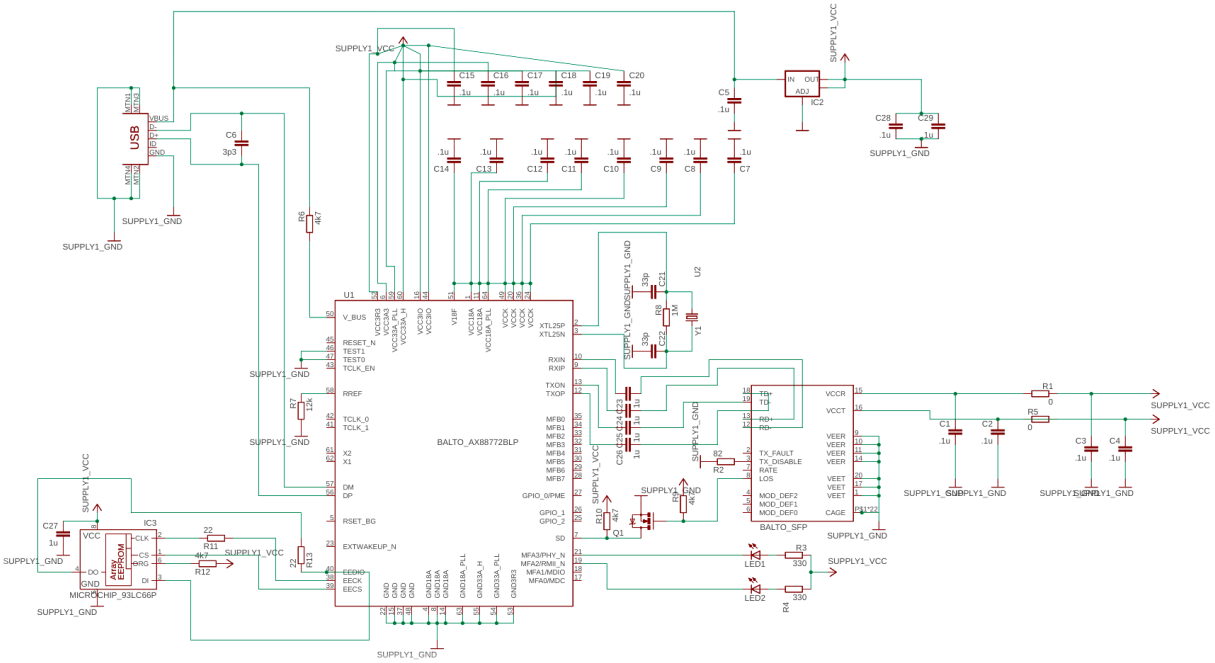

Figure 14: Schematics of PCB created with EAGLE software

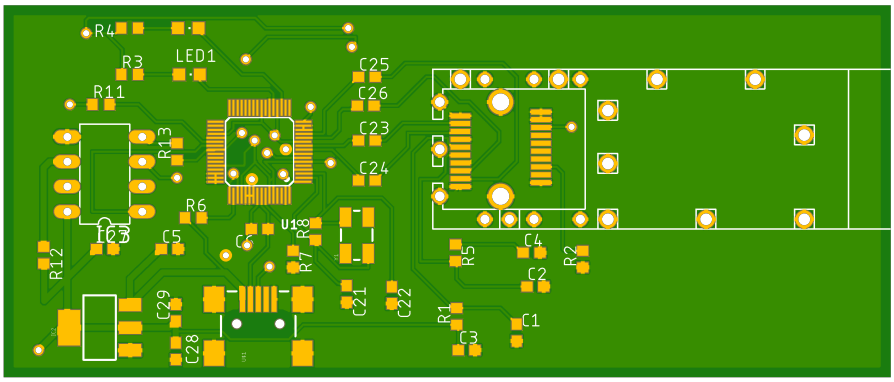

Figure 15: Top side of the board

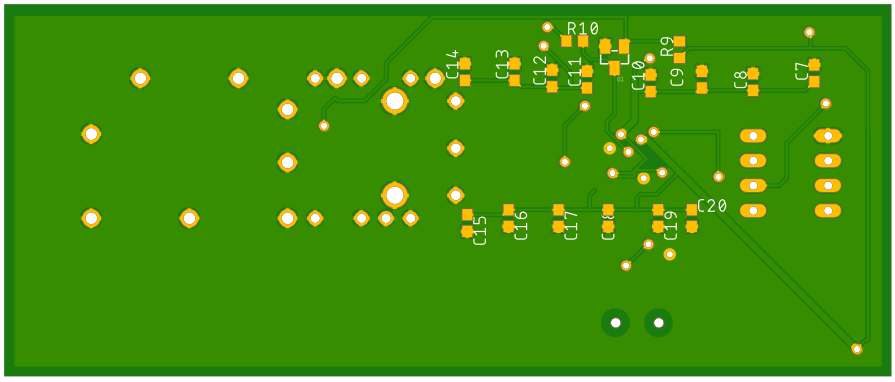

Figure 16: Bottom side of the board

6 Testing and Verification of PCB using fiber optic cable

All the components ares soldered to PCB using soldering oven.The connections are checked for possible short´s and good contact of all components.Visual inspection of Assembled PCB is done in Microscope, electrical and signal check and verification is done using Oscilloscope and Multi-meter.Fiber Optic transmission is verified using Fiber optic power meter.

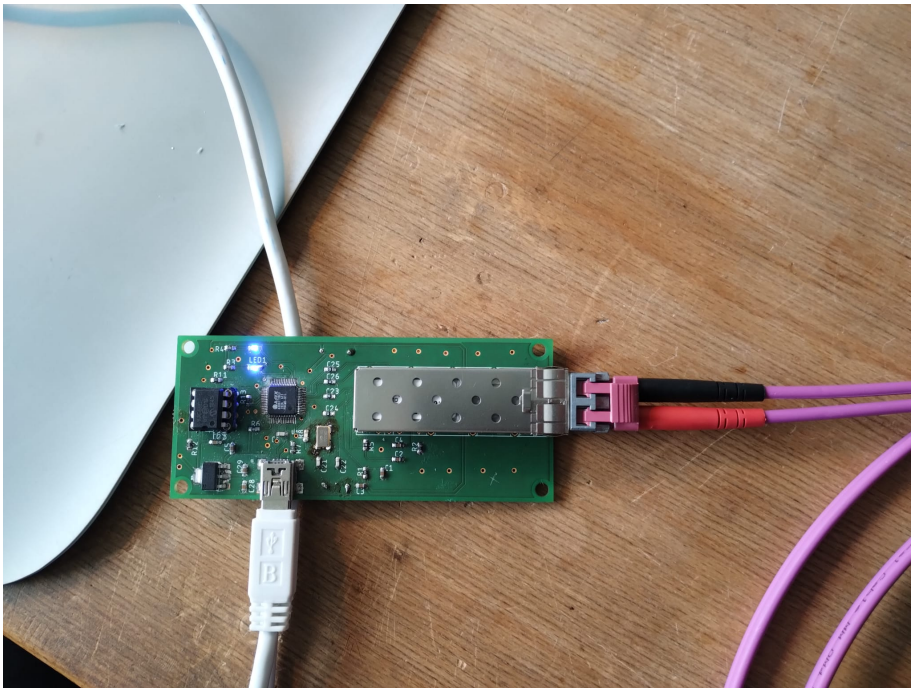

Figure 17: USB to Fiber Optic converter

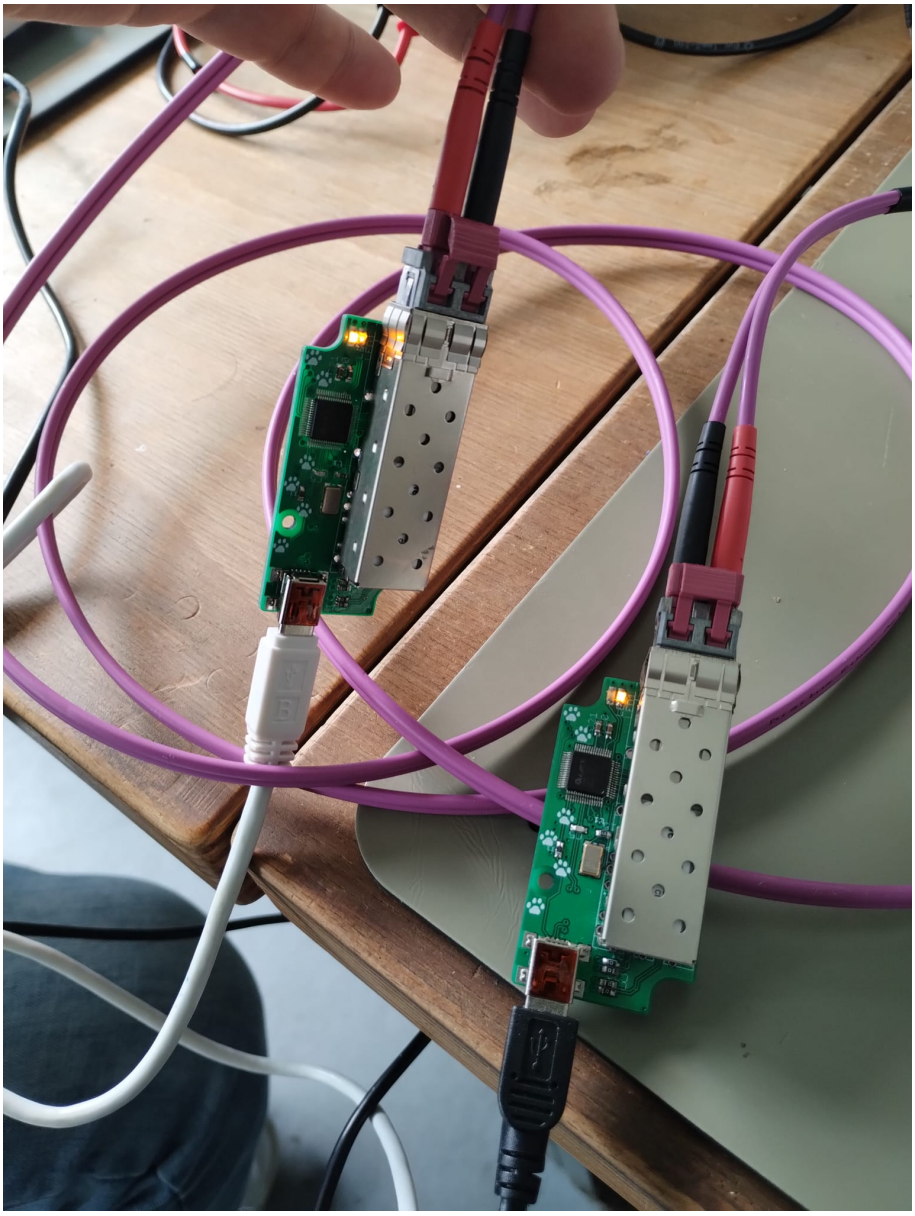

Figure 18: Adapters connected with fiber optic cable

7 Conclusion

In this project, we aimed to created USB to fiber optic adapter using SFP modules.We looked into possible ways to do data transmission over fiber optic cables.We researched into required components and schematics to make such an adapter.Finally PCB is designed and assembled to verify working of adapter over fiber optic cable.The adapter is recognized by the Windows computers on both ends of cable and SFP transceivers are sending signal on both ends.The receiving and Ethernet link between adapters even though it is shown to be established in Windows,Wire shark and Fiber optic power meter,the data transmitted cannot be received by other computer.We did as much debugging as possible to find error whether it is in driver or circuit design or EEPROM.At the end we are unable to find the error causing the problem to not receive data at USB ports.

References

[1] *93LC66 datsheet*. April 12, 2023. August 25, 2022. URL: https://cdn-reichelt.de/documents/datenblatt/A300/93AA66_93LC66_93C66-MIC.pdf.

[2] *AX88772B datasheet*. April 12, 2023. December 23, 2021. URL: https://www.asix.com.tw/en/product/USBEthernet/High-Speed_USB_Ethernet/AX88772B.

[3] *AX88772BLI/Typical System Block Diagrams*. April 12, 2023. January 21, 2015. URL: http://www.datasheet-pdf.com/PDF/AX88772BLI-Datasheet-ASIX-1303646.

[4] *Convert ASIX AX88772 to D-Link DUB-E100 for MIB2 hacking*. July 30 , 2023. August 19, 2021. URL: https://www.youtube.com/watch?v=NGaXMYTP_YA.

[5] *HFBR -5701L datasheet*. July 30 , 2023. August 19, 2021. URL: https://www.digikey.co.uk/htmldatasheets/production/1799966/0/0/1/hfbr-5701l-lp.html.

[6] *LM-117 datsheet*. July 30 , 2023. August 19, 2021. URL: https://asset.conrad.com/media10/add/160267/c1/-/en/001184700DS01/datenblatt-1184700-stmicroelectronics-ld1117s33ctr-spannungsregler-linear-sot-223-positiv-fest-800-ma.pdf.

[7] *LM-117 datsheet*. July 30 , 2023. August 19, 2021. URL: https://asset.conrad.com/media10/add/160267/c1/-/en/001184700DS01/datenblatt-1184700-stmicroelectronics-ld1117s33ctr-spannungsregler-linear-sot-223-positiv-fest-800-ma.pdf.

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2. I hereby declare that I have written this master thesis independently, have not submitted it elsewhere for examination purposes, have not used any sources or aids other than those indicated, and have labelled quotations as such.

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Student ID:	3330180
Study Programme:	Master - Electrical and Microsystems Engineering
Supervisor:	Prof. Dr. Thomas Fuhrmann