State Transition Diagram

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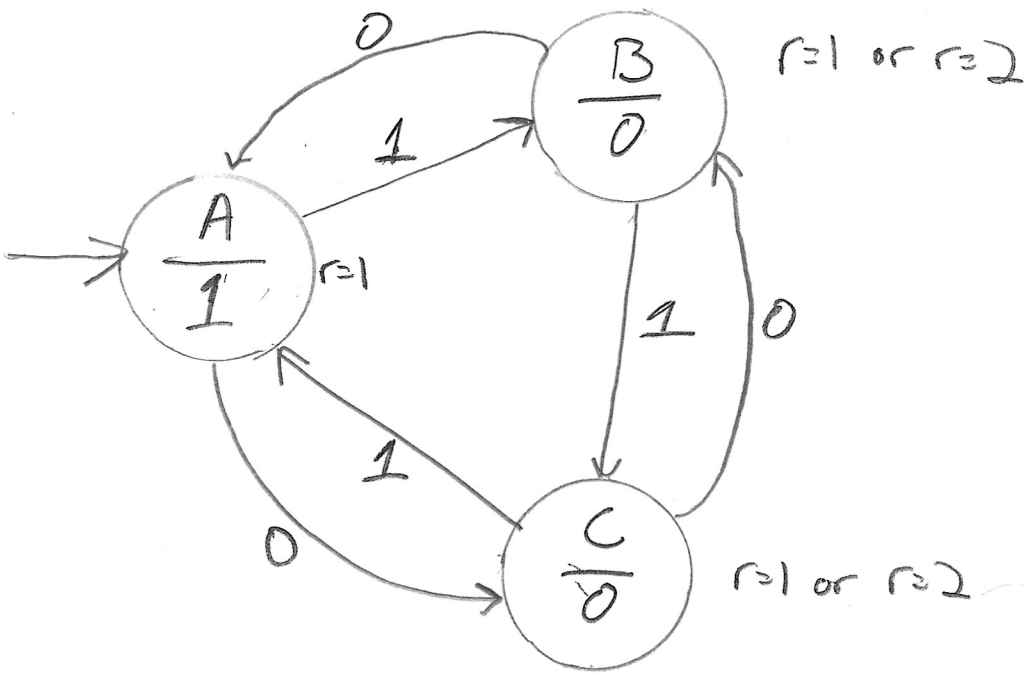
Computer Architecture
Homework 5



Description of states

A: the difference of 0's and 1's is a multiple of 3, r=0, output 1

B: the difference of 0's and 1's is not a multiple of 3, r=1 or r=2, output 0

C: the difference of 0's and 1's is not a multiple of 3, r=1 or r=2, output 0

State transition diagram

Current state	Input	Next State
A	0	C
A	1	B
B	0	A
B	1	C
C	0	B
C	1	A

Output Table

Current State	Output
A	1
B	0
C	0

State Encoding

	S_1	S_0
States A:	0	0
B:	0	1
C:	1	0

After State Encoding — state transition table

Current state S_1	Current state S_0	Input I	Next state S_1'	Next state S_0'
0	0	0	1	0
0	0	1	0	1
0	1	0	0	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0

Output table

Current state S_1	Current state S_0	Output Y
0	0	1
0	1	0
1	0	0

K-Maps

K-Map for Y:

S_1 \ S_0	0	1
0	(1)	0
1	0	X

$Y = \bar{S_0}\bar{S_1}$

K-Map for S_1':

I \ S_1S_0	00	01	11	10
0	(1)	0	X	0
1	0	(1	X)	0

$S_1' = S_0I + \bar{S_1}\bar{S_0}\bar{I}$

K-Map for S_0':

I \ S_1S_0	00	01	11	10
0	0	0	(X	1)
1	(1)	0	X	0

$S_0' = \bar{S_1}\bar{S_0}I + S_1\bar{I}$

Moore FSM Circuit Schematic