Automatic Pipeline Register Placement Through Backannotation in Chisel

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Abstract

We improve the Chisel automatic pipelining tool by automatically optimizing the placement of the pipeline registers. We do this by back annotating Chisel graph nodes with delay data obtained through synthesis and then using this delay information to optimize the placement of the pipeline registers through the use of simulated annealing.

1. Introduction

In the existing automatic pipelining tool, the designer can specify the exact placement of the pipeline registers by labeling particular Chisel nodes as pipeline boundary nodes. Alternatively, the designer can label a small subset of the chisel node graph with pipeline stage numbers and have the automatic pipelining tool infer where to place the pipeline registers. In this second method of pipeline specification, the tool will pick some legal pipeline register placement without considering the consequences of the pipeline register placement on critical path delay. A pipeline register placement is legal if every combinational logic node has all of its inputs in the same pipeline stage.

In the second method of specification, we want to automatic pipelining tool to be able to infer not only a legal pipeline register placement, but also a pipeline register placement that optimizes the critical path delay. This will allow the designer to be able to create a well-balanced pipelined design without going repeatedly going through the vlsi design tools to get feedback on critical path length. Combined with ability of the automatic pipelining tool to automatically generate control logic, the designer will be able to very quickly explore the design space of different pipeline depths and hazard

2. Related Works

[1]

3. Project Objectives

4. Technical Approach

5. Results

6. Conclusion and Future Work

References

[1] J. Bachrach, H. Vo, B. Richards, Y. Lee, A. Waterman, R. Avižienis, J. Wawrzynek, and K. Asanović. Chisel: constructing hardware in a scala embedded language. In *Proceedings of the 49th Annual Design Automation Conference*, DAC '12.