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Lab 3 – Traffic Light

Introduction

The focus of this lab was to design a traffic light controller that uses two different state machines. Using the same counter used in the previous lab, we were assigned to create different time periods for each light sequence and depending on user input via the switches, the time periods could be altered.

Theory of Operation - Requirements

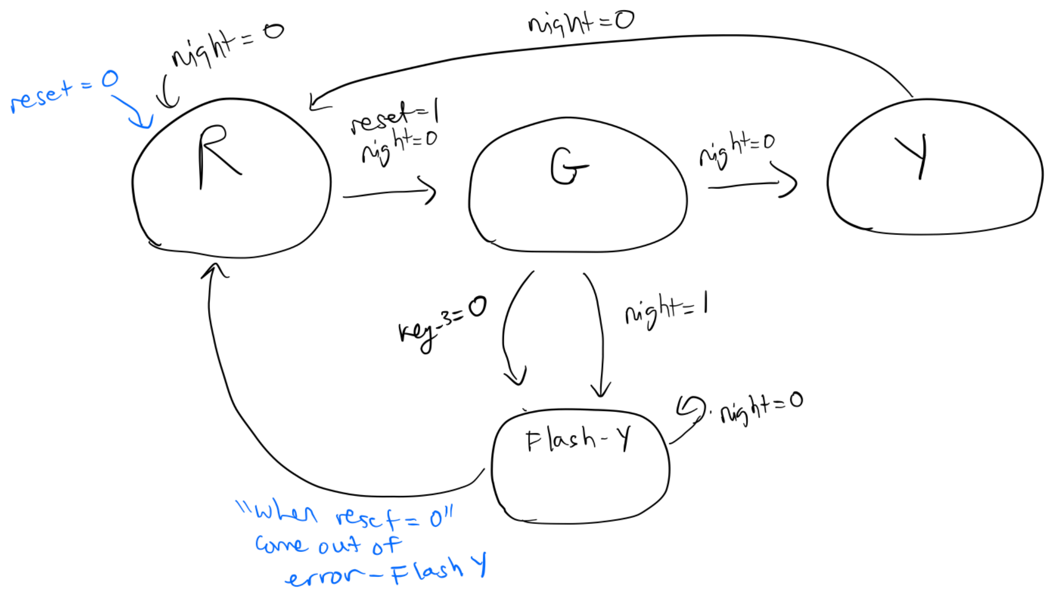
- Uses two state machines, one for north/south and east/west.
    - NS:
        - Green – 7.5 or 10 seconds depending on SW8
        - Yellow – 1.5 seconds
        - Red – east/west green + yellow
        - When KEY(0) is a logic ‘0’ -> reset state, default to red, when reset key is pressed off, transitions to Red.
        - HEX0 is used to display the current light
        - When SW9 is a logic ‘1’ -> night mode, NS will flash yellow every second.
            - Only transition into night mode coming from a green state,
            - Transition back to green state when coming out of night mode.
        - When KEY(3) is a logic ‘0’, transition to error mode using capture and hold method.
            - Only transition into error mode coming from a green state,
            - Can only leave error mode on reset only
    - EW:
        - Green – 5.25 seconds
        - Yellow – 1.75 seconds
        - Red – North/South Green + yellow, notice if SW8 is 1, the red duration for EW will be longer
        - When KEY(0) is a logic ‘0’ -> reset state, default to red, when reset key is pressed off, stays on Red≥
        - HEX5 is used to display the current light
        - When SW9 is a logic ‘1’ -> night mode, NS will flash red every second.
            - Only transition into night mode coming from a yellow state,
            - Transition to red state when coming out of night mode.

- When KEY(3) is a logic ‘0’, transition to error mode using capture and hold method.
    - Only transition into error mode coming from a yellow state,
    - Can only leave error mode on reset only

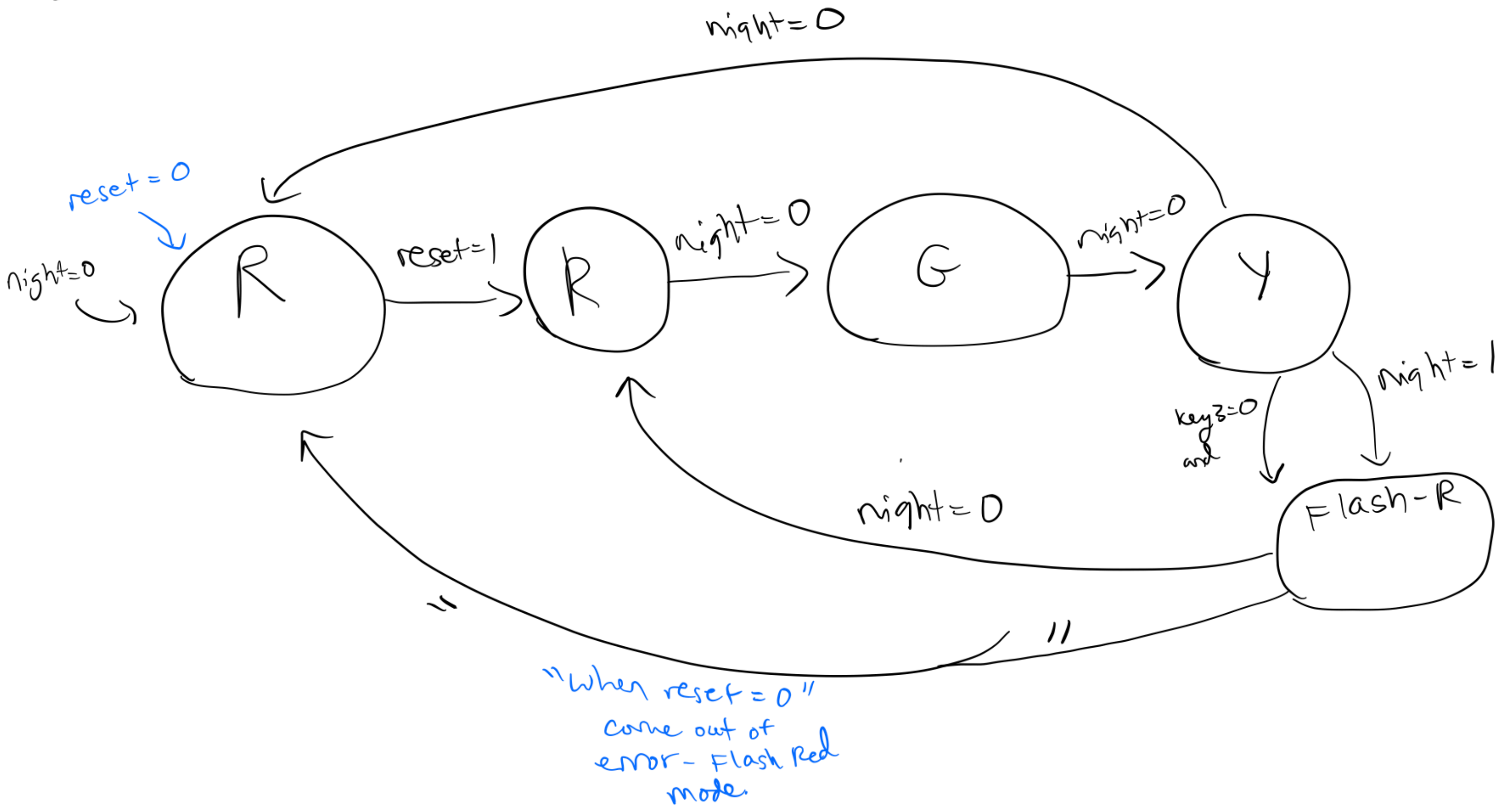
Theory of Operation – State Diagram

The North/South state diagram is broken up into 4 states; Red, Green, Yellow, Flash Yellow. The East/West state diagram is broken up into 4 states; Red, Green, Yellow, Flash Red, in the actual diagram 5 states are shown, but in reality, it is only 4. This is done to show that E/W controller should stay at a Red after coming out from reset. As described in the theory of operation section, night mode and error mode are shown in each state diagram.

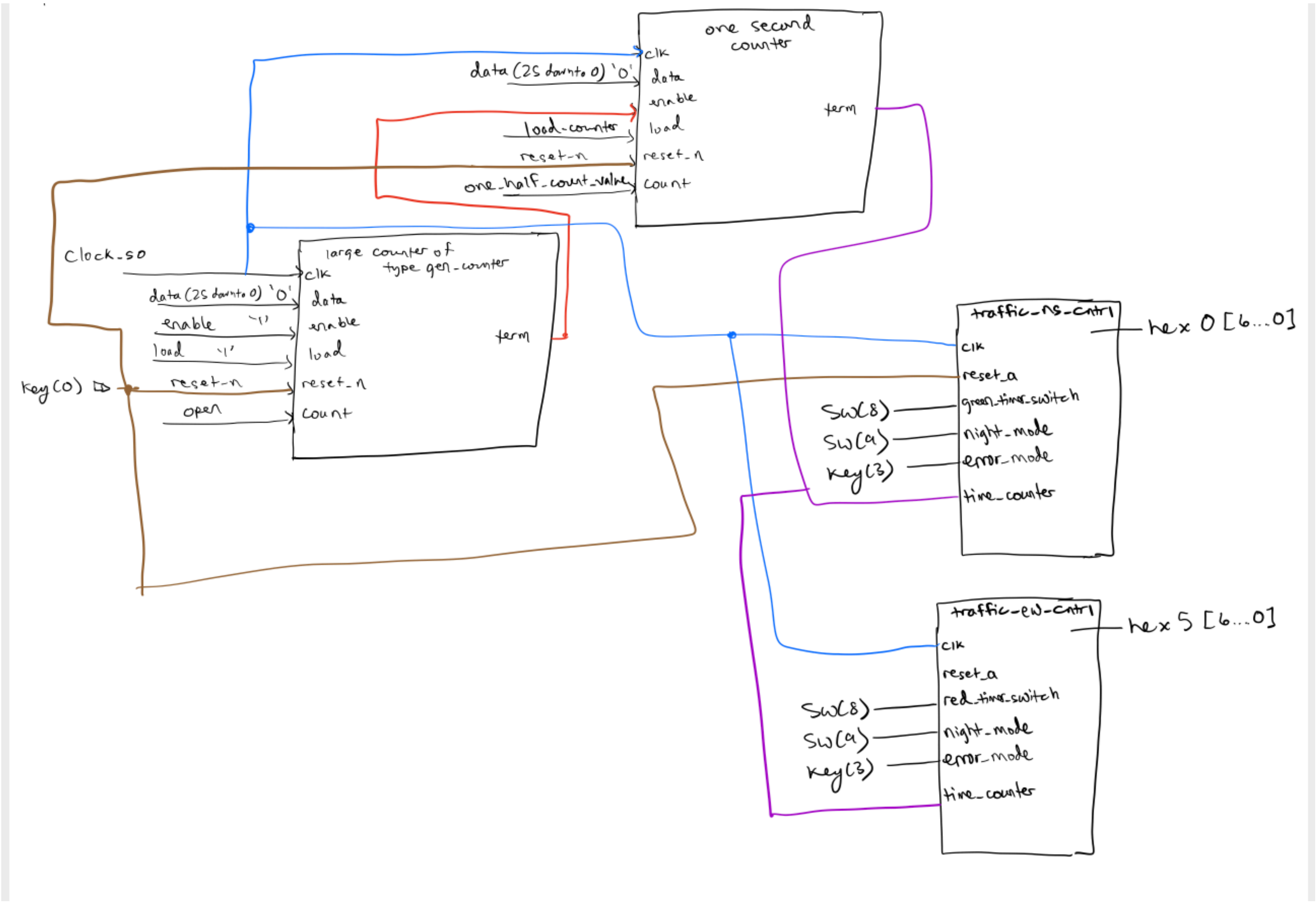
State Diagram – N/S



State Diagram – E/W



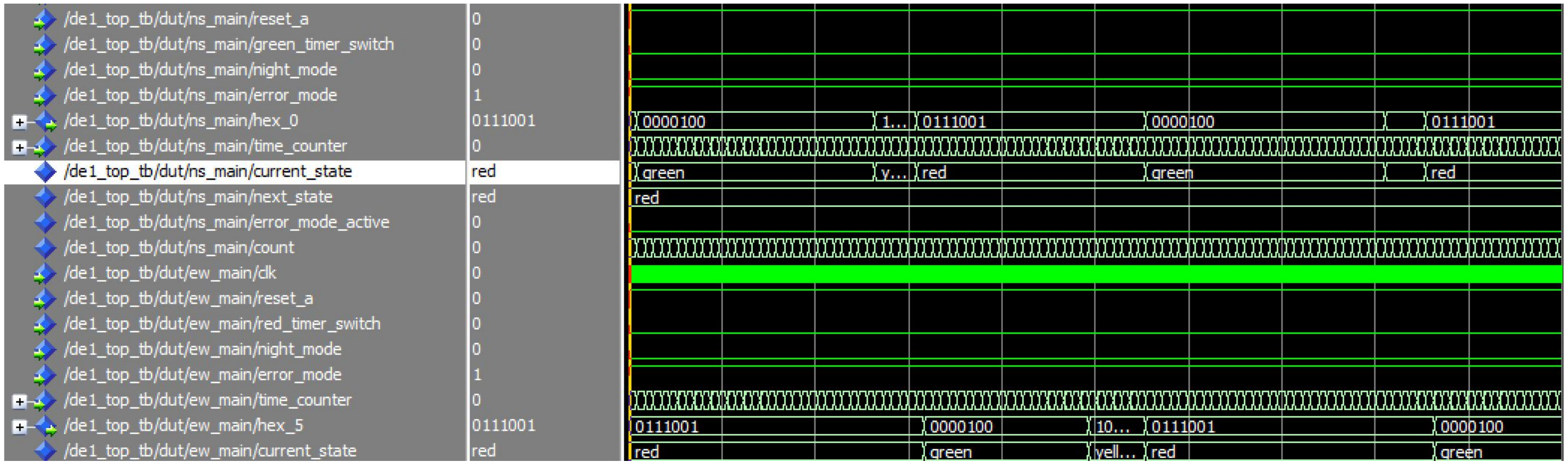
Block Diagram



Verification – Test Plan

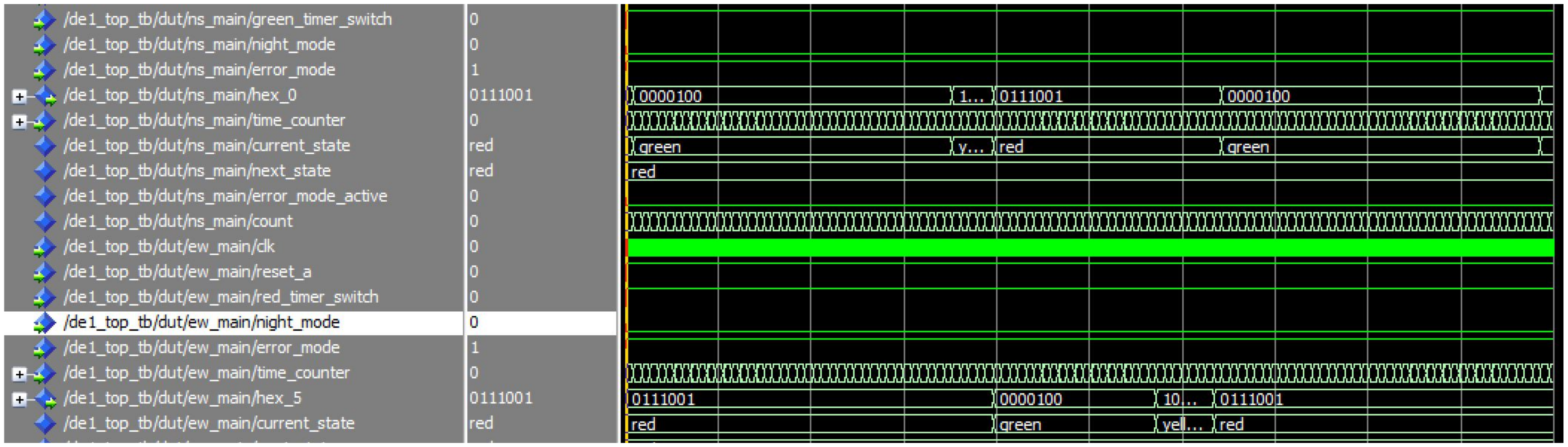
To test the design of this lab, the following will be tested in this order.

1. Start at the default state – high traffic mode off, night and error mode all off



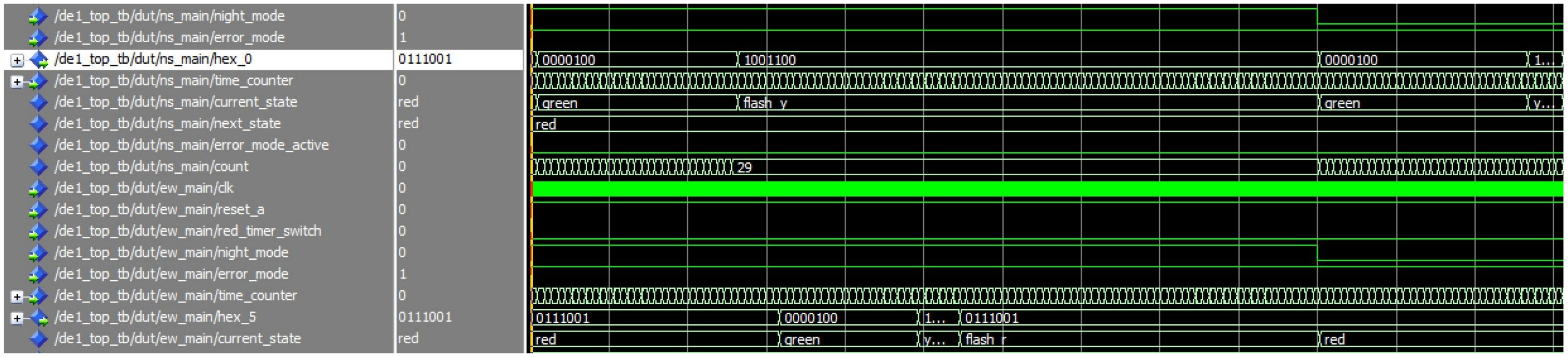
```
/de1_top_tb/dut/ns_main/reset_a             0
/de1_top_tb/dut/ns_main/green_timer_switch  0
/de1_top_tb/dut/ns_main/night_mode          0
/de1_top_tb/dut/ns_main/error_mode          1
/de1_top_tb/dut/ns_main/hex_0               0111001
/de1_top_tb/dut/ns_main/time_counter        0
/de1_top_tb/dut/ns_main/current_state       red
/de1_top_tb/dut/ns_main/next_state          red
/de1_top_tb/dut/ns_main/error_mode_active   0
/de1_top_tb/dut/ns_main/count               0
/de1_top_tb/dut/ew_main/clk                 0
/de1_top_tb/dut/ew_main/reset_a             0
/de1_top_tb/dut/ew_main/red_timer_switch    0
/de1_top_tb/dut/ew_main/night_mode          0
/de1_top_tb/dut/ew_main/error_mode          1
/de1_top_tb/dut/ew_main/time_counter        0
/de1_top_tb/dut/ew_main/hex_5               0111001
/de1_top_tb/dut/ew_main/current_state       red
```

2. Next test high traffic mode – N/S green should last 10 seconds, and E/W red - 11.5 seconds



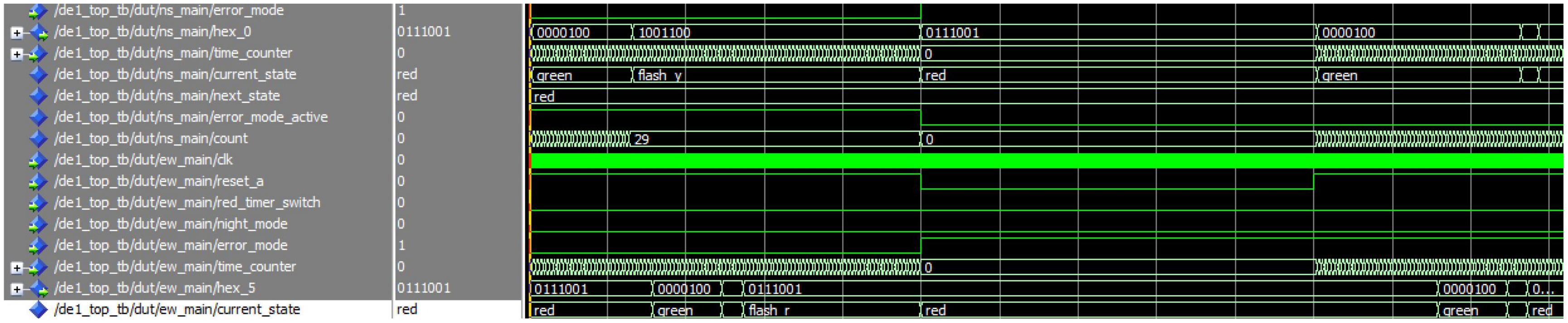
```
/de1_top_tb/dut/ns_main/green_timer_switch  0
/de1_top_tb/dut/ns_main/night_mode          0
/de1_top_tb/dut/ns_main/error_mode          1
/de1_top_tb/dut/ns_main/hex_0               0111001
/de1_top_tb/dut/ns_main/time_counter        0
/de1_top_tb/dut/ns_main/current_state       red
/de1_top_tb/dut/ns_main/next_state          red
/de1_top_tb/dut/ns_main/error_mode_active   0
/de1_top_tb/dut/ns_main/count               0
/de1_top_tb/dut/ew_main/clk                 0
/de1_top_tb/dut/ew_main/reset_a             0
/de1_top_tb/dut/ew_main/red_timer_switch    0
/de1_top_tb/dut/ew_main/night_mode          0
/de1_top_tb/dut/ew_main/error_mode          1
/de1_top_tb/dut/ew_main/time_counter        0
/de1_top_tb/dut/ew_main/hex_5               0111001
/de1_top_tb/dut/ew_main/current_state       red
```

3. Next, test the operation of night mode on and off, notice N/S transitions from green state, and E/W waits till yellow state first before transitioning to flash red.



```
/de1_top_tb/dut/ns_main/night_mode            0
/de1_top_tb/dut/ns_main/error_mode            1
/de1_top_tb/dut/ns_main/hex_0                 0111001
/de1_top_tb/dut/ns_main/time_counter          0
/de1_top_tb/dut/ns_main/current_state         red
/de1_top_tb/dut/ns_main/next_state            red
/de1_top_tb/dut/ns_main/error_mode_active     0
/de1_top_tb/dut/ns_main/count                 0
/de1_top_tb/dut/ew_main/clk                   0
/de1_top_tb/dut/ew_main/reset_a               0
/de1_top_tb/dut/ew_main/red_timer_switch      0
/de1_top_tb/dut/ew_main/night_mode            0
/de1_top_tb/dut/ew_main/error_mode            1
/de1_top_tb/dut/ew_main/time_counter          0
/de1_top_tb/dut/ew_main/hex_5                 0111001
/de1_top_tb/dut/ew_main/current_state         red
```

4. Next, test error mode on and error mode off via reset. Notice, N/S transitions to error mode from green state, and when the error mode is off via reset, it set to red state, then when reset is no longer being pressed, transitions to green state. Likewise, E/W transitions to error mode from yellow state, and when the error mode is off via reset, it set to red state, then when reset is no longer being pressed, transitions to red state, and at the appropriate time, it transitions to the green state and on.



```
/de1_top_tb/dut/ns_main/error_mode            1
/de1_top_tb/dut/ns_main/hex_0                 0111001
/de1_top_tb/dut/ns_main/time_counter          0
/de1_top_tb/dut/ns_main/current_state         red
/de1_top_tb/dut/ns_main/next_state            red
/de1_top_tb/dut/ns_main/error_mode_active     0
/de1_top_tb/dut/ns_main/count                 0
/de1_top_tb/dut/ew_main/clk                   0
/de1_top_tb/dut/ew_main/reset_a               0
/de1_top_tb/dut/ew_main/red_timer_switch      0
/de1_top_tb/dut/ew_main/night_mode            0
/de1_top_tb/dut/ew_main/error_mode            1
/de1_top_tb/dut/ew_main/time_counter          0
/de1_top_tb/dut/ew_main/hex_5                 0111001
/de1_top_tb/dut/ew_main/current_state         red
```

The tests do cover a good amount of cases and edge cases, especially the last one. Also, the simulation tests, do work on the actual board.

Conclusion

Just like lab 2, I started this lab with a rocky start, I had the state diagrams designed, however getting the timing working was very challenging. Originally, I was using several counters for each time frame, however that become way too complicated way to fast. Thus, I transitioned to only using one counter (one second counter) and using if statements to check for specific time limits. This was also a bit complicated because there were several if statements, keeping track of the structure was difficult. I had to adjust my logic several times before I finally got it functioning as planned.

This lab really thought me how to use more than one state machine and have them wait on each other based on time. Also, it thought me how to troubleshoot design flaws. Overall, I believe this lab was a success, I learned a lot.