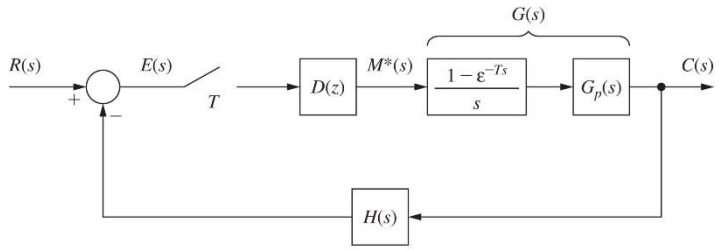
Digital Control Systems (MECE.743) **NAME:**_____

Final Exam (take-home) **Assigned: May 6, 2016**

Due: May 13, 2016 (4pm)



$$G_p(s) = \frac{20(s+20)}{(s^4 + 106s + 605s + 500)} \qquad H(s) = 1$$

1. Consider the feedback control system shown in the figure where the sampling time is T=0.1.
   a. Determine the system pulse transfer function (by hand) *C/M(z)* and verify with Matlab. Simulate the open loop system unit step response.
   b. By hand sketch the root locus for the closed loop system when subject to proportional control only ($D(z)=K_{prop}$). Verify root locus by Matlab.
   c. Determine the gain (K_{prop}) for
      i. a critically damped system response.
         1. Simulate the closed loop step response *C/R(z)*. Find the rise time, % overshoot, and steady-state error.
         2. Simulate the controller response *M/R(z)*.
      ii. less than 5% steady-state response (if possible)
         1. Simulate the closed loop step response. Find the rise time, % overshoot, and steady-state error.
         2. Simulate the controller response *M/R(z)*.
   d. Using Matlab (cuz I'm nice) find the open loop frequency response (*D(z)=1*)
      i. Matlab will do the conversion for you but it is not in w-domain. Remember $\omega_w=2/T*\tan(\omega*T/2)$
      ii. Determine the gain and phase margin. What is the open loop system bandwidth?
   e. **Goal**: Design a controller *D(z)* that reduces steady-state error to less than 5% when subject to a step input and yields a system damping ratio of $\zeta=0.8$.
      i. Using Matlab find the frequency response of the compensated system (*D(z)G(z)*).
      ii. Check the open loop frequency response (*margin(D(z)G(z)*) to determine if you achieved your phase margin goal.
      iii. Simulate the closed loop step response. Find the rise time, % overshoot, bandwidth, and steady-state error.
      iv. Simulate the controller output to the step response.
   f. **Goal**: To increase the system response, design a controller *D(z)* that yields the fastest system response with less than 5% steady-state error and does NOT saturate the controller above +/- 10.
      i. Determine the frequency response of the compensated system (*D(z)G(z)*)
      ii. Simulate the closed loop step response. Calculate the rise time, % overshoot, bandwidth, and steady-state error. (sliding mode control is NOT allowed)
      iii. Simulate the controller output to the step response.
   g. Plot all three (c, e, f) step response simulations on the same figure with a well-defined legend and uses a table to compile all of the results.

- Provide a summary sheet on Page 1 as to the results of all sections.
- It is understood that you will work individually on this exam.
- You are not allowed to use Matlab controller design tools (e.g. sisotool)
- Please do not come to me and ask if your results are OK. Treat this as an exam not a project.
- No extra time will be granted.