# Chapter 1 - Processors

- 3 Components: Control unit, ALU and registers
- Data path: Instruction operands serve as inputs to the ALU, ALU performs operations and produces output
- Instruction execution: Fetch, decode and execute
- Basic cycle more complex in modern CPUs

1

### Chapter 1 - Design Principles

- Direct execution of instructions by hardware
- Maximize throughput
- Instructions should be easy to decode
- Minimize memory references
- Provide enough registers

Chapter 1 - RISC vs CISC

- Characteristics of RISC:
  - Small instruction set
  - Instruction size constant
  - Simple instructions
  - Requires 1 cycle of the data path
- Characteristics of CISC:
  - Large instruction set
  - Variable instruction size
  - Complex instructions
  - Takes more than 1 cycle to complete

#### Comparison: Intel Pentium II and PowerPC604

| Characteristic    | Pentium II   | PowerPC604     |
|-------------------|--------------|----------------|
| Direct execution  | NO           | YES            |
| Throughput        | VARIES       | VARIES         |
| Decoding          | DIFFICULT    | EASY           |
| Memory references | MANY         | FEW            |
| Registers         | 8 GRs, 8 FRs | 32 GRs, 32 FRs |

### Chapter 1 - Instruction Pipeline

- Execution divided into stages
- Pipeline models
- Speculative and out-of-order execution
- Dependencies: RAW, WAR and WAW

### Chapter 1 - Branch Prediction

- Single bit history
- Saturated counters
- Two-level adaptive algorithm

5

6

# Chapter 1 - Memory

- Bits
- Memory addresses
- Byte ordering: Big and little endian
- Intel: little endian, Arm: little, big endian
- Memory errors: detection and correction

### Chapter 1 - Cache

- Primary memory slow
- Fast memory on CPU very expensive
- Solution: Cache memory
- Frequent memory references resolved from cache
- Locality principle

# Chapter 1 - Access Policies

- Chapter 1 Design and Organization
- Direct mapped
- Set associative
- Fully associative

- Read hit
- Read miss
- Write hit
- Write miss
- Increasing performance

10

### Chapter 1 - Replacement Policies

- Optimal and LRU techniques
- LFU
- Second chance
- Improved second chance
- Effective access time

# Chapter 1 - Secondary Memory

- Capacity vs. cost
- Slow compared to primary memory
- Magnetic disks Access time:
  - 1. Seektime
  - 2. Latency
  - 3. Transfer rate

11 12

Magnetic Disks - Example

A magnetic disk rotates at 7200 RPM and has a transfer rate of 9 MB/second and an average seek time of 7ms. How long does it take (in milliseconds) to retrieve a specific sector assuming that a single sector contains 512 bytes.

- Transfer rate:  $\frac{9 \times 1024 \times 1024}{1000} = 9437.184$  bytes / ms
- Transfer of single sector::  $\frac{512}{9437.184} = 0.0543$  ms
- Latency:  $\frac{1}{2} \times \frac{60}{7200} \times 1000 = 4.17 \text{ ms}$
- Total time: 7 + 4.17 + 0.0543 = 11.22 ms

13

# Chapter 1 - Input and Output

- Communication takes place over bus
- Internal and external buses
- Arbitration
- Bus transactions
- Bus types: ISA, PCI, USB, etc.

# Chapter 1 - IDE en SCSI

- Disk controller used to access disks
- IDE: Only a single disk active
- SCSI: Executes operations in parallel

14

#### Chapter 1 - Communication and Information Trans

- Registers: data, command and status
- I/O instructions and memory-mapped I/O
- Interrupts and polling
- Data transfer: DMA or PIO
- DMA: Transfer data without CPU intervetion. Interrupt generated after transfer
- Cycle Stealing
- PIO: Very slow. Interrupt after every wordsize transfer