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Project #0 Notes

- We learned the basics of Verilog and how to compile then run while doing UUT (Unit Under Testing).
- Verilog doesn't use brackets or indents to separate codeblocks
    - Instead it uses keywords to mark the beginning and end of a codeblock
        - Each module starts with the "module" keyword, and ends with the "endmodule" keyword
- In a testbench file variables are declared with:
    - "reg" for inputs
    - "wire" for outputs
- The variables in Verilog are passed to the modules in parentheses, similarly to the methods(functions)
- When running the TrafficLite example we learned about the clock edge updating state when the clock edge is positive
- The key commands we used were (The commands all are ran in cli):
    - iverilog -o <output file> <input file>
    - vvp <output file>
    - gtkwave (this opens gtkwave)
- The iverilog -o command uses a .v testbench file as input and output a .vvp file
- The vvp command reads the .vvp file and outputs a .vcp file which can be read by gtkwave to visualize the wave
- We also gained understanding of how the code blocks interact and connect with each other (testbench implementation)
- Using gtkwave software we were able to simulate circuit operation
- Verilog modules operate similar to methods(functions) with testbench being a 'main' method.
- When writing a test branch the actual test starts after the "initial being" keywords and ends with the "end" keyword