Yingwei Zheng

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RESEARCH INTERESTS

Compiler (LLVM/MLIR/DSL Compiler)

High-Performance Computing (Automatic offloading/scheduling)

Computer Graphics (High-performance physically based rendering)

EXPERIENCES

PLCT Lab, Institute of Software Chinese Academy of Sciences (Remote) Feb. 2023 - present

- Contribute to LLVM (improve transforms/RISC-V backend)
- Maintain a performance monitoring system for LLVM on RISC-V (https://lnt.rvperf.org)

EDUCATION

2020 - present Bachelor's Degree at Southern University of Science and Technology

Department of Computer Science and Technology (Turing Class) GPA: 3.9/4.0 (3/218)

SKILLS

Programming Languages Modern C++ (8 years), CUDA (7 years)

Compiler Infrastructure LLVM (8 years), MLIR

Graphics API OpenGL/DX11/DX12/Vulkan

AWARDS

Nov. 2021	SC21 Student Cluster Competition Highest LINPACK Benchmark		
	LINPACK Benchmark (1/10)), Overall $(3/10)$	
	Contribution: tune LLNL cardioid and achieve 25% speedup on the NVIDL	5% speedup on the NVIDIA DGX System	
Nov. 2021	2021 APAC HPC-AI Competition 1st Place & AI Special Prize	Overall $(1/36)$	
	Contribution: tune GROMACS with NVIDIA HPC-X MPI Library		
June 2022	ISC 2022 Student Cluster Competition Online Third Place Winne	t Cluster Competition Online Third Place Winner Overall (3/16)	
	Contribution: (Coding Challenge) optimize Xcompact3d and gain up to 7% performance		
	benefits $(0 \rightarrow 46\%$ overlapping rate) on the cluster equipped with NVIDIA	e cluster equipped with NVIDIA Bluefield DPUs	
Nov. 2022	SC22 IndySCC 2nd Place Hero HPL Challenge(2/10	Overall $(2/10)$	
	Contribution: Leader/Cluster Maintainer, HPL/HPCG Benchmark		
Aug. 2023	Special Prize of National Compiler Design Competition for College	al Prize of National Compiler Design Competition for College Students 2023	
	Contribution: Leader/Infrastructure/RISC-V backend RISC	C-V track (1/26)	

HIGHLIGHTED PROJECTS

CMMC: a dependency-free compiler for the course project of Compilers

- Multiple frontends (Spl/SysY2022)
- Multiple backends (TAC/MIPS32r5/RISC-V/ARMv7)
- Produces competitive results compared with LLVM/GCC
- Won the special prize of the National Computer Design Competition for College Students

Piper: a high-performance CPU/GPU physically based renderer

• Spectral rendering (IOR-based dielectric/conductor rendering, dispersion)

- OCIO support (SPD \leftrightarrow XYZ Color Space \leftrightarrow sRGB Color Space)
- Embree/OptiX backend (high-performance ray-tracing with SIMD/RT-Core)
- Custom rendering pipeline (real-time preview/NN-based image denoising)

YAAS: a sub-object OOB detector for the course project of Computer Security

- Full C/C++17 compatibility (RTTI/exceptions/threading/standard libraries)
- LLVM-based Instrumentation (provided as a built-in option in clang)
- Check GEP instead of LD/ST (detect more access violations than Address Sanitizer)
- Not limited to stack/heap objects (mmap/custom allocators/nested allocators)

Hive: a MIPS CPU for the course project of Computer Organization (H)

- Mips32r6 target (most of Integer/FP instructions are supported)
- LLVM-based toolchain
- Modern CPU features (Pipeline/Multiple issue/Out-of-order/Branch prediction/Hardware prefetcher)
- LLVM patch for Hive sub-target to improve instruction scheduling ($\sim 2\%$ speedup)

PotatOS: a tiny RISC-V OS for the course project of Operating Systems (H)

- Written from scratch in modern C++
- SMP support (Work-stealing based scheduler)
- Asynchronous I/O with zero-copy buffers
- Musl libc support

MiniZip: an implementation of deflate for the course project of Algorithm Design And Analysis (H)

- Fine-tuned for Intel Rocket Lake CPU
- Optimal algorithm for length-limited huffman encoding
- up to 7x faster (16 threaded)/12x faster (single-threaded) than 7-zip's standard deflate implementation in the same compression ratio

Last updated: September 15, 2023