Modeling Complex Random Memristor Networks

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NIMS

MANA

National Nanotechnology Coordinated Infrastructure

NSF

Novel Electronics

Computers aren't getting much faster.

(2D photolithographic silicon/CMOS)

search for new computing methods

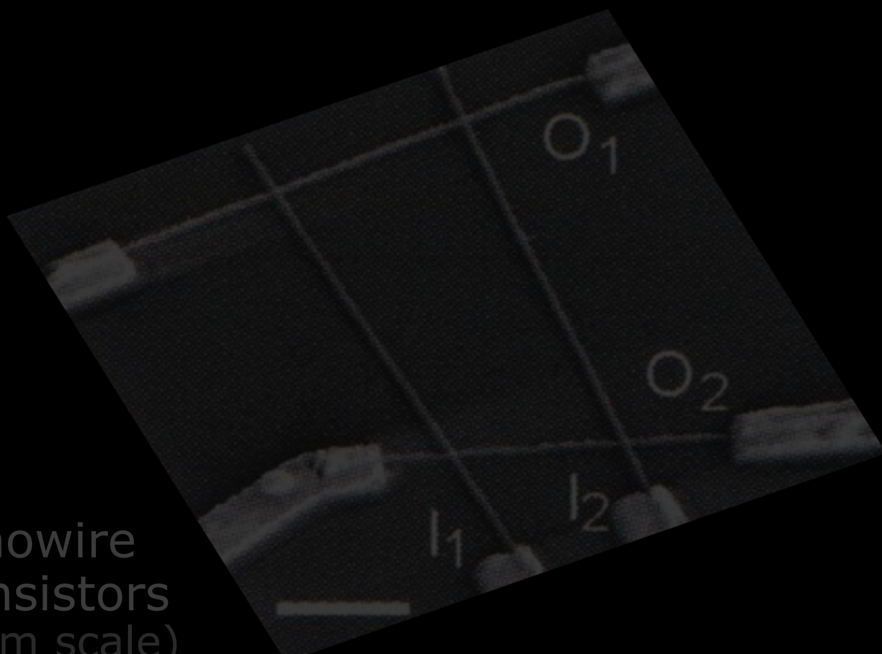
- 3D circuitry
- quantum computing
- programmable hardware (FPGA)
- photonic computing
- neuromorphic computing

(nanowire electronics)

Nanowires for Electronics

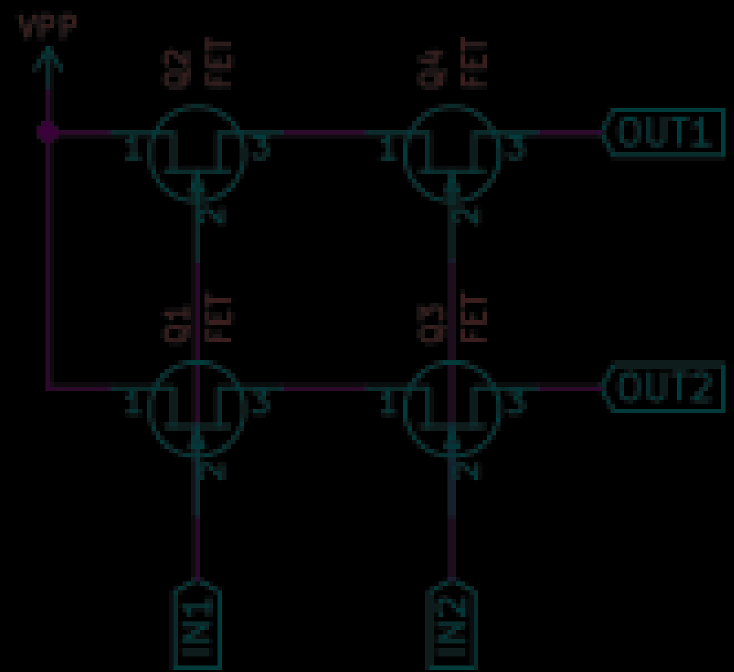
Nanowire (NW): 1D cylinder of Ag, Si, Au...

- NW-NW junction = circuit element



nanowire transistors
(1 μm scale)

equivalent circuit



Zhong, Z., Wang, D., Cui, Y., Bockrath, M. W., & Lieber, C. M. (2003). Nanowire Crossbar Arrays as Address Decoders for Integrated Nanosystems. Science, 302(5649), 1377–1379. https://doi.org/10.1126/science.1090899

PVP@Ag Nanowire Networks

collection of Ag nanowires with PVP coating

- model properties, understand potential
- similar to neural network?

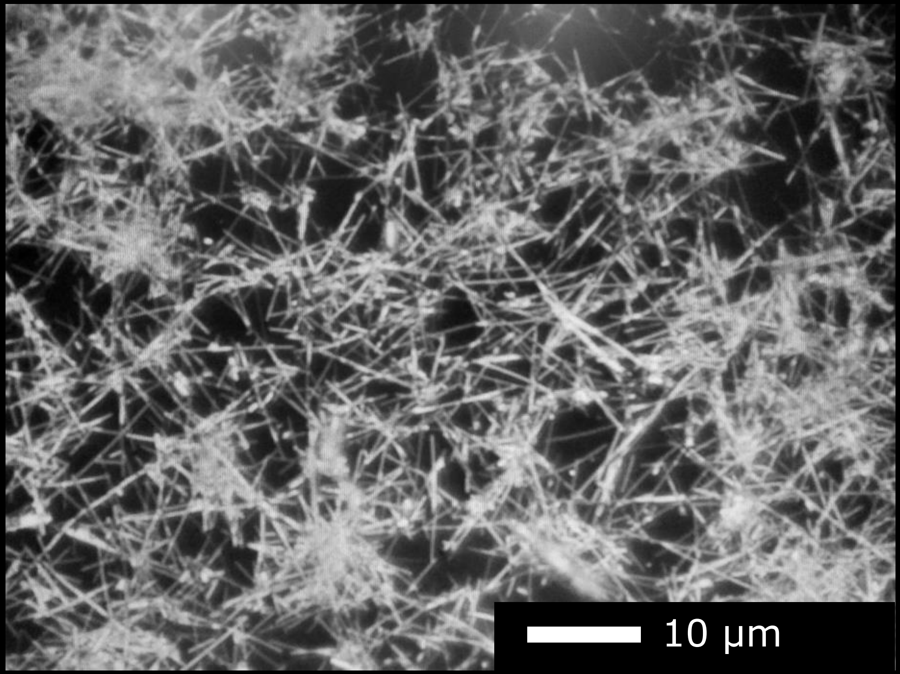
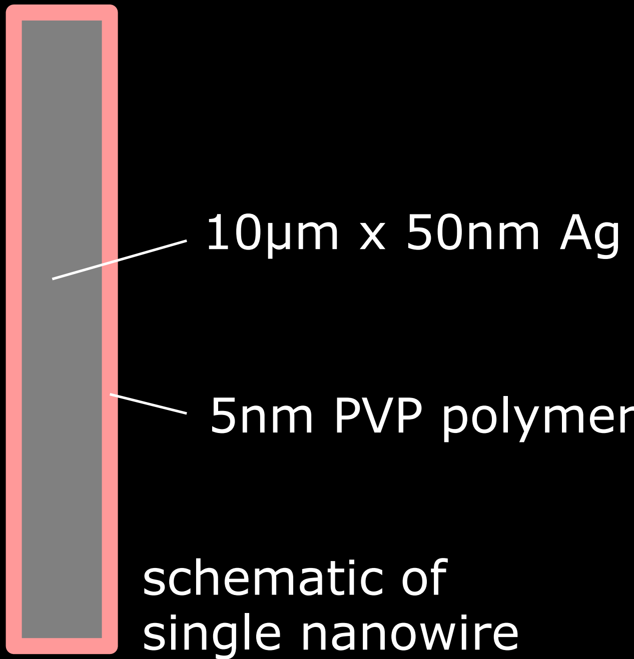
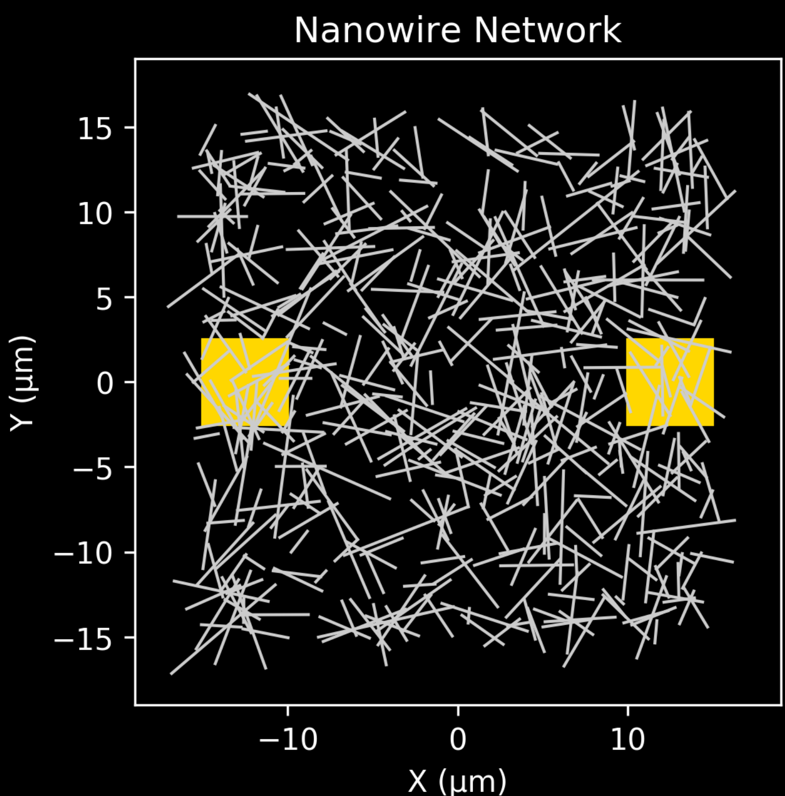


image of a PVP@Ag network

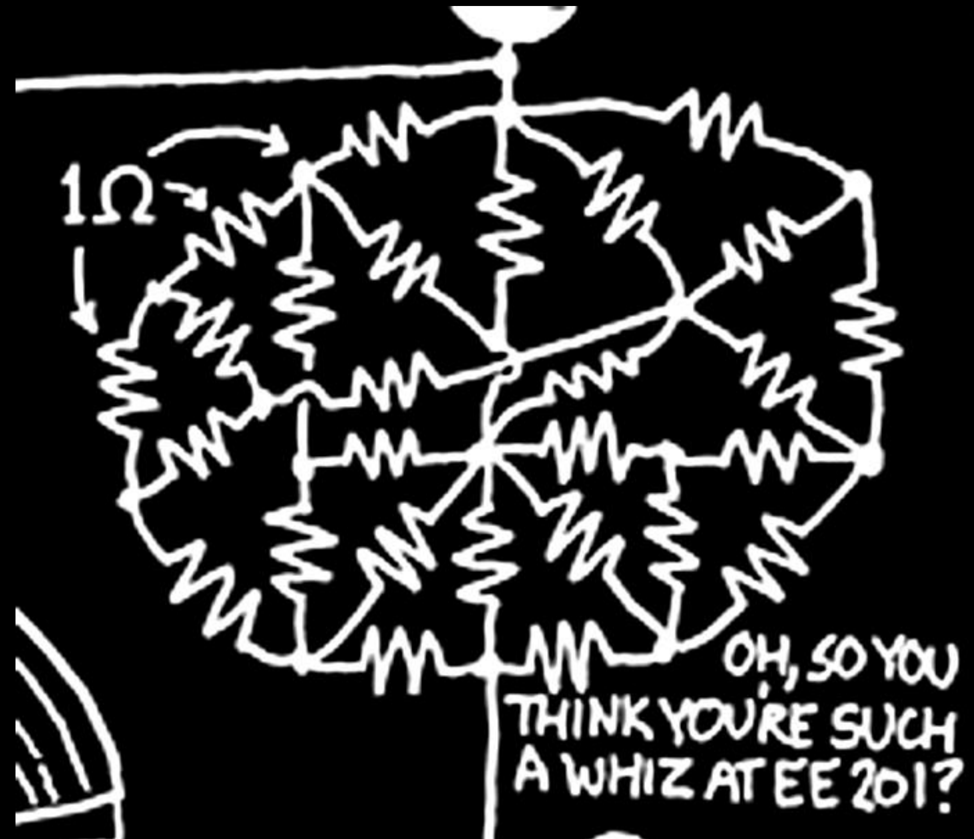


schematic of
single nanowire

Step 1: Create Simulation



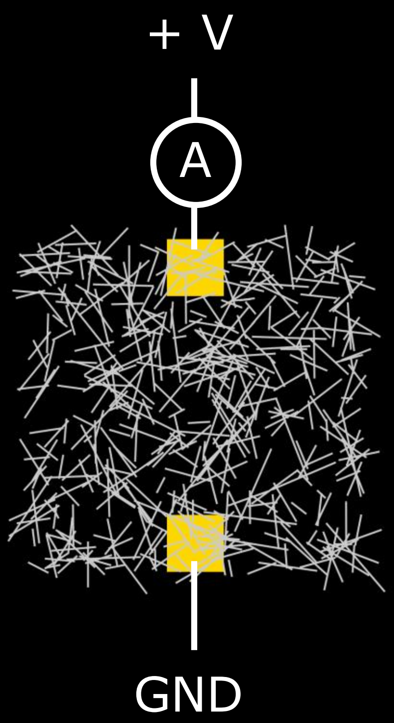
a complete simulated network

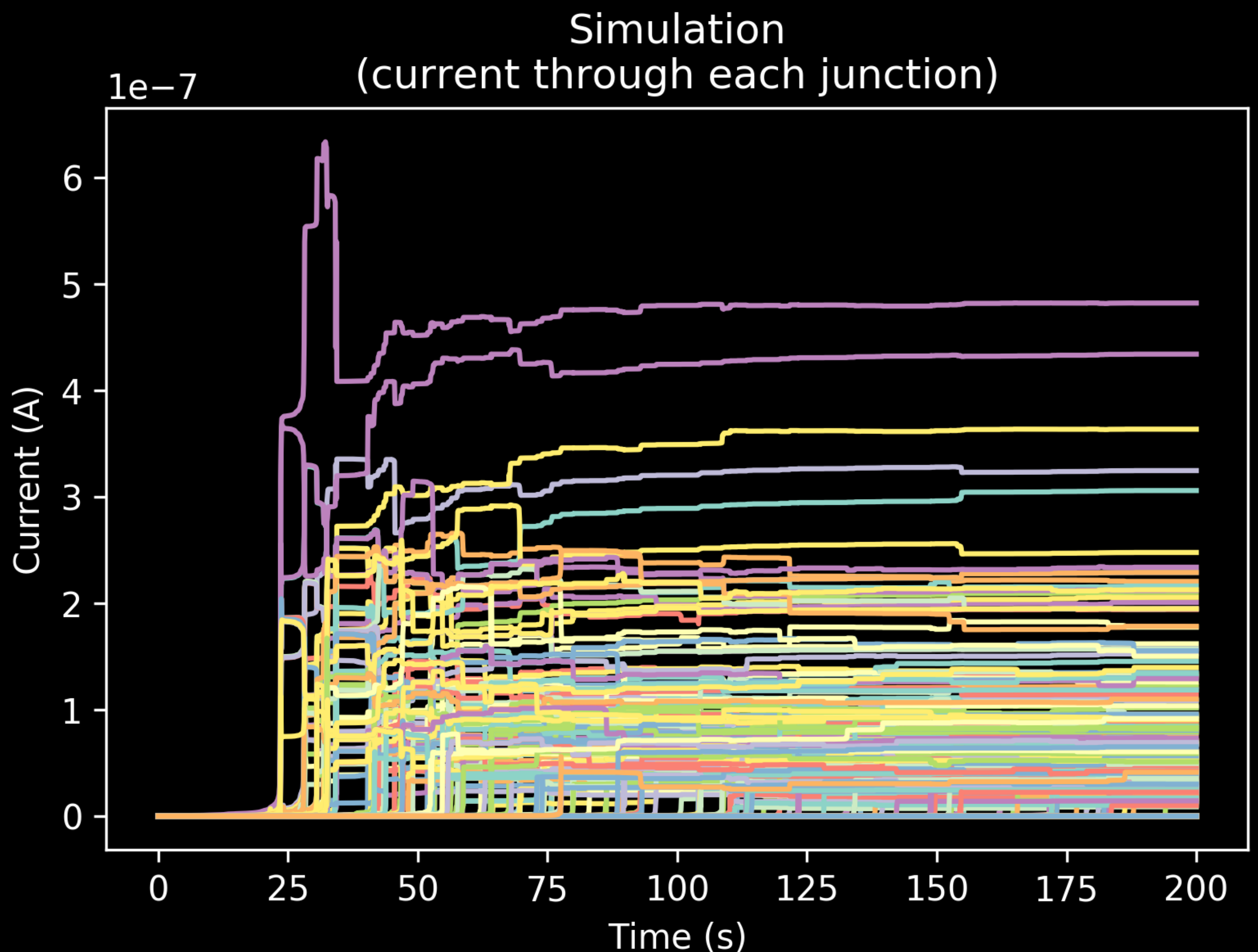


equivalent circuit

Munroe, R. Circuit Diagram. XKCD 730.

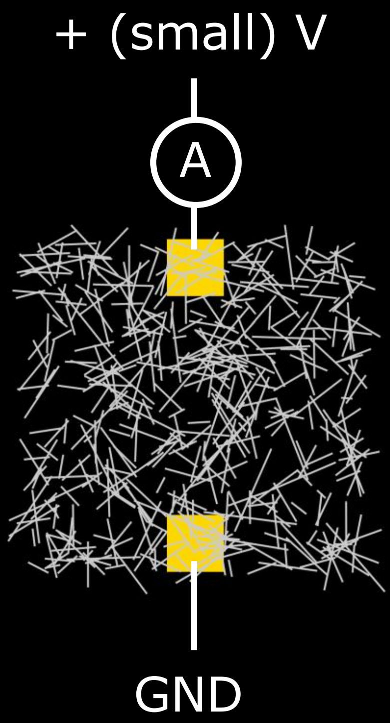
Step 2: Response to Constant Voltage

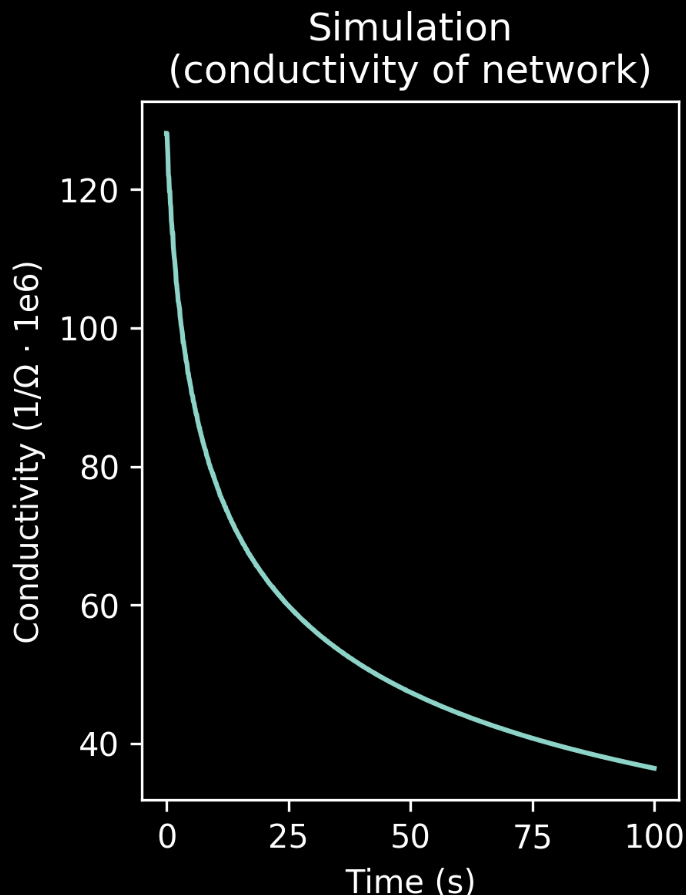


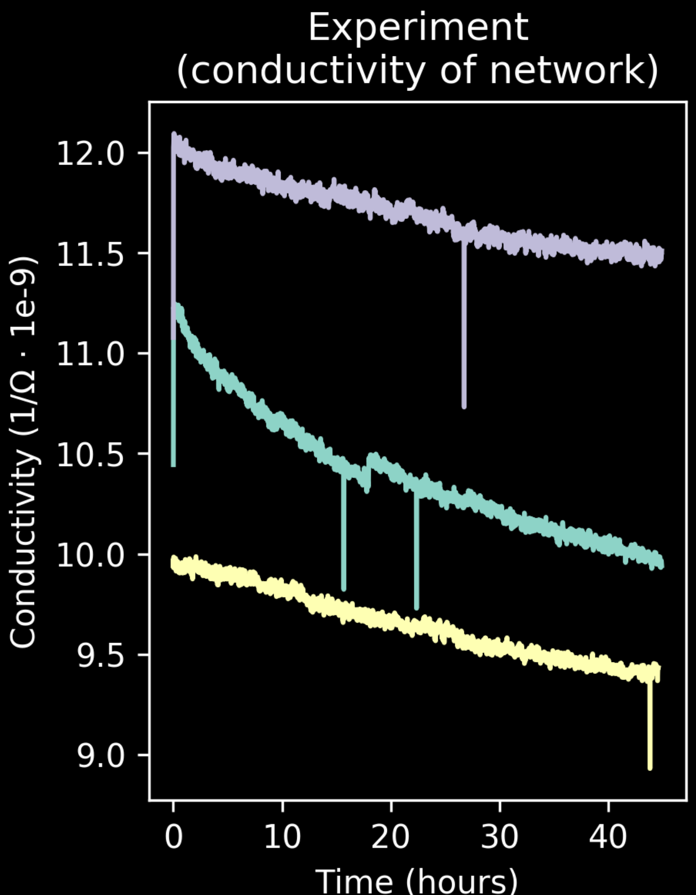


relative current density over time

Step 3: Resistance Decay with Time

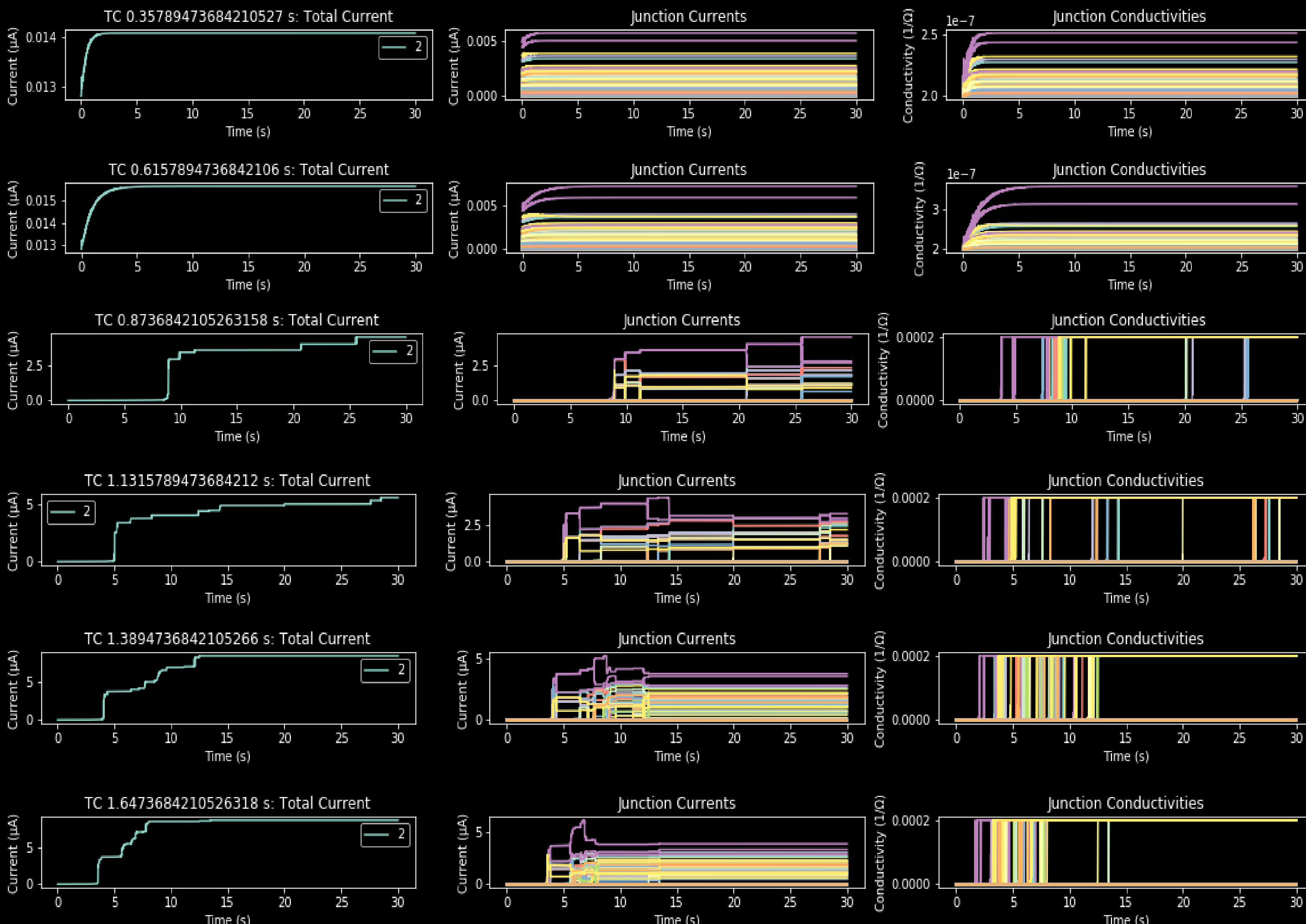




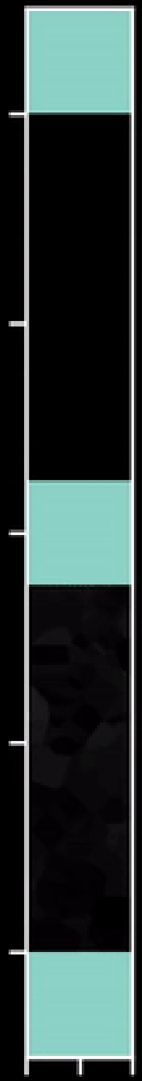


full decay is very slow- weeks!

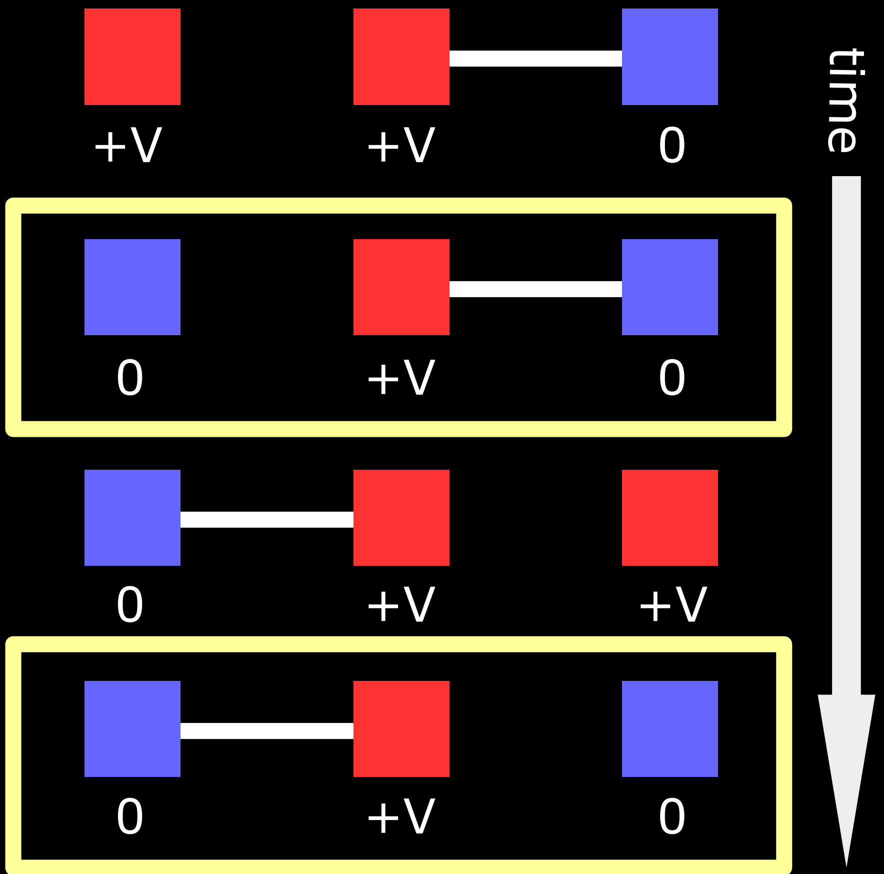
Parameter sweep found nothing else



One use: current switch



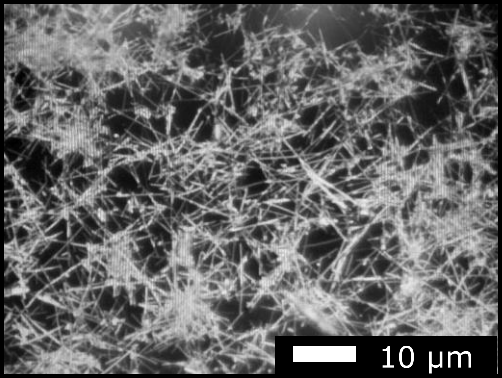
switch simulation



white indicates current flow

Conclusions

- Simulation predicts behavior
- Junction memristor hypothesis supported
- Network acts like planar memristor



Applications:

- Switch for a finite state machine
- Ephemeral memory: information that disappears after a week
- Custom non-CMOS electronics
- Planar memristance

Future work:

- Attempt to control memristor parameters (decay, resistance)
- Add capacitance for higher-order behavior

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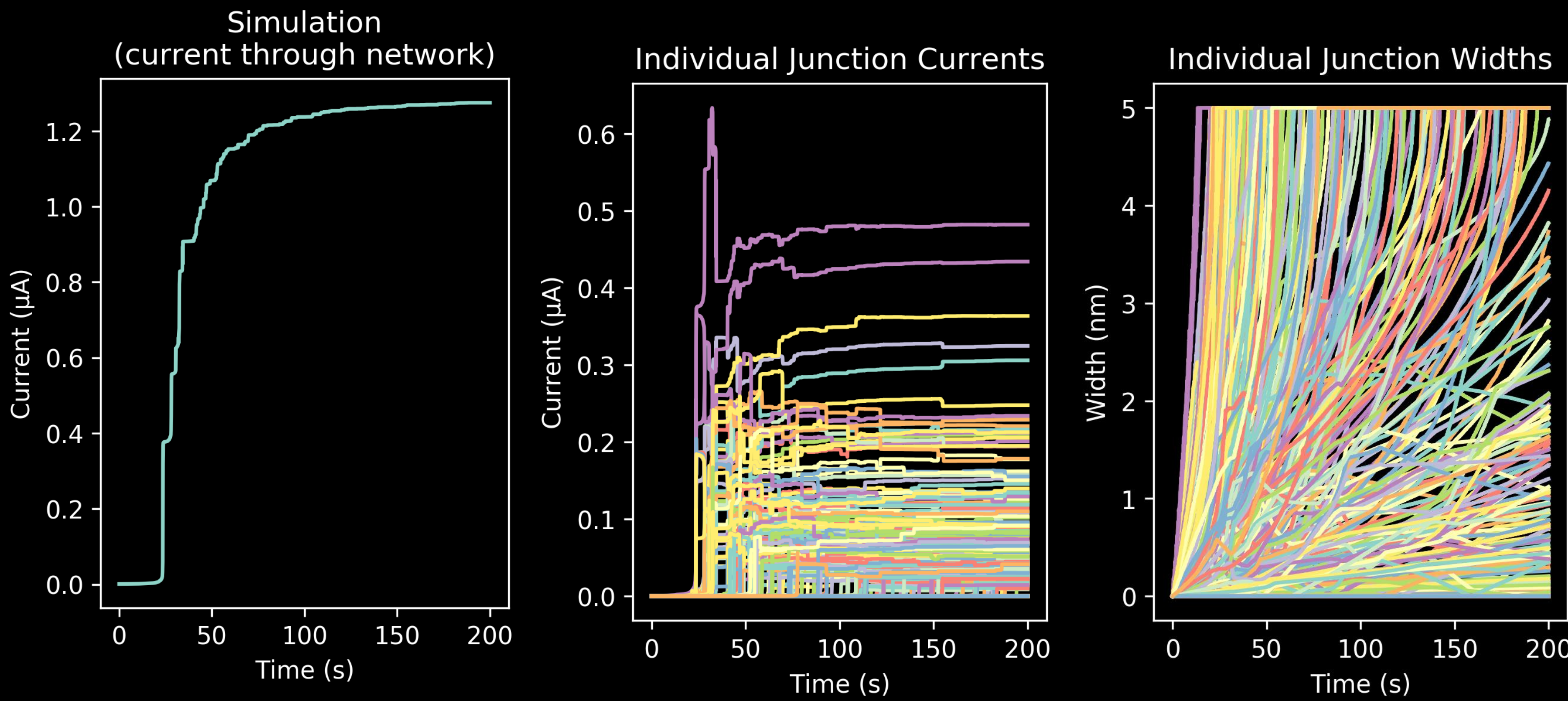
- Nano Functionality Integration Group: Qiao Li, Adrian, Sasaya...
- Dr. Lynn Rathbun and other program coordinators

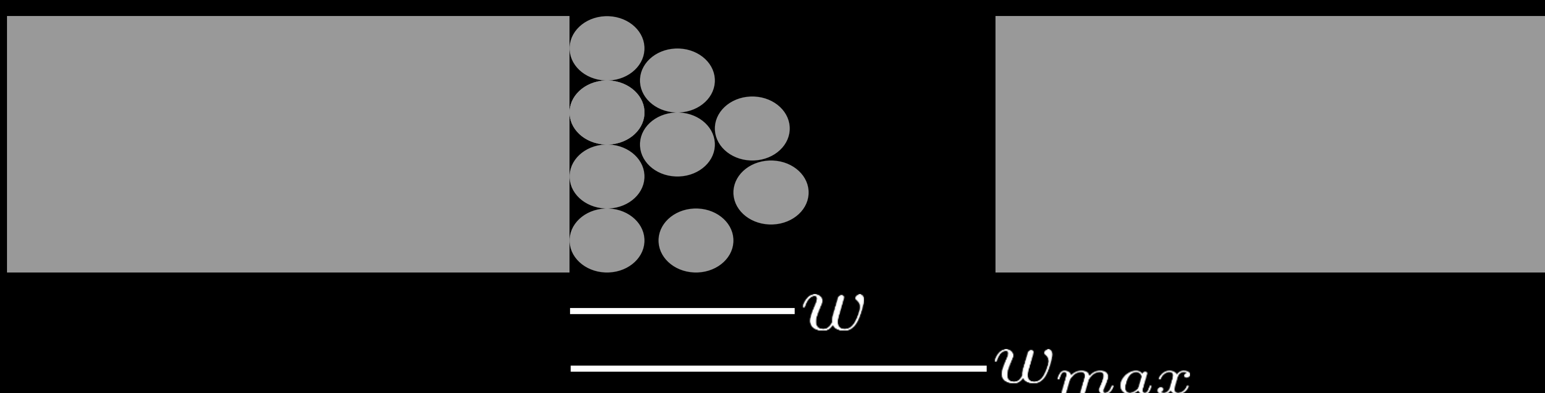
Junction Behavior



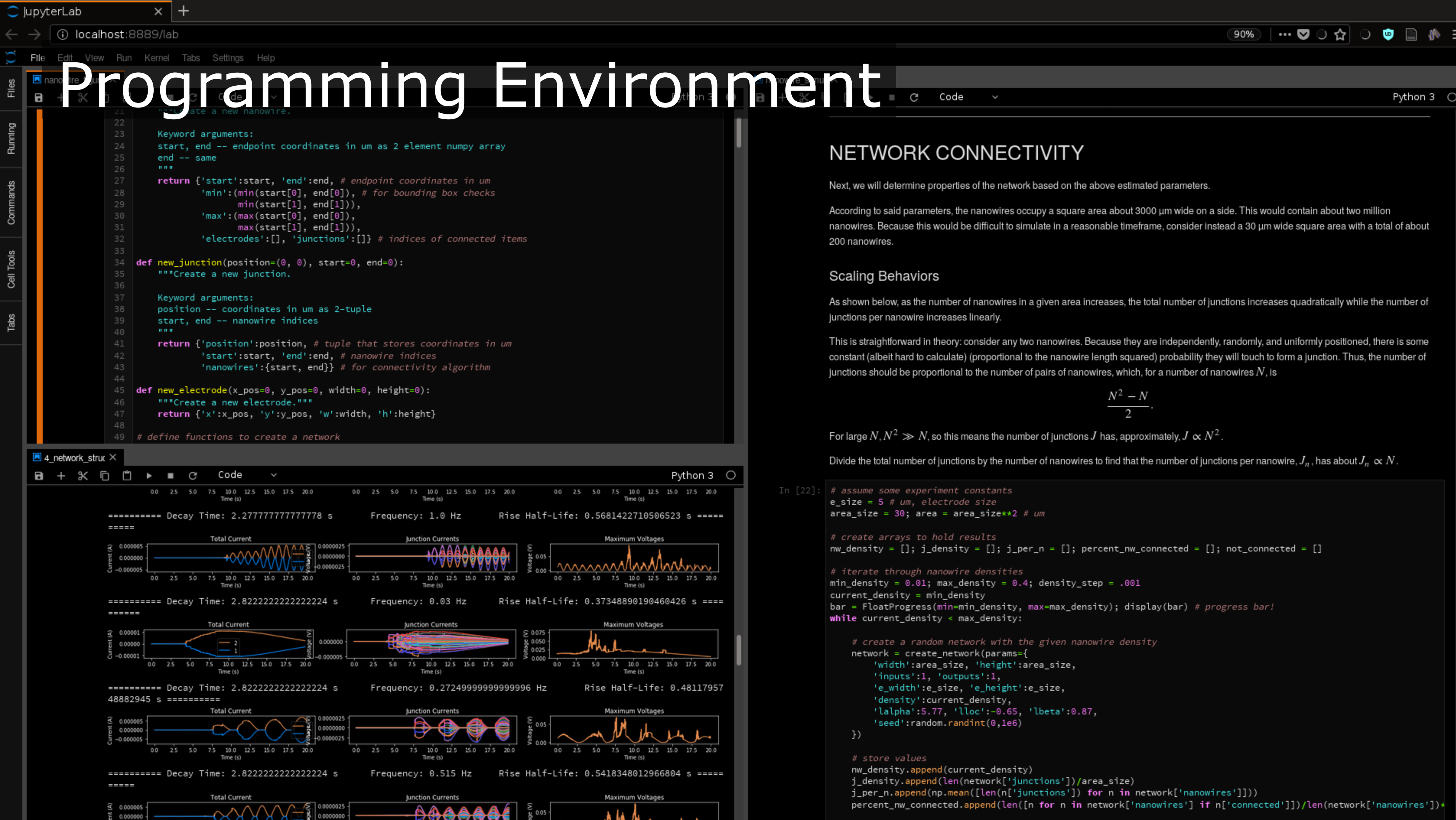
NW-NW Junction Electrical Model

$$V = \left[\frac{w}{w_{max}} \cdot R_{on} + \left(1 - \frac{w}{w_{max}} \right) \cdot R_{off} \right] \cdot I$$

$$\frac{dw}{dt} = \mu_v \cdot \frac{R_{on}}{w_{max}} \cdot |I| - \frac{w}{\tau}$$



Programming Environment



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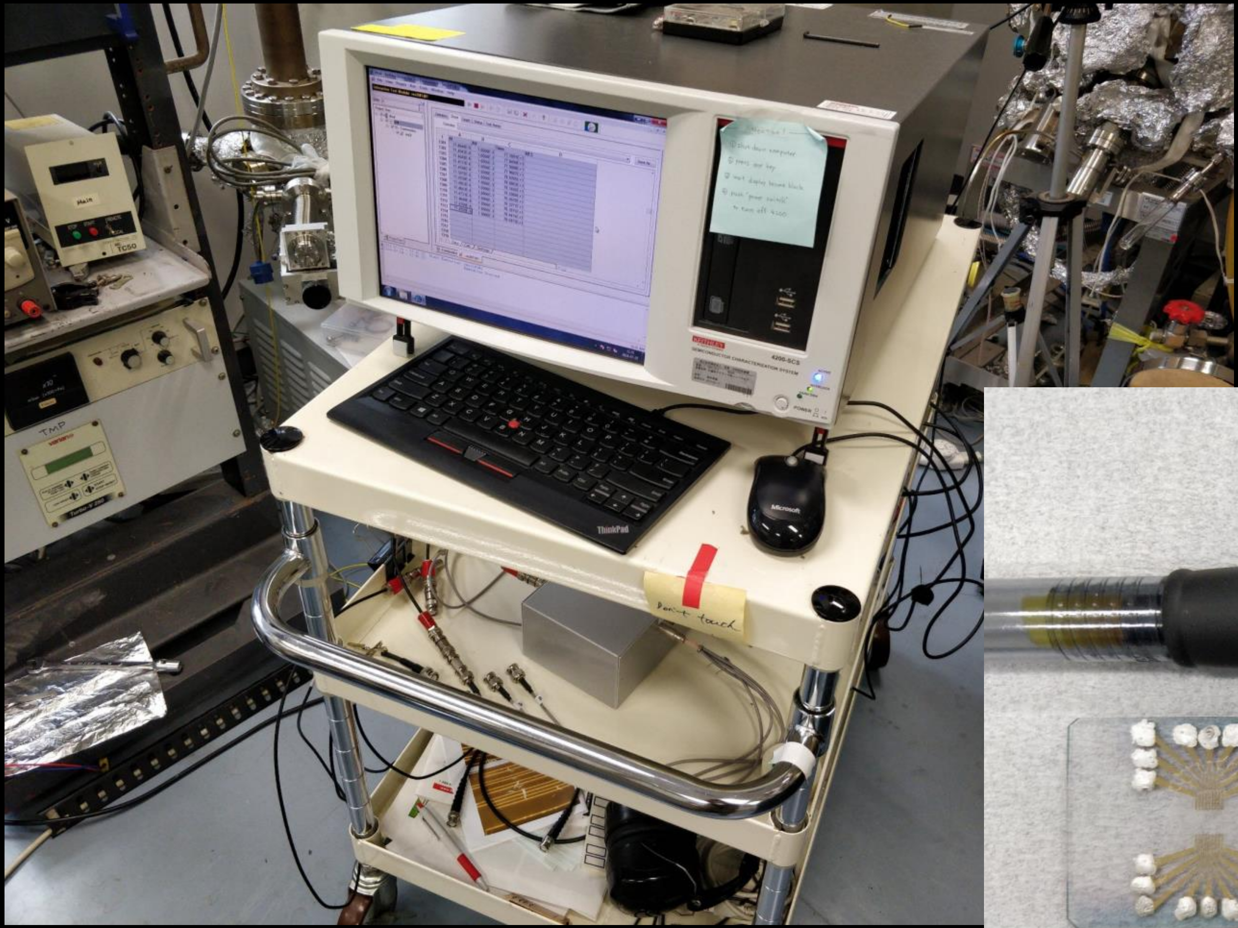
Test Apparatus



Keithley SCS 4200

Test devices