**ECE 374 Lab 6&7: Pipelining**

Due in Lab March 26, 2019

In this lab, you will be required to pipeline the ISA processor into a 5-stage processor. Note that you do not have to address any hazards for this lab. All you have to do is set up the pipeline by incorporating the pipeline registers and reconnecting some of the wires. You have to pipeline both the datapath and the control signals. Refer to Figure 4.51 (textbook page 304), which shows how to setup the pipeline. You can ignore Branch and J instructions for this pipeline.

Following are not required for this lab: Forwarding and hazard-detection-unit (for load use hazards).

**Pre-Lab :** To be done before coming to the lab (CAD simulation). Implement the pipeline by only port mapping the pipeline registers into the top-level file and reconnecting wires as need be. You should not have to do anything else. Do not modify the register file. Test your design using code without data hazards, Branch, or Jump instructions. Use a sequence of about 8 instructions to see if your pipeline is working correctly.

Note that the dest address and RegWrite signal for the RF should come from the WB stage and not from the ID stage.

**Lab:** To be done in the lab (FPGA simulation). Show FPGA simulation to the TA for check off.