**ECE 374 Lab 9: Hazard Detection**

Due in Lab April 23, 2019

**Pre-Lab :** Extend the 5-stage pipelined processor from Lab 8 with hazard detection to handle load-use hazards. The logic for hazard detection is given in page 314. The logic defines how the stall signal is generated. Figure 4.60 (page 316) shows the hazard detection unit. The unit has 3 outputs. Primarily, if the stall signal is one, then PC register and the IF/ID pipeline registers should be stalled. Stalling can be incorporated by introducing a mux in front of the registers that need to be stalled. If stall is asserted, the registers should be updated with their previous value, otherwise, they should take the new value from the input to the register.

Also, if stall is asserted, the ID/EX pipeline registers should be updated with a NOP. This can be achieved by making all the control values in the ID/EX pipeline register “0”. Figure 4.60 shows how to do this.

Test your design with RAW dependencies that trigger both forwarding and hazard detection. CAD simulation is to be done pre-lab. Your test code should have at least one load instruction, which is followed right after by an instruction that uses the value generated by the load instruction.

**Lab:** To be done in the lab (FPGA simulation). Show FPGA simulation to the TA for check off.