The University of Alabama in Huntsville
Electrical & Computer Engineering Department
CPE 431 01
Test II
November 12, 2002

Name: _____

1. (5 points) For an m-stage pipeline, how many cycles does it take to execute n instructions if the pipeline is empty when these instructions begin to execute? _____

2. (10 points) Here is a series of address references given as word addresses: 1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6. Assuming a direct-mapped cache with four-word blocks and a total size of 16 words that is initially empty, (a) label each reference in the list as a hit or a miss and (b) show the final contents of the cache.

3. (1 point) In the _____ stage of the MIPS pipeline, the register file is written.

4. (15 points) Consider two machines with different cache configurations:
   Cache 1: Direct-mapped with two-word blocks
   Cache 2: Direct-mapped with four-word blocks
   The following miss rate measurements have been made:
   Cache 1: Instruction miss rate is 1%, data miss rate is 4%
   Cache 2: Instruction miss rate is 2%, data miss rate is 5%
   For these machines, one-half of the instructions contain a data reference. Assume that the cache miss penalty is 6 + Block size in words. The CPI for this workload was measured on a machine with cache 1 and was found to be 2.0. The cycle time for machine 1 is 1.4 and the cycle time for machine 2 is 1.0 ns. Determine which machine is the fastest and which is the slowest.

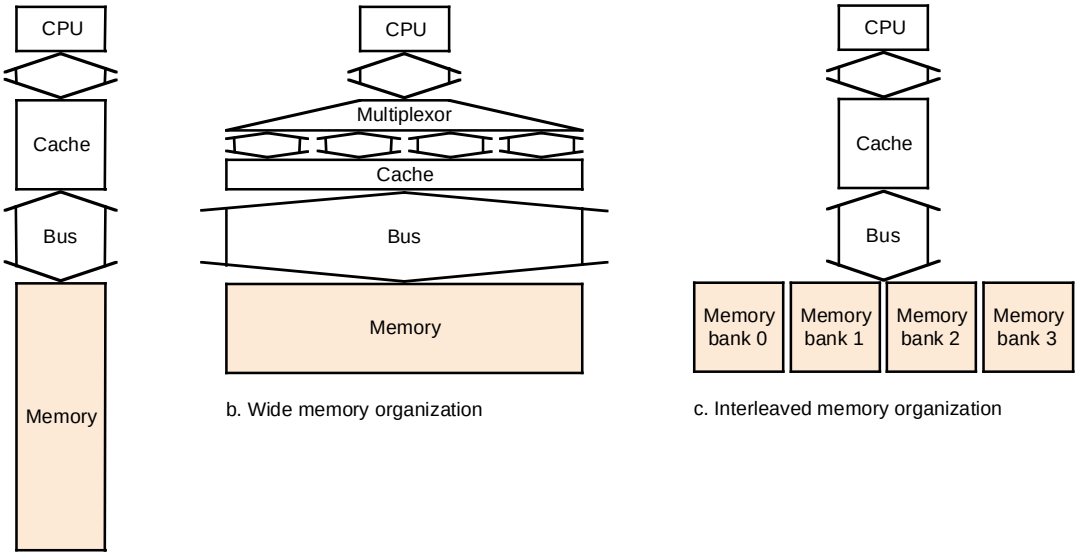
5. (1 point) _____ pipeline diagrams show the state of the entire datapath during a single clock cycle.

6. (1 point) A _____ is a delay in determining the proper instruction to fetch.

7. (1 point) _____ is the idea that if an item is referenced, items whose addressed are close by will tend to be referenced soon.

8. (1 point) If the data requested by the processor appears in some block in the cache, this is called a _____.

9. (15 points) Consider a memory hierarchy using one of the three organizations for main memory shown below. Assume that the cache block size is 8 words, that the width of organization b of the figure is four words, and that the number of banks in organization c is four. If the main memory latency for a new access is 40 cycles and the transfer time is 5 cycles, what are the miss penalties for organizations a and c?



a. One-word-wide memory organization

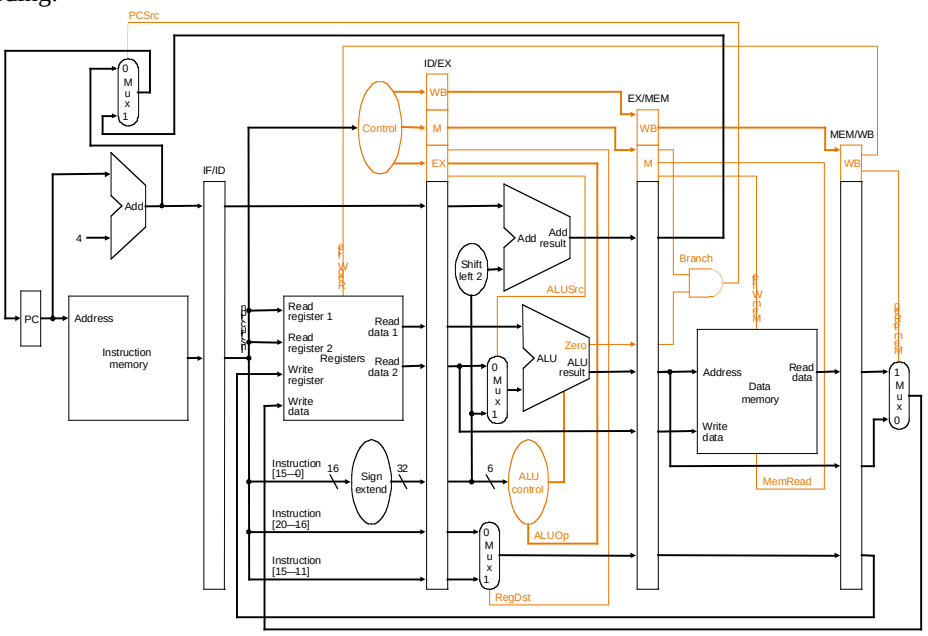
b. Wide memory organization

c. Interleaved memory organization

10. (10 points) (a) Identify all of the data dependencies in the following code. (b) How is each data dependency either handled or not handled by forwarding? If forwarding occurs, state the source of the data.

```
add   $2, $5, $4
lw    $5, 25($2)
add   $4, $2, $5
sw    $5, 100($2)
add   $3, $2, $4
```

11. (20 points) Consider executing the following code on a pipelined datapath like the one shown, except that it has forwarding:



```
sort:    addi$sp, $sp, -20
         sw  $ra, 16($sp)
         sw  $s3, 12($sp)
         sw  $s2, 8($sp)
         sw  $s1, 4($sp)
         sw  $s0, 0($sp)
         add $s2, $a0, $zero
         add $s3, $a1, $zero
         add $s0, $zero, $zero
for1tst: slt $t0, $s0, $s3
         beq $t0, $zero, exit1
         addi$s1, $s0, -1
for2tst: slt $t0, $s1, $zero
         bne $t0, $zero, exit2
         add $t1, $s1, $s1
         add $t1, $t1, $t1
         add $t2, $s2, $t1
         lw  $t3, 0($t2)
         lw    $t4, 4($t2)
         slt   $t0, $t4, $t3
         beq   $t0, $zero, exit2
         add   $a0, $s2, $zero
         add   $a1, $s1, $zero
         jal   swap
         addi  $s1, $s1, -1
         j     for2tst
exit2:   addi  $s0, $s0, 1
         j     for1tst
exit1:   lw    $s0, 0($sp)
         lw    $s1, 4($sp)
         lw    $s2, 8($sp)
         lw    $s3, 12($sp)
         lw    $ra, 16($sp)
         addi  $sp, $sp, 20
         jr    $ra
```

If the `add $s0` instruction one instruction before the `for1tst` label begins executing in cycle 1 and the `beq $t0, $zero, exit1` is taken, what are the values stored in the following fields of the EX/MEM pipeline register in the 10^{th} cycle? Assume that before the instructions are executed, the state of the machine was as follows:

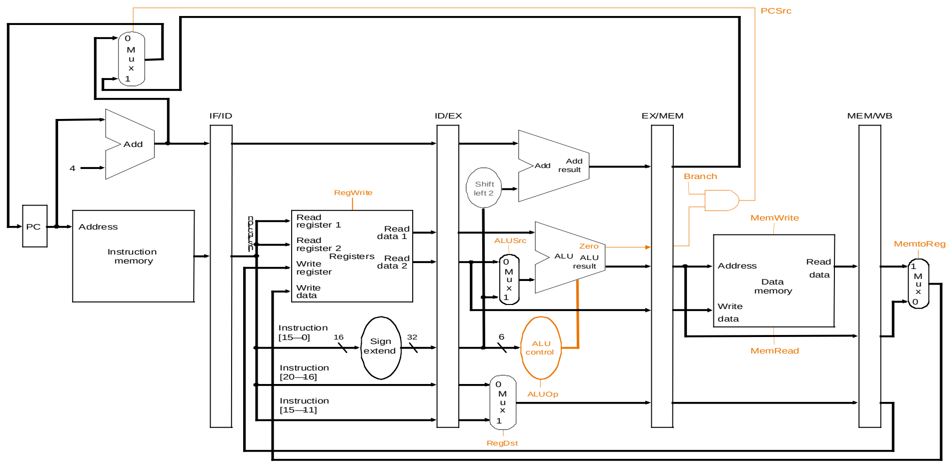
The PC has the value 500_{10}, the address of the `addi` instruction (with the label sort).

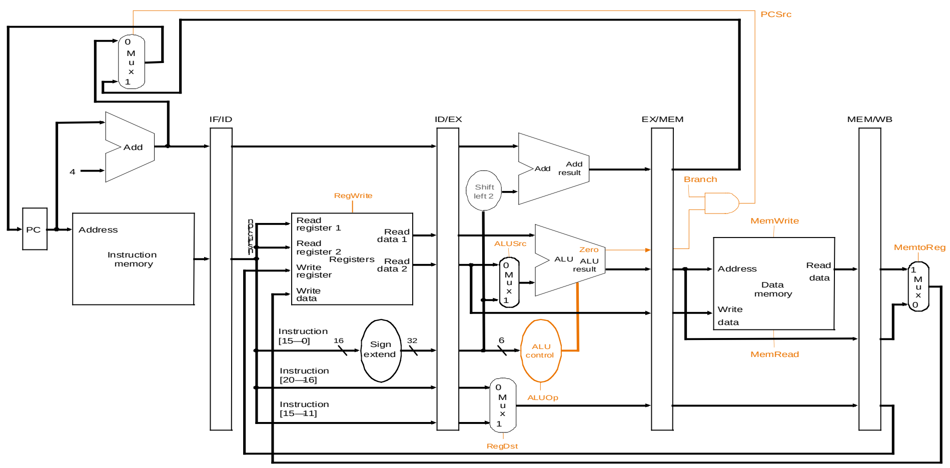
Every register has the initial value 10_{10} plus the register number.

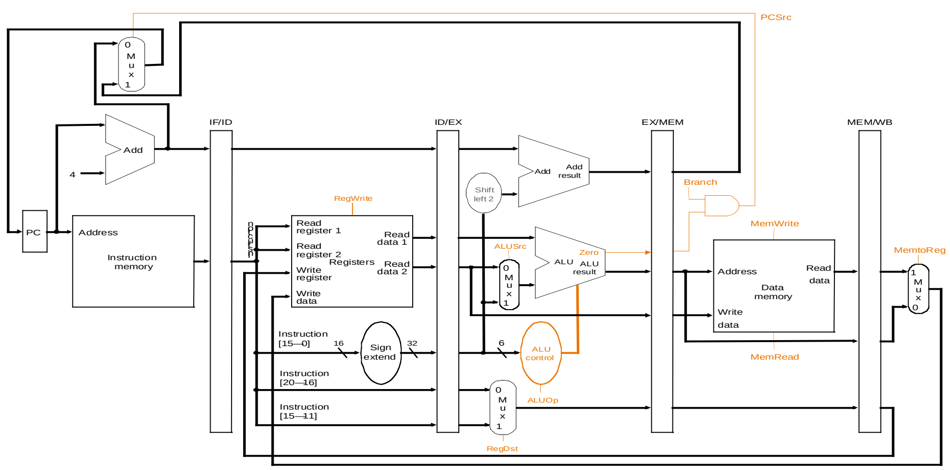
Every memory word accessed as data has the initial value 1000_{10} plus the byte address of the word.

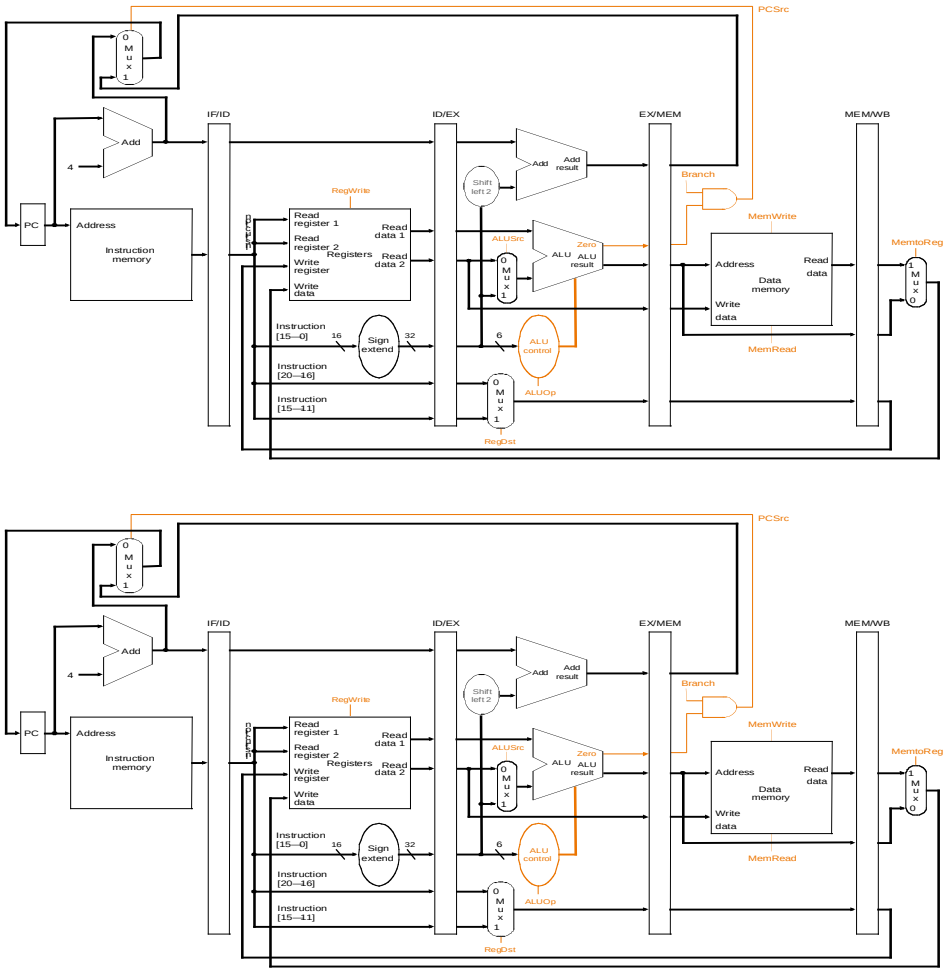
EX/MEM.WB =
EX/MEM.MEM =
EX/MEM.ALUResult =
EX/MEM.Readdata2 =
EX/MEM.WriteRd =

12. (10 points) Using the figures provided below, indicate which portions of the datapath are active (performing an operation used later by the instructionÕ execution) in each of the five stages of an `addi` instruction.









13. (10 points) Consider the pipeline of Chapter 6, shown in Problem 11, which has no forwarding and in which branches complete in the MEM stage. Rewrite the following code to minimize performance on this datapath — that is, reorder the instructions so that this sequence takes the most clock cycles to execute while still obtaining the same result.

```
lw    $3,0($5)
lw    $4,4($5)
add   $7, $7, $3
add   $8, $8, $4
add   $10, $7, $8
sw    $6, 0($5)
beq   $10, $11, Loop
```