Name: _____

1. (15 points) Consider the case of a four-deep pipeline where the branch is resolved at the end of the second stage for unconditional branches and at the end of the third cycle for conditional branches. The program run on this pipeline has the following branch frequencies (as percentages of all instructions) are as follows:

Conditional branches	20%
Jumps and calls	5%
Conditional branches	60% are taken

    Assuming that the CPI of the program, neglecting branch hazards, is 1.0, how much slower is the real number, when branch hazards are considered?

2. (15 points) You have been given 50 32K x 16-bit SRAMS to build an instruction cache for a processor with a 32-bit address. You do not have a byte offset. What is the largest size (i.e., the largest size of the data storage area in bytes) two-way set associative instruction cache that you can build with two-word blocks? Show the breakdown on the address into its cache access components and describe how the various SRAM chips will be used.

3. (1 point) A _____ means that the hardware cannot support the combination of instructions that we want to execute in the same clock cycle.

4. (1 point) The one case where forwarding cannot save the day is the case where a _____ instruction is followed by _____.

5. (1 point) A _____ computer can launch multiple instructions in a single cycle.

6. (1 point) _____ states that if an item is referenced, items whose addresses are close by will tend to be referenced soon.

7. (20 points) Consider executing the following code on a pipelined datapath like the one shown, except that it has forwarding:
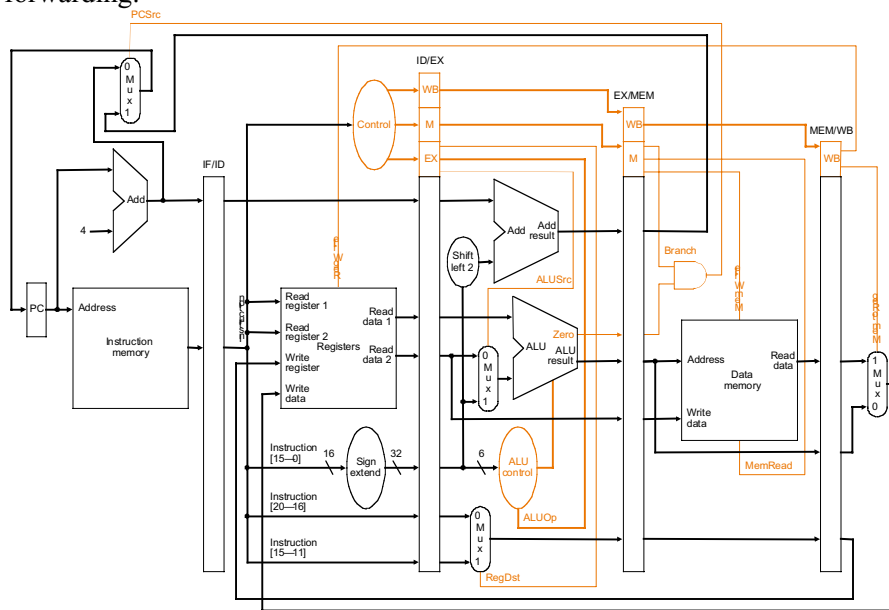

```
sort:       addi $sp, $sp, -20                          lw     $t4, 4($t2)
            sw   $ra, 16($sp)                           slt    $t0, $t4, $t3
            sw   $s3, 12($sp)                           beq    $t0, $zero, exit2
            sw   $s2, 8($sp)                            add    $a0, $s2, $zero
            sw   $s1, 4($sp)                            add    $a1, $s1, $zero
            sw   $s0, 0($sp)                            jal    swap
            add  $s2, $a0, $zero                        addi   $s1, $s1, -1
            add  $s3, $a1, $zero                        j      for2tst
            add  $s0, $zero, $zero           exit2:     addi   $s0, $s0, 1
for1tst:    slt  $t0, $s0, $s3                          j      for1tst
            beq  $t0, $zero, exit1          exit1:      lw     $s0, 0($sp)
            addi $s1, $s0, -1                           lw     $s1, 4($sp)
for2tst:    slt  $t0, $s1, $zero                        lw     $s2, 8($sp)
            bne  $t0, $zero, exit2                      lw     $s3, 12($sp)
            add  $t1, $s1, $s1                          lw     $ra, 16($sp)
            add  $t1, $t1, $t1                          addi   $sp, $sp, 20
            add  $t2, $s2, $t1                          jr     $ra
            lw   $t3, 0($t2)
```

If the `sw $s3` instruction two instructions after the `sort` label begins executing in cycle 1 and the `beq $t0, $zero, exit1` is taken, what are the values stored in the following fields of the ID/EX pipeline register in the 8th cycle? Assume that before the instructions are executed, the state of the machine was as follows:

The PC has the value 500_{10}, the address of the `addi` instruction (with the label sort).

Every register has the initial value 20_{10} plus the register number.

Every memory word accessed as data has the initial value 10000_{10} plus the byte address of the word.

Fill in all of the fields, even if the current instruction in that state is not using them.

ID/EX.WB =
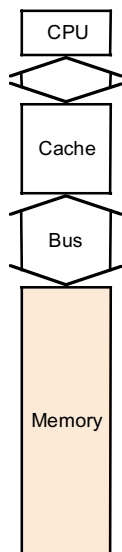ID/EX.MEM =
ID/EX.EX =
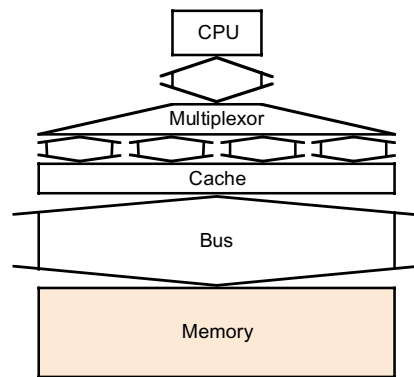ID/EX.PCInc =
ID/EX.Read1 =
ID/EX.Read2 =
ID/EX.SignEx =
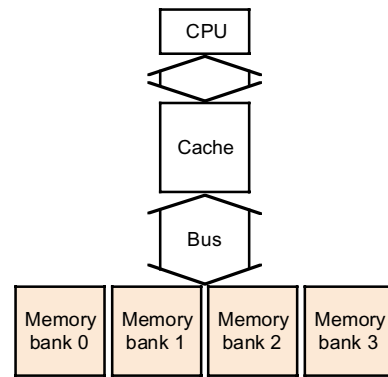ID/EX.Writert =
ID/EX.Writerd =

8. (5 points) For an m-stage pipeline, how many cycles does it take to execute n instructions if the pipeline is empty when these instructions begin to execute? _____

9. (1 point) In the case where memory and cache have different values for the same memory location, the cache and memory are said to be _____.

10. (15 points) Consider a memory hierarchy using one of the three organizations for main memory shown below. Assume that the cache block size is 16 words, that the width of organization b of the figure is eight words, and that the number of banks in organization c is four. If the main memory latency for a new access is 30 cycles and the transfer time is 3 cycles, what are the miss penalties for organizations a, b and c?

CPU

Cache

Bus

Memory

a. One-word-wide
   memory organization

CPU

Multiplexor

Cache

Bus

Memory

b. Wide memory organization

CPU

Cache

Bus

| Memory bank 0 | Memory bank 1 | Memory bank 2 | Memory bank 3 |

c. Interleaved memory organization

11. (15 points) (a) Identify all of the data dependencies in the following code. (b) How is each data dependency either handled or not handled by forwarding? Draw a multiple clock cycle style diagram to support your answer.

```
add    $2, $5, $4
lw     $4, 28($2)
add    $3, $2, $5
sw     $4, 100($2)
add    $3, $3, $4
```

12. (10 points) Here is a series of address references given as word addresses: 1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6. Assuming a direct-mapped cache with two-word blocks and a total size of 16 words that is initially empty, (a) label each reference in the list as a hit or a miss and (b) show the final contents of the cache.