The University of Alabama in Huntsville
Electrical & Computer Engineering Department
CPE 431 01
Final Exam
December 8, 2009

Name: _____

1. (1 point) GPUS were developed for the _____ industry.
2. (1 point) _____ law deals with the amount of speedup possible.
3. (1 point) Block is to cache as _____ is to virtual memory.
4. (1 point) MIPS uses the _____ save convention.
5. (1 point) _____(True or False) The computing industry has committed itself to multicores.

6. (10 points) The following table shows the instruction type breakdown of a given application executed.

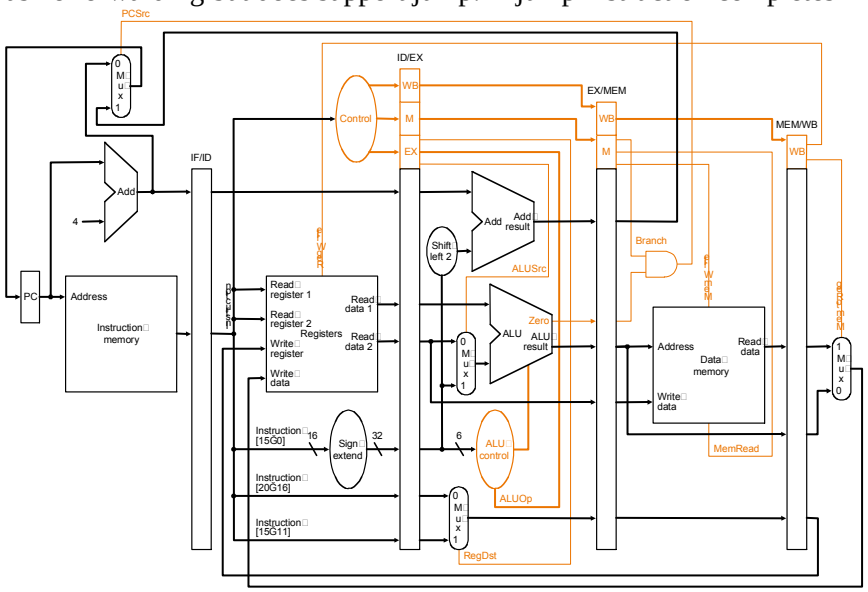
FP instructions	INT instructions	L/S instructions	Branch Instructions	CPI (FP)	CPI (INT)	CPI (L/S)	CPI (Branch)
560×10^6	2000×10^6	1280×10^6	256×10^6	1	1	4	2

Assume that the processor has a 2 GHz clock rate. By how much must we improve the CPI of FP instructions if we want the program to run two times faster?

7. (10 points) For the following C statement what is the corresponding MIPS assembly code? Assume that the variables `f`, g, h , i and j are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Further assume that the base addresses of the arrays A and B are in registers $s6 and $s7, respectively and that the declaration of the arrays is char A[20], B[20];

f = A[B[g] + 1];

8. (10 points) Consider executing the following code on a pipelined datapath like the one shown which has no forwarding but does support jump. A jump instruction completes in the ID stage.




```
sort:    addi$sp, $sp, -20
         sw  $ra, 16($sp)
         sw  $s3, 12($sp)
         sw  $s2, 8($sp)
         sw  $s1, 4($sp)
         sw  $s0, 0($sp)
         add $s2, $a0, $zero
         add $s3, $a1, $zero
         add $s0, $zero, $zero
for1tst: slt $t0, $s0, $s3
         beq $t0, $zero, exit1
         addi$s1, $s0, -1
for2tst: slt $t0, $s1, $zero
         bne $t0, $zero, exit2
         add $t1, $s1, $s1
         add $t1, $t1, $t1
         add $t2, $s2, $t1
         lw  $t3, 0($t2)
         lw    $t4, 4($t2)
         slt   $t0, $t4, $t3
         beq   $t0, $zero, exit2
         add   $a0, $s2, $zero
         add   $a1, $s1, $zero
         jal   swap
         addi  $s1, $s1, -1
         j     for2tst
exit2:   addi  $s0, $s0, 1
         j     for1tst
exit1:   lw    $s0, 0($sp)
         lw    $s1, 4($sp)
         lw    $s2, 8($sp)
         lw    $s3, 12($sp)
         lw    $ra, 16($sp)
         addi  $sp, $sp, 20
         jr    $ra
```

If the `addi $s1` instruction one instruction before the `for2tst` label begins executing in cycle 1 and the `bne $t0, $zero, exit2` is taken, what are the instructions in each stage of the

pipeline in the 14th cycle? If there is a bubble in any stage of the pipeline, also indicate which instruction was there before it became a bubble.

IF: _____

ID: _____

EX: _____

MEM: _____

WB _____

Cycle	IF	ID	EX	MEM	WB
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					

9. (10 points) Stall cycles due to mispredicted branches increase the CPI. Assume the breakdown of dynamic instructions into various categories and that the branch predictor accuracies are as follows:

R-type	beq	jmp	lw	sw
50 %	15 %	10 %	15 %	10%

Always-taken	Always not-taken	2-bit
50 %	15 %	10 %

Further assume that branch outcomes are determined in the EX stage, that there are no data hazards, and that no delay slots are used. What is the extra CPI due to mispredicted branches with the always-taken predictor?

10. (5 points) What is the minimum number of bits needed to represent -287 in 2's complement? What is that representation in hexadecimal?

11. (10 points) Here is a series of address references given as word addresses: 1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6. Assuming a two-way set associative cache with one word blocks and a total size of 8 words that is initially empty, (a) label each reference in the list as a hit or a miss and (b) show the entire history of the cache

12. (5 points) What MIPS instruction does the following collection of bits represent?
0x00020A82

13. (10 points) Assume you are configuring a Sun Fire x4150 server and assume that this configuration contains four processors. Determine whether configurations of 4, 8, and 16 disks present an I/O bottleneck.

Program Instructions Per I/O Operation	OS Instructions Per I/O Operation	Workload (KB reads)	Processor Speed (Instructions/Second)
500,000	100,000	32	1 Billion

The seek time for the disks is 2.9 ms. Consider sequential reads and writes. The disks rotate at 15,000 RPM and have a sustained transfer rate of 112 MB/s. Assume that the bandwidth of all other elements is sufficient to sustain the I/O rate of the processors and the disks.

14. (10 points) Consider the following portions of two different programs running at the same time on three processors in a symmetric multicore processor (SMP). Assume that before this code is run, w is 0, x is 3 and y and z are 1. w, x, y, and z are type `int`.

Core 1: `y = 5/z;`
Core 2: `w = x + y + 1;`
Core 3: `z = w*x + y;`

What are all the possible resulting values of w, x, y, and z? Show all possible interleavings of instructions and the resulting values of w, x, y, and z.

15. (5 points) Represent 0.0 in single precision floating-point format.

16. (10 points) There are several parameters that have an impact on the overall size of a page table. Listed below are several key page table parameters.

Virtual address size	Page size	Page table entry size
32 bits	4 KB	4 bytes

Calculate the total page table size for a system running five applications that utilize half of the memory available.