The University of Alabama in Huntsville
ECE Department
CPE 431 01
Test 1
October 1, 2013

Name: _____

1. (1 point) An _____ computer is one that is used for running one predetermined application or collection of software
2. (1 point) A _____ is the component of the processor that performs arithmetic operations.
3. (1 point) _____ is a natural element that is a semiconductor.
4. (1 point) The _____ is a data structure for spilling registers organized as a last-in-first-out queue.
5. (1 point) The _____ is the register that is reserved to point to the static area.
6. (10 points) In a von Neumann architecture, groups of bits have no intrinsic meanings by themselves. What a bit pattern represents depends entirely on how it is used. What decimal number does the bit pattern 0xF359 0AC9 represent if it is a floating point number? Use the IEEE 754 standard.

7. (15 points) Compilers can have a profound impact on the performance of an application on a given processor. For the same program, two different compilers are used. The table shows the execution time of the two different compiled programs. Find the average CPI for each program given that the processor has a clock cycle time of 1 ns.

Compiler A		**Compiler B**	
# Instructions	**Execution time**	**# Instructions**	**Execution Time**
1.00 E+09	1.3 s	1.50E+09	1.8 s

A new compiler is developed that uses only 600 million instructions and has an average CPI of 1.1. What is the speedup of using this new compiler versus using Compiler A or B on the original processor?

8. (10 points) If the current value of the PC is 0x0FFF FFFC, can you use a single jump instruction to get to the PC address 0x0FBE 4000?

9. (15 points) In this exercise, we examine how pipelining affects the clock cycle time of the processor. Problems in this exercise assume that individual stages of the datapath have the following latencies:

IF	ID	EX	MEM	WB
150 ps	220 ps	300 ps	280 ps	140 ps

(a) (8 points) What is the total latency of an LW instruction in a pipelined and non-pipelined processor?
(b) (7 points) If we can split one stage of the pipelined datapath into two new stages, each with half of the latency of the original stage, which stage would you split and what is the new latency for an LW instruction

10. (15 points) Find the shortest sequence of MIPS instructions that perform the same operation as `rpt $t2, loop`, where the meaning is

```
if (R[rs] > 0)
{
    R[rs] = R[rs] – 1
    PC = PC + 4 + BranchAddr
}
```

11. **(**15 points**)** Consider two different implementations, P1, and P2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. P1 has a clock rate of 4 GHz, and P2 has a clock rate of 6 GHz. The average number of cycles for each instruction class for P1 and P2 are listed in the following table.

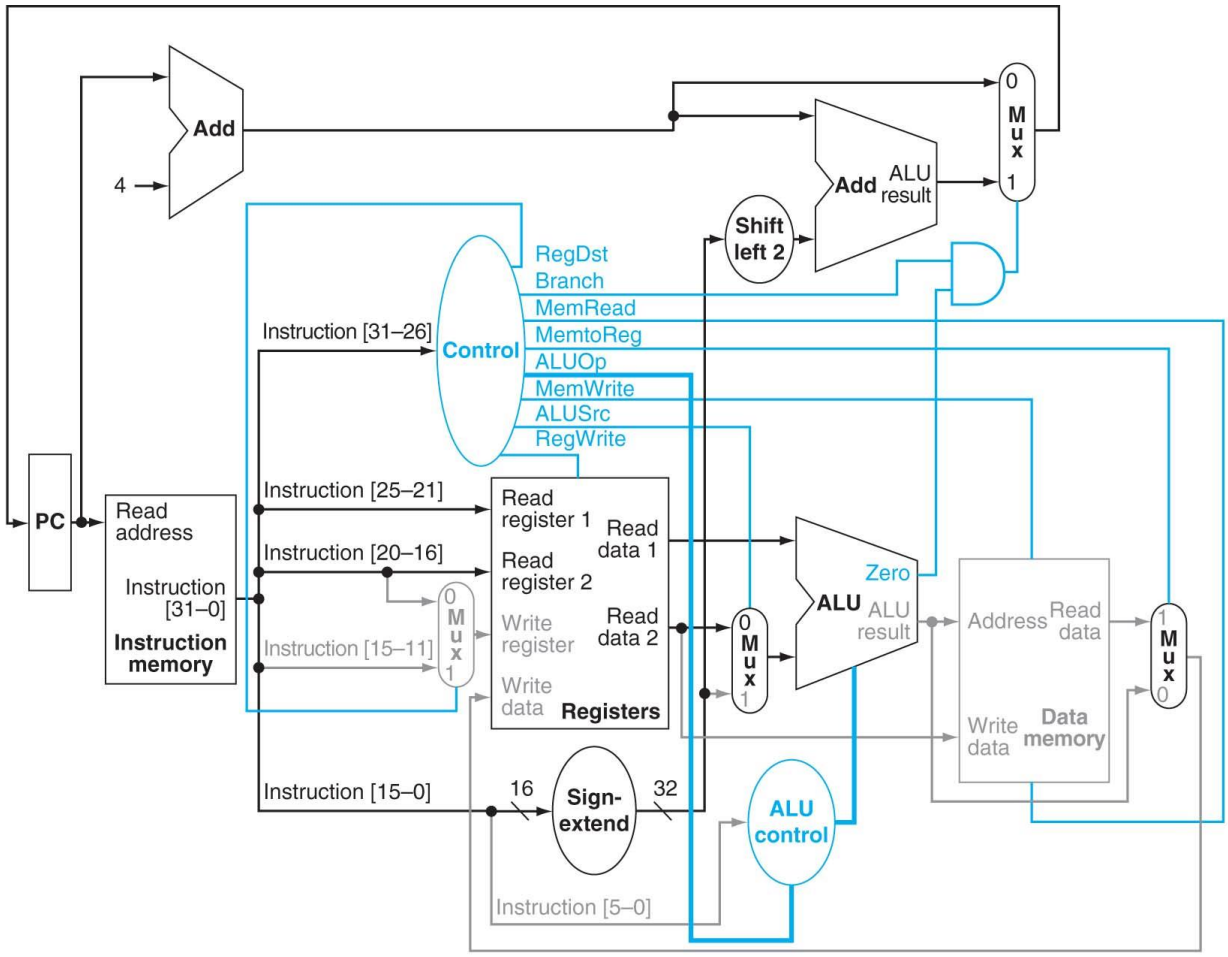
	CPI Class A	CPI Class B	CPI Class C
P1	1	2	3
P2	2	3	5

If the number of instructions executed in a certain program is divided among the three instruction classes so that the number of cycles for each class is the same on processor P1, how much faster is P2 than P1?

12. (15 points) Add a variant of the `lw` instruction which sums the contents of two registers to obtain the address of the data and which uses the R format to the single-cycle datapath shown in the figure below. Add any necessary datapaths and control signals and show the necessary additions to the table of control signals given.

```
lw   $9, $6, $22
$9 ← MEM[$6+$22]
```

36	6	22	9	0	32



Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALU Op1	ALU Op0	
R-format	1	0	0	1	0	0	0	1	0	
lw	0	1	1	1	1	0	0	0	0	
sw	d	1	d	0	0	1	0	0	0	
beq	d	0	d	0	0	0	1	0	1	

d – don't care