**The University of Alabama in Huntsville
ECE Department
CPE 431 01
Test 1
October 3, 2019**

Name: _____

You *must* show your work to receive full credit: You may use additional sheets of paper for your work, please put your name on each additional sheet.
Remember: ET = IC*CPI*CT

1. (1 point) Floating-point numbers are represented in _____ notation.

2. (1 point) More fraction bits give you more _____.

3. (1 point) _____ (True or False) The algorithm chosen can affect performance.

4. (2 points) A typical workload specifies both the _____ run and their

   _____.

5. (10 points) Write down the hexadecimal representation of the decimal number -52451.75 in the IEEE 754 double precision format.

6.   (10 points) Translate the following C code to MIPS. Assume that the variables f, g, h, i, and j
        are given and are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Assume
        that the base address of the arrays A and B are in registers $s6 and $s7, respectively. Assume
        that the elements of the arrays A and B are 4-byte words:

        B[i] = A[j] + 12

7.   (5 points) Assume the following register contents:
        ```
        $t0 = 0xAAAAAAAA
        $t1 = 0x12345678
        ```
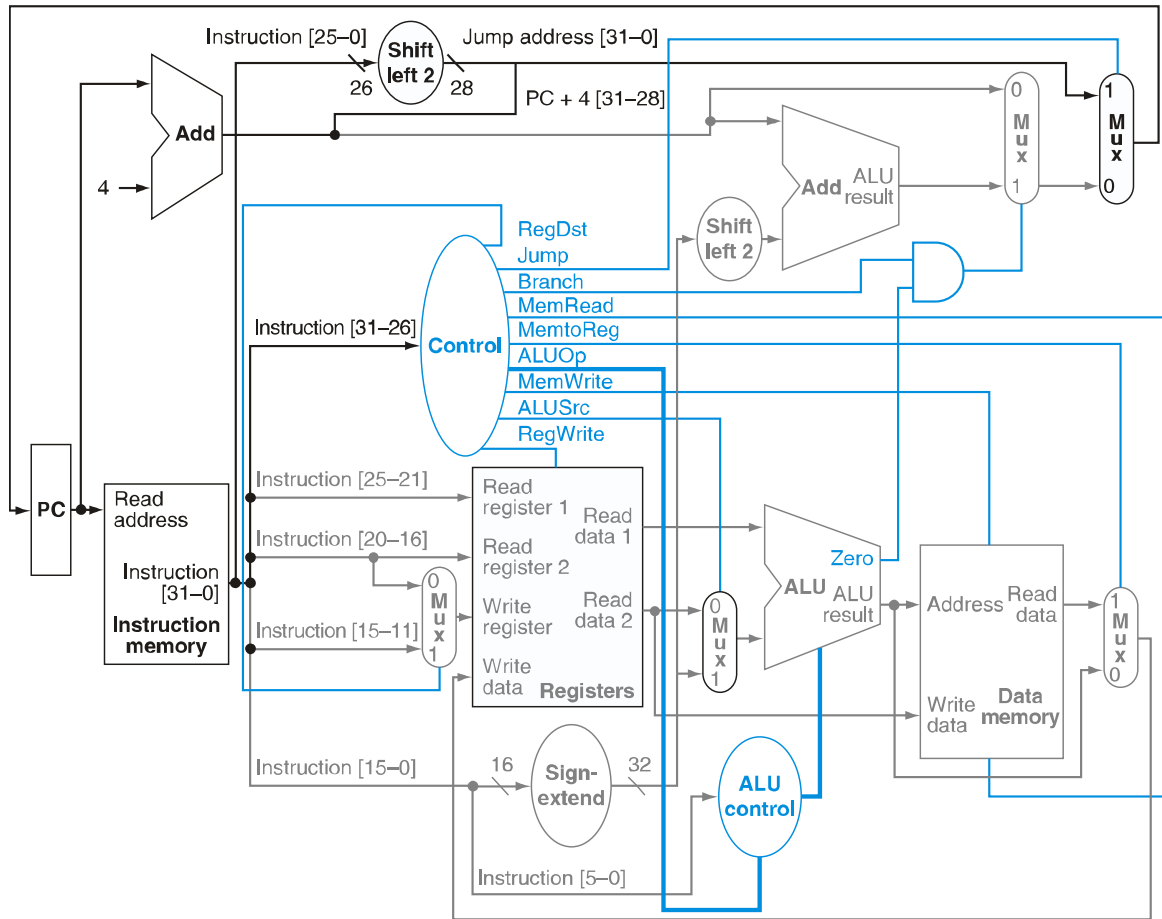   What is the value of $t2 for the following sequence of instructions?

        ```
        sll    $t2, $t0, 5
        andi   $t2, $t2, -1
        ```

8.   (15 points) Assume the following latencies for logic blocks in the datapath: Any components not listed have zero delay. What is the clock cycle for this datapath? Show all of your work.

| I-Mem	Add	ALU	Regs	D-Mem	SignExtend	Shift-Left-2
200 ps	120 ps	90 ps	105 ps	250 ps	30 ps	20 ps

9.   (5 points) If the current value of the PC is 0x0000 0000, can you use a single branch instruction to get to the PC address 0x0000 0EF2?

10.   (15) Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes of instructions according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.2 GHz and CPIs of 1, 2, 4, and 3, and P2 with a clock rate of 3 GHz and CPIS of 1, 2, 3, and 4.

      (a) (9 points) Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

      (b) (6 points) Find the clock cycles required in both cases.

11.	(15 points) Add the `lui` (load upper immediate) instruction which uses the I format to the single-cycle datapath shown in the figure below. Add any necessary datapaths and control signals and show the necessary additions to the table of control signals given. An example `lui` instruction, its RTL, and the instruction fields are shown below.

```
lui    $t1, 22
$t1 ← 22 * 2^16
```

$$\$t1 \leftarrow 22 * 2^{16}$$

| 15 | 0 | 9 | 22 |
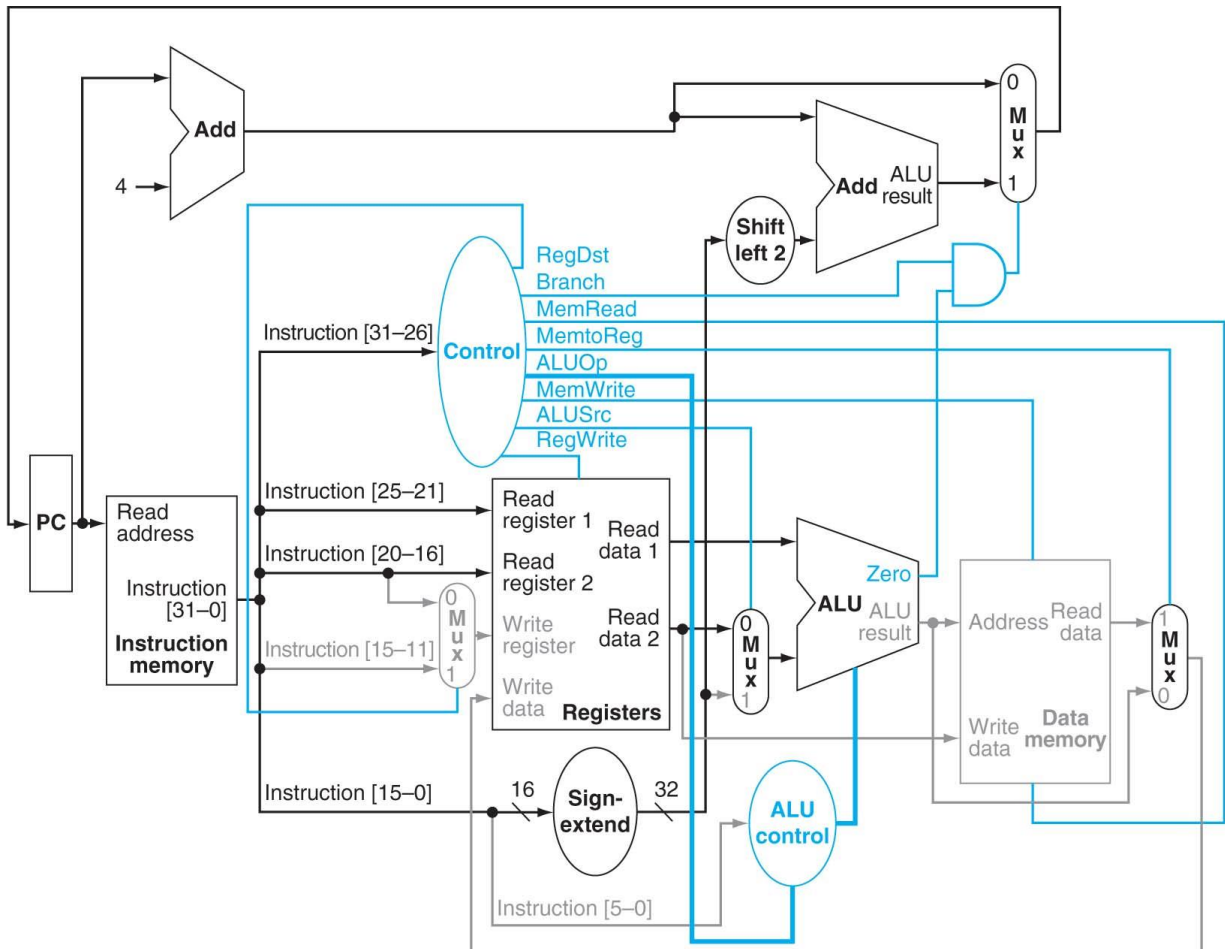
Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALU Op1	ALU Op0	
R-format	1	0	0	1	0	0	0	1	0	
Lw	0	1	1	1	1	0	0	0	0	
Sw	d	1	d	0	0	1	0	0	0	
Beq	d	0	d	0	0	0	1	0	1	

d – don't care

12.   (20 points) Assume there is no forwarding in a five stage MIPS pipelined processor. Neglect pipeline fill.

        (a) (10 points) Indicate hazards and add nop instructions to eliminate them.

```
or    $s0, $t2, $s1
lw    $s5, 0($s0)
and   $t1, $s5, $s0
sw    $t1, 0($s0)
```

        (b) (5 points) What is the total execution time of this instruction sequence with only ALU-ALU forwarding?
        (c) (5 points) What is the speedup over a no-forwarding pipeline?