

The University of Alabama in Huntsville
Electrical & Computer Engineering Department
CPE 431 01
Final Exam Solution
Fall 2010

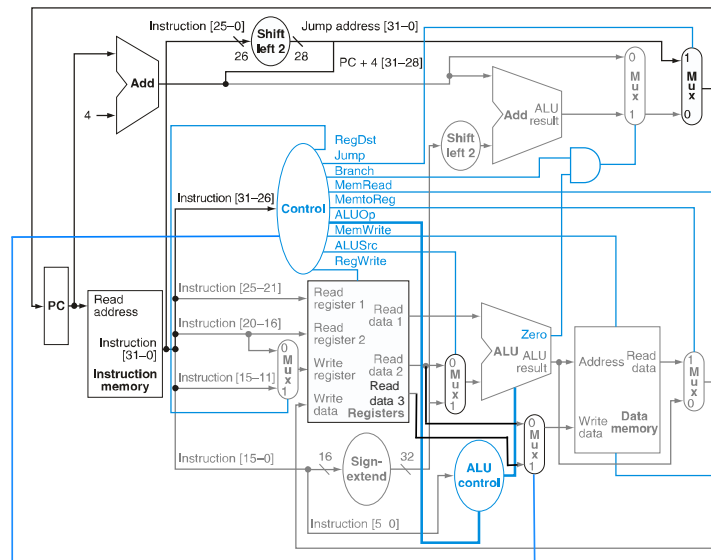
1. (1 point) A symmetric multiprocessor (SMP) is one that offers the programmer a single physical address space across all processors.
2. (1 point) As processors operating in parallel normally share data, they need to coordinate when operating on shared data, this coordination is called synchronization.
3. (1 point) Pipelining allows sharing of functional units of a single processor in an overlapping fashion.
4. (1 point) A virtual memory miss is called a page fault.
5. (1 point) True (True or False) Overhead for communication is one of the reasons that it is difficult to write fast parallel processing programs.
6. (10 points) Consider two different implementations of the same instruction set architecture. There are four classes of instructions, A, B, C, and D. The clock rate and CPI of each implementation are given in the following table. Given a program with 10^6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C and 20% class D, which implementation is faster?

	Clock rate	CPI Class A	CPI Class B	CPI Class C	CPI Class D
P1	1.5 GHz	1	2	3	4
P2	2 GHz	2	2	2	2

$$\begin{aligned}
 \frac{P_{P2}}{P_{P1}} &= \frac{ET_{P1}}{ET_{P2}} = \frac{\frac{IC_{P1} * CPI_{P1}}{CR_{P1}}}{\frac{IC_{P2} * CPI_{P2}}{CR_{P2}}} = \frac{IC * CPI_{P1} * CR_{P2}}{IC * CPI_{P2} * CR_{P1}} = \\
 &= \frac{(0.1 * 1 + 0.2 * 2 + 0.5 * 3 + 0.2 * 4) * 2 \times 10^9}{(0.1 * 2 + 0.2 * 2 + 0.5 * 2 + 0.2 * 2) * 1.5 \times 10^9} \\
 &= \frac{(0.1 + 0.4 + 1.5 + 0.8) * 2}{(0.2 + 0.4 + 1.0 + 0.4) * 1.5} = \frac{2.8 * 2}{2 * 1.5} \\
 &= \frac{5.6}{3} = 1.87
 \end{aligned}$$

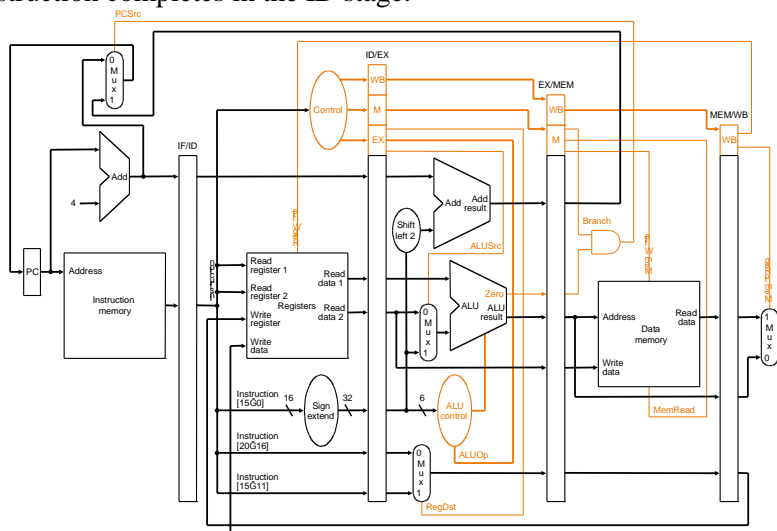
P2 is faster than P1 by a factor of 1.87

7. (10 points) Consider the following instruction: `swi Rd, Rs (Rt)` whose operation is defined by the following register transfer statement $\text{Mem}[\text{Rs} + \text{Rt}] = \text{Rd}$. What must be changed in the single cycle datapath to add this instruction to the MIPSA ISA?



The register file has to be modified so that there are three read ports. A MUX has to be added with an attendant control line.

8. (10 points) Consider executing the following code on a pipelined datapath like the one shown which (a) has no forwarding, (b) does support jump and (c) has branch completion in the ID stage. A jump instruction completes in the ID stage.



```
sort:    addi $sp, $sp, -20
         sw  $ra, 16($sp)
         sw  $s3, 12($sp)
         sw  $s2, 8($sp)
         sw  $s1, 4($sp)
         sw  $s0, 0($sp)
         add $s2, $a0, $zero
         add $s3, $a1, $zero
         add $s0, $zero, $zero
```

```
for1tst: slt $t0, $s0, $s3
         beq $t0, $zero, exit1
         addi $s1, $s0, -1
for2tst: slt $t0, $s1, $zero
         bne $t0, $zero, exit2
         add $t1, $s1, $s1
         add $t1, $t1, $t1
         add $t2, $s2, $t1
         lw  $t3, 0($t2)
```

```

        lw      $t4, 4($t2)
        slt     $t0, $t4, $t3
        beq     $t0, $zero, exit2
        add     $a0, $s2, $zero
        add     $a1, $s1, $zero
        jal     swap
        addi    $s1, $s1, -1
        j       for2tst
exit2:  addi    $s0, $s0, 1

        j       for1tst
exit1:  lw      $s0, 0($sp)
        lw      $s1, 4($sp)
        lw      $s2, 8($sp)
        lw      $s3, 12($sp)
        lw      $ra, 16($sp)
        addi    $sp, $sp, 20
        jr      $ra

```

If the `addi $s1` instruction one instruction before the `for2tst` label begins executing in cycle 1 and the `bne $t0, $zero, exit2` is taken, what are the instructions in each stage of the pipeline in the 14th cycle? If there is a bubble in any stage of the pipeline, also indicate which instruction was there before it became a bubble.

IF: _ `addi $s1` _
 ID: ___ `beq $t0` ___
 EX: ___ `slt $t0` ___
 MEM: ___ `bubble (lw $s0)` ___
 WB ___ `j for1tst` ___

Cycle	IF	ID	EX	MEM	WB
1	<code>addi \$s1</code>				
2	<code>slt \$t0</code>	<code>addi \$s1</code>			
3	<code>bne \$t0</code>	<code>slt \$t0</code>	<code>addi \$s1</code>		
4	<code>bne \$t0</code>	<code>slt \$t0</code>	bubble	<code>addi \$s1</code>	
5	<code>bne \$t0</code>	<code>slt \$t0</code>	bubble	bubble	<code>addi \$s1</code>
6	<code>add \$t1</code>	<code>bne \$t0</code>	<code>slt \$t0</code>	bubble	bubble
7	<code>add \$t1</code>	<code>bne \$t0</code>	bubble	<code>slt \$t0</code>	bubble
8	<code>add \$t1</code>	<code>bne \$t0</code>	bubble	bubble	<code>slt \$t0</code>
9	<code>addi \$s0</code>	bubble	<code>bne \$t0</code>	bubble	bubble
10	<code>j for1tst</code>	<code>addi \$s0</code>	bubble	<code>bne \$t0</code>	bubble
11	<code>lw \$s0</code>	<code>j for1tst</code>	<code>addi \$s0</code>	bubble	<code>bne \$t0</code>
12	<code>slt \$t0</code>	bubble	<code>j for1tst</code>	<code>addi \$s0</code>	bubble
13	<code>beq \$t0</code>	<code>slt \$t0</code>	bubble	<code>j for1tst</code>	<code>addi \$s0</code>
14	<code>addi \$s1</code>	<code>beq \$t0</code>	<code>slt \$t0</code>	bubble	<code>j for1tst</code>

9. (10 points) Assume that the variables `f`, `g`, `h`, `i`, and `j` are assigned to registers `$s0`, `$s1`, `$s2`, `$s3`, and `$s4`, respectively. Assume that the base address of the arrays `A` and `B` are in registers `$s6` and `$s7`, respectively. Additionally, `A` and `B` are arrays of integers. What is the corresponding MIPS assembly code for the following C statement?

$$f = g - A[B[4]]$$

```

lw      $t0, 16($s7)
sll     $t0, $t0, 2
add     $t0, $t0, $s6
lw      $t0, 0($t0)
sub     $s0, $s1, $t0

```

10. (5 points) What MIPS instruction does the following collection of bits represent?
 0x8D080040

```

1000 1101 0000 1000 0000 0000 0100 0000
Opcode = 10 0011 = lw
Rs = 01000 = $t0
Rt = 01000 = $t0
Offset = 0000 0000 0100 0000 = 64

lw    $t0, 64($t0)

```

11. (5 points) What is the minimum number of bits needed to represent -150 in 2's complement? What is that representation in hexadecimal?

With 8 bits, the numbers that can be represented are $-2^7 - +2^7 - 1$ or $-128 - +127$, can't represent -150. With 9 bits, the numbers that can be represented are $-2^8 - +2^8 - 1$ or $-256 - +255$, so 9 bits is enough and the minimum.

12. (10 points) Here is a series of address references given as word addresses: 1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6. Assuming a two-way set associative cache with two word blocks and a total size of 16 words that is initially empty, (a) label each reference in the list as a hit or a miss and (b) show the entire history of the cache

$$16\text{words} \times \frac{1\text{block}}{2\text{words}} \times \frac{1\text{set}}{2\text{blocks}} = 4\text{sets}, 1 \text{ bit of block offset, 2 bits of index}$$

	Index	Block	Offset					
1	0000	0	00	1	m	5	0000	0 10 1 h
4	0000	0	10	0	m	6	0000	0 11 0 m
8	0001	1	00	0	m			
5	0000	0	10	1	h			
20	0001	0	10	0	m			
17	0001	0	00	1	m			
19	0001	0	01	1	m			
56	0011	1	00	0	m			
9	0000	1	00	1	m			
11	0000	1	01	1	m			
4	0000	0	10	0	h			
43	0010	1	01	1	m			

Set	Element 0	Element 1
0	MEM[0:1], MEM[16:17], MEM[8:9]	MEM[8:9], MEM[56:57]
1	MEM[18:19], MEM[42:43]	MEM[10:11]
2	MEM[4:5]	MEM[20:21]
3	MEM[6:7]	

13. (10 points) Mean Time Between Failures (MTBF), Mean Time To Replacement (MTTR), and Mean Time To Failure (MTTF) are useful metrics for evaluating the reliability and availability of a storage resource. Explore these concepts by answering the questions about a device with the following metrics.

MTTF	MTTR
5 Years	10 days

- (a) Calculate the MTBF for the devices.
(b) Calculate the availability for this device.

$$\text{MTBF} = \text{MTTF} + \text{MTTR} = 5 \times 365 + 10 = 1835 \text{ days} = 44,040 \text{ hours}$$

$$\text{Availability} = \frac{\text{MTTF}}{\text{MTTF} + \text{MTTR}} = \frac{5\text{Years} \times \frac{365\text{Days}}{1\text{Year}}}{5\text{Years} \times \frac{365\text{Days}}{1\text{Year}} + 10\text{Days}} = \frac{1825}{1835} = 0.9986$$

14. (10 points) Consider the following portions of two different programs running at the same time on three processors in a symmetric multicore processor (SMP). Assume that before this code is run, w is 2, x is -2 and y and z are 1. w, x, y, and z are type `int`.

Core 1: `y = 5/z;`

Core 2: `w = x + y + 1;`

Core 3: `z = w*x + y;`

What are all the possible resulting values of w, x, y, and z? Show all possible interleavings of instructions and the resulting values of w, x, y, and z.

Possible Sequences	Resulting Values			
	w	x	y	z
	2	-2	1	1
1, 2, 3	4	-2	5	3
1, 3, 2	4	-2	5	1
2, 1, 3	0	-2	5	5
2, 3, 1	0	-2	5	1
3, 1, 2	-2	-2	-1	-3
3, 2, 1	0	-2	-1	-3

15. (5 points) Represent -16.0 in single precision floating-point format.

$$-16.0_{10} = 10000_2 = 1.0 \times 2^4$$

Sign = 1, negative number

$$\text{Exponent} = 4 + 127 = 131_{10} = 1000_0001_2$$

$$\text{Fraction} = 000\ 0000\ 0000\ 0000\ 0000\ 0000$$

Putting them together $1100\ 0000\ 1000\ 0000\ 0000\ 0000\ 0000\ 0000 = 0xC080\ 0000$

```

2    0    1
2    1    0
2    2    0
2    4    0
2    8    0
2   16

```

16. (10 points) The following code is written in MATLAB, where elements within the same column are stored contiguously. References to which variables exhibit spatial locality? I and J are both arrays of integers 8000 by 8000.

```

for J=1:8;
    for I=1:8000;
        A(I, J) = B(J, 1) + A(J, I);
    end
end

```

Variable	I	J	A(I,J)	B(J, 1)	A(J, I)
Spatial	Unknown	Unknown	Yes, elements are accessed by column	Yes, elements are accessed by column	No, elements are accessed by row
Temporal	Yes, used 64000 times to access array elements	Yes, used 64000 times to access array elements	No, a different element is accessed each time	Yes, used 8000 times, each	No, a different element is accessed each time