The University of Alabama in Huntsville
Electrical & Computer Engineering Department
CPE 431 01
Final Exam
December 2, 2016

Name: _____

1. (1 point) _____ is the most important performance metric.
2. (1 point) A _____ includes one or more threads, the address space and the operating system stack.
3. (1 point) _____ is the process of coordinating the behavior of two or more processes, which may be running on different processors.
4. (1 point) _____ involves communicating between multiple processor by explicitly sending and receiving information.
5. (1 point) MIPS in an example of a _____ architecture.
6. (8 points) What number does 0x36E9 A000 represent, assuming the IEE 754 single precision format?

7. (15 points) Here is a series of address references given as hexadecimal word addresses: 21, 4, 8, 5, 20, 37, 19, 5E, 209, 11, 4, 43, 5, 3E, 8, 16, 59, 187, 2E8, 30. Assuming a direct mapped cache with eight word blocks, a total size of 64 words that is initially empty, (a) label each reference in the list as a hit or a miss and (b) show the entire history of the cache, including tag and data.

Word Address (Hexadecimal)	Word Address (Decimal)	Binary	Miss/Hit
0x21	33	0000 0000 0010 0001	
0x4	4	0000 0000 0000 0100	
0x8	8	0000 0000 0000 1000	
0x5	5	0000 0000 0000 0101	
0x20	32	0000 0000 0010 0000	
0x37	55	0000 0000 0011 0111	
0x19	25	0000 0000 0001 1001	
0x5E	94	0000 0000 0101 1110	
0x209	521	0000 0010 0000 1001	
0x11	17	0000 0000 0001 0001	
0x4	4	0000 0000 0000 0100	
0x43	67	0000 0000 0100 0011	
0x5	5	0000 0000 0000 0101	
0x3E	62	0000 0000 0011 1110	
0x8	8	0000 0000 0000 1000	
0x16	22	0000 0000 0001 0110	
0x59	89	0000 0000 0101 1001	
0x187	391	0000 0001 1000 0111	
0x2E8	744	0000 0010 1110 1000	
0x30	48	0000 0000 0011 0000	

8. (10 points) Consider the following portions of three programs running at the same time on three processors in a symmetric multicore processor (SMP). Assume that before this code is run, w is 1, x is 3 and y is 2 and z is 4. w, x, y, and z are type `int`. What are all the possible outcomes of executing these instructions?

Core 1:
```
y = 5/z + w;
```
Core 2:
```
x = x + y/(w + 1);
```
Core 3:
```
z = w*(x – y) + z;
```

9. (5 points) Assume a program requires the execution of 50 x 10E6 FP operations, 110 x 10E6 INT instructions, 80 X 10E6 L/S instructions and 16 x 10E6 branch instructions. The CPI for each type of instruction is 1, 1, 4, and 2, respectively. Assume that the processor has a 2 GHz clock rate. By how much must we improve the CPI of FP instructions if we want the program to run two times faster?

10. (15 points) (a) Identify all of the data dependencies in the following code. (b) How is each data dependency either handled or not handled by forwarding? Draw a multiple clock cycle style diagram to support your answer.

```
a     add   $5, $5, $4
b     lw    $4, 28($2)
c     add   $2, $4, $5
d     sw    $2, 100($4)
e     add   $3, $2, $7
```

11. (10) points Consider an SMT processor that allows instructions from 2 threads to be run concurrently (i.e., there are two functional units), and instructions from either or both threads can be issued to run on any cycle. Assume we have two threads X and Y to run on these CPUs that include the following operations:

Thread X	Thread Y
A1 – takes 3 cycles to execute A2 – no dependences A3 – can't be executed at the same time as A1 A4 – depends on the result of A3 A5 – no dependences and takes two cycles to execute	B1 – take 2 cycles to execute B2 – can't be executed at the same time as B1 B3 – depends on the result of B2 B4 – no dependences and takes 2 cycles to execute B5 – depends on the results of B1 and takes 3 cycles to execute

Assume all operations take a single cycle to execute unless noted otherwise or they encounter a hazard. How many cycles will it take to execute these two threads? How many issue slots are wasted due to hazards?

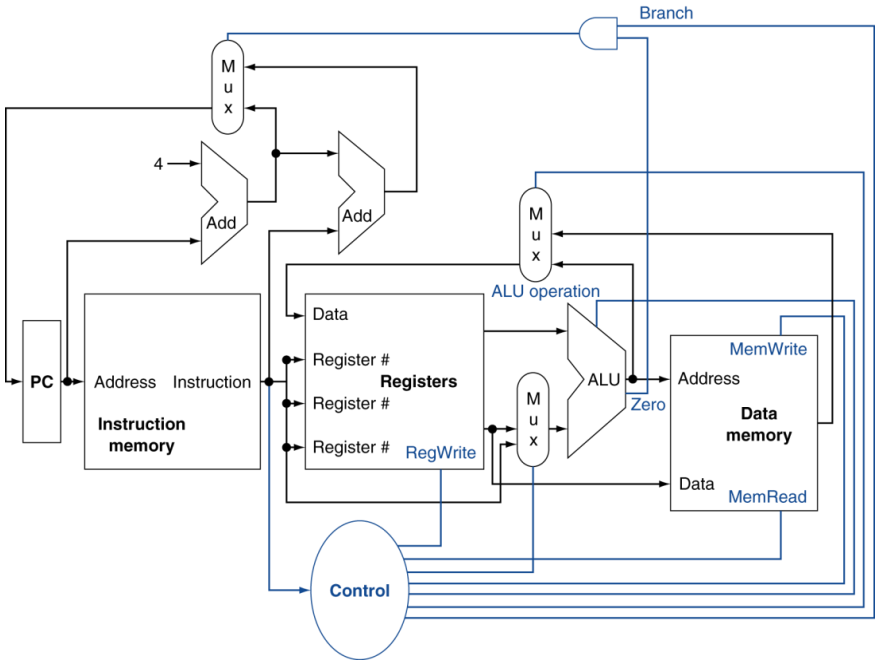
12. (10 points For the MIPS assembly instructions below, what is the corresponding C statement? Assume that the variables `f`, `g`, `h`, `i`, and `j` are assigned to registers `$s0`, `$s1`, `$s2`, `$s3`, and `$s4`, respectively. Assume that the base address of the arrays `A` and `B` are in registers `$s6 and $s7`, respectively.

```
sll   $t0, $s0, 2
add   $t0, $s6, $t0
sll   $t1, $s1, 2
add   $t1, $s7, $t1
lw    $t2, 0($t0)
addi  $t0, $t0, 4
lw    $t0, 0($t0)
add   $t0, $t0, $t2
sw    $t0, 0($t1)
```

13. (7 points) Given a virtual memory system with 48 bit virtual addresses, 16 KiB pages, and 8 byte page table entries. Calculate the total page table size for a system running 7 applications that utilize a third of the memory available.

14. (15 points)When processor designers consider a possible improvement to the processor datapath, the decision usually depends on the cost/performance trade-off. In the following three problems, assume that we are starting with the datapath shown, where I Mem, Add, Mux, ALU, Regs, D Mem, and Control blocks have latencies of 320 ps, 150 ps, 40 ps, 120 ps, 250 ps, 300 ps, and 80 ps, respectively, and costs of 1000, 30, 10, 100, 200, 2000, and 500, respectively.

Consider the addition of a multiplier to the ALU. This addition will add 300 ps to the latency of the ALU and will add a cost of 600 to the ALU. The result will be 5% fewer instructions executed since we will no longer need to emulate the MUL instruction.



What is the speedup achieved by adding this improvement?