The University of Alabama in Huntsville
Electrical & Computer Engineering Department
CPE 431 01
Final Exam
December 5, 2013

Name: ________________________________

1. (1 point) A ____________ is one of thousands of concentric circles that make up the surface of a magnetic disk.
2. (1 point) **A** ____________________________________ is a series of steps used to coordinate asynchronous bus transfers in which the sender and receiver proceed to the next step only when both parties agree that the current step has been completed.
3. (1 point) ________________ is the process of periodically checking the status of an I/O device to determine the need to service the device.
4. (1 point) ___________________ is the allocation of logically sequential blocks to separate disks to allow higher performance than a single disk can deliver.
5. (1 point) ______________________ is replacing a hardware component while the system is running.
6. (5 points) What is the value of the following 32 bits if they represent a single precision floating point number?

   0xC850 B300

7. (10 points) Here is a series of address references given as word addresses: 1, 4, 8, 5, 20, 17, 19, 56, 209, 11, 4, 43, 5, 36, 8, 16. Assuming a two-way set associative cache with two word blocks, a total size of 16 words that is initially empty, and an LRU replacement policy (a) label each reference in the list as a hit or a miss and (b) show the entire history of the cache

8. (8 points) Mean Time Between Failures (MTBF), Mean Time To Replacement (MTTR), and Mean Time To Failure (MTTF) are useful metrics for evaluating the reliability and availability of a storage resource. Explore these concepts by answering the questions about a device with the following metrics.

MTTF	MTTR
5 Years	20 days

(a) Calculate the MTBF for the devices.
(b) Calculate the availability for this device.

9. (10 points)) Consider the following portions of two different programs running at the same time on three processors in a symmetric multicore processor (SMP). Assume that before this code is run, w is 3, x is 5 and y and z are 1. w, x, y, and z are type `int`.

Core 1: `y = 5/(z + w);`
Core 2: `x = (x + y)/(w + 1);`
Core 3: `z = w*x - y;`

10. (8 points) A cache designer wants to increase the size of a 4 KB virtually indexed, physically tagged cache. Given a page size of 64 KB, is it possible to make a 16 KB direct-mapped cache, assuming 4 words per block? If not, how would the designer increase the size of the cache? If so, is 16 KB the largest direct-mapped cache size possible?

11. (5 points) Pseudoinstructions are not part of the MIPS instruction set but often appear in MIPS programs. For the pseudoinstruction in the following table, produce a minimal sequence of actual MIPS instructions to accomplish the same thing. You may need to use $at for some of the sequences. In the table, big refers to a specific number that requires 32 bits to represent and small to a number that can fit in 16 bits.

Pseudoinstruction	What it accomplishes
`beq $t2, big, L`	`if ($t2 = big) go to L`

12. (4 points) For the following MIPS instruction, show the value of the opcode (OP), source register (RS), and target register (RT) fields. For the I-type instructions, show the value of the immediate field, and for the R-type instructions, show the value of the destination register (RD) field.

```
srl  $t0, $s0, 6
```

13. (5 points) Consider the following loop. Assume that perfect branch prediction is used (no stalls due to control hazards), that there are no delay slots, and that the pipeline has full forwarding support. Also assume that many iterations of this loop are executed before the loop exits.

```
Loop:  add  $s1, $s2, $s1
       lw   $s2, 0($s1)
       lw   $s2, 16($s2)
       slt  $s1, $s2, $s4
       beq  $s1, $s7, Loop
```

At the start of the cycle in which we fetch the first instruction of the third iteration of the loop, what is stored in the IF/ID register?

14. (10 points) Consider two different implementations, P1, and P2, of the same instruction set. There are five classes of instructions (A, B, C, D, and E) in the instruction set. P1 has a clock rate of 4 GHz, and P2 has a clock rate of 6 GHz. The average number of cycles for each instruction class for P1 and P2 are listed in the following table.

	CPI Class A	CPI Class B	CPI Class C	CPI Class D	CPI Class D
P1	1	2	3	4	5
P2	3	3	3	5	5

If the number of instructions executed in a certain program is divided equally among the five classes of instructions except for class A, which occurs twice as often as each of the others, how much faster is P2 than P1?

15. (20 points) a) (5 points) Consider the following loop executing on a MIPS pipeline with MEM/WB forwarding only. Calculate the number of cycles it takes to execute this loop, neglecting pipeline fill cycles. b) (12 points) Unroll the loop so that 2 iterations of the loop are executed at once and schedule the unrolled code for a single issue MIPS pipeline. c) (3 points) Calculate the speedup from the original loop to the unrolled loop.

```
for (i=0; i < n; i++)
  A[i] = B[i] + C[i];

      addi  $s0, $t1, 200
Loop: add   $t5, $t2, $t1
      add   $t6, $t3, $t1
      add   $t7, $t4, $t1
      lw    $t5, 0($t5)
      lw    $t6, 0($t6)
      add   $t5, $t5, $t6
      sw    $t5, 0($t7)
      addi  $t1, $t1, 4
      bne   $t1, $s0, Loop
```