**The University of Alabama in Huntsville**
**Electrical & Computer Engineering Department**
**CPE 431 01**
**Test 1 Solution**
**Fall 2010**

1. (1 point) State one of the design principles: _ Simplicity favors regularity or Make the common case fast or Good design demands good compromises or Smaller is faster _.
2. (1 point) A form of representation of an instruction composed of fields of binary numbers is an _ instruction format _
3. (1 point) The program that instigates a procedure and provides the necessary parameter values is the _ caller _ .
4. (1 point) The register that is reserved to point to the static area is called the _ global pointer _.
5. (1 point) A systems program that places an object program in main memory so that it is ready to execute is a _ loader _.
6. (9 points) At the point where this function is called, registers `$a0`, `$a1`, `$a2`, and `$a3` have values 1, 100, 1000, and 30, respectively. What is the value returned by this function?

```
F:    sub   $s0, $a0, $a3        // $s0 ← 1 – 30 = -29
      sll   $v0, $s0, 0x1        // $v0 ← -29 << 1 = -58
      add   $v0, $a2, $v0        // $v0 ← 1000 + (-58) = 942
      sub   $v0, $v0, $a1        // $v0 ← 942 – 100 = 842
      jr    $ra
```

842 is in $v0 at the end of this routine and is the return value.

7. (6 points) What are the binary representations of the opcode, rs, rt, rd, shamt, and funct fields in this instruction?

```
slt $t0, $s1, $a0
```

opcode (R-type) = $0_{10} = 000000_2$, rs ($s1) = $17 = 10001_2$, rt ($a0) = $4 = 00100_2$,
rd ($t0) = $8 = 01000_2$, shamt = $0 = 00000_2$,
funct (slt) = $2A_{16} = 42_{10} = 101010_2$

8. (5 points) Show the IEEE 754 binary representation for the floating-point number $253.125_{10}$ in single precision.

$253.125_{10} = 1111\ 1101.001_2 = 1.1111101001_2 \times 2^7$
Exponent = 7 + Bias = 7 + 127 = $134_{10} = 10000110_2$
Sign = 0, since number is positive

$0100\ 0011\ 0111\ 1101\ 0010\ 0000\ 0000\ 0000_2$ = 0x437D2000

9. (15 points) One user has told you that three programs constitute the bulk of his workload, but he does not run them equally. The user wants to determine how these three computers compare when the workload consists of different mixes of these three programs.

Suppose the total execution time is divided among the three programs so that the number of FLOPS (Floating-point operations) is equally divided between the three programs. Find which computer is fastest for this workload and by what factor.

| Program | FLOPS | Computer A | Computer B | Computer C | Weight |
|---|---|---|---|---|---|
| 1 | $5 \times 10^9$ | 2 s | 5 s | 10 s | 8 |
| 2 | $20 \times 10^9$ | 20 s | 20 s | 20 s | 2 |
| 3 | $40 \times 10^9$ | 200 s | 50 s | 15 s | 1 |

$w_1 = 8$ because program 1 has $5 \times 10^9$ FLOPs, and must be run eight times to have as many FLOPS as program 3, $w_2 = 2$ because program 2 has $20 \times 10^9$ FLOPs, and must be run two times to have as many FLOPS as program 3, $w_3 = 1$ because program 3 has $40 \times 10^9$ FLOPs, the least common multiple of the number of FLOPS in the three programs.

$ET = w_1 * ET_{P1} + w_2 * ET_{P2} + w_3 * ET_{P3}$
$ET_A = 8*2\text{ s} + 2*20\text{ s} + 1*200\text{ s} = (16 + 40 + 200)\text{s} = 256\text{ s}$
$ET_B = 8*5\text{ s} + 2*20\text{ s} + 1*50\text{ s} = (40 + 40 + 50)\text{s} = 130\text{ s}$
$ET_C = 8*10\text{ s} + 2*20\text{ s} + 1*15\text{ s} = (80 + 40 + 15)\text{s} = 135\text{ s}$

$\frac{P_B}{P_C} = \frac{ET_C}{ET_B} = \frac{135s}{130s} = 1.04$, Computer B is 1.04 times faster than Computer C

$\frac{P_B}{P_A} = \frac{ET_A}{ET_B} = \frac{256s}{130s} = 1.97$, Computer B is 1.97 times faster than Computer A

10. (10 points) The following problem deals with translating from C to MIPS. Assume that the variables `f`, `g`, `h`, `i`, and `j` are assigned to registers `$s0`, `$s1`, `$s2`, `$s3`, and `$s4`, respectively. Assume that the base address of the arrays `A` and `B` are in registers `$s6` and `$s7`, respectively.

f = g – A[B[4]]

```
lw    $t0, 16($s7)
sll   $t0, $t0, 0x2
add   $t0, $t0, $s6
lw    $t0, 0($t0)
sub   $s0, $s1, $t0
```

11. (10 points) What decimal number does the bit pattern represent if it is a two's-complement integer? An unsigned integer?

1010 1110 0011 0101

Two's Complement Signed

$1 \times -2^{15} + 1 \times 2^{13} + 1 \times 2^{11} + 1 \times 2^{10} + 1 \times 2^{9} + 1 \times 2^{5} + 1 \times 2^{4} + 1 \times 2^{2} + 1 \times 2^{0} = -20939$

Unsigned

$1 \times 2^{15} + 1 \times 2^{13} + 1 \times 2^{11} + 1 \times 2^{10} + 1 \times 2^{9} + 1 \times 2^{5} + 1 \times 2^{4} + 1 \times 2^{2} + 1 \times 2^{0} = 44597$

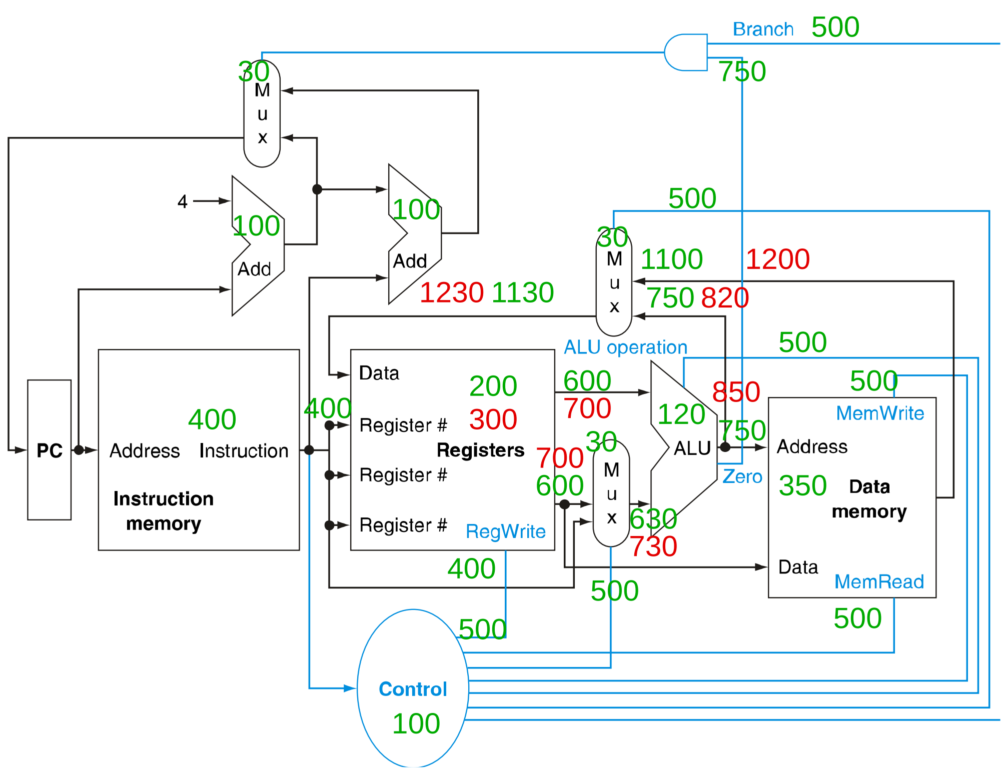
12. (20 points) When processor designers consider a possible improvement to the processor datapath, the decision usually depends on the cost/performance tradeoff. Consider the datapath shown, with the latencies and costs given in the table. One possible improvement is to make the registers larger, this modification will add 100 ps to the latency for Regs, add 200 to the cost of Regs and result in 5% fewer instructions because fewer loads and stores are needed to save and restore register values.

| | I-Mem | Add | Mux | ALU | Regs | D-Mem | Control |
|---|---|---|---|---|---|---|---|
| Latency | 400 ps | 100 ps | 30 ps | 120 ps | 200 ps | 350 ps | 100 ps |
| Cost | 1000 | 30 | 10 | 100 | 200 | 2000 | 500 |

a. (10 points) What is the clock cycle time with and without this improvement?
b. (10 points) Compare the cost/performance ratio with and without this improvement?

a. Cycle time without this improvement: 1330 ps
Cycle time with this improvement: 1530 ps
b. Cost without this improvement: 1000 + 2*30 + 3*10 + 100 + 200 + 2000 + 500 = 3890
Cost with this improvement: 1000 + 2*30 + 3*10 + 100 + 400 + 2000 + 500 = 4090

CPR = Cost/Performance = Cost*Execution Time
$CPR_{without}$ = 3890 * IC * 1330 ps
$CPR_{with}$ = 4090 * 0.95IC * 1530 ps
$CPR_{with}/CPR_{without}$ = (4090 * 0.95IC * 1530)/(3890 * IC * 1330) = 1.15
The "improvement" gives a higher cost/performance ratio, not really an improvement.



13. (10 points) Consider two different implementations, P1 and P2 of the same instruction set. There are five classes of instructions (A, B, C, D, E) in the instruction set. P1 has a clock rate of 4 GHz. P2 has a clock rate of 6 GHz. The average number of cycles for each instruction class for P1 and P2 is as follows:

| Class | CPI on P1 | CPI on P2 |
|---|---|---|
| A | 1 | 2 |
| B | 2 | 2 |
| C | 3 | 2 |
| D | 4 | 4 |
| E | 3 | 4 |

Assume that peak performance is defines as the fastest rate that a computer can execute any instruction sequence. What are the peak performances of P1 and P2 expressed in instructions per second?

For P1, peak performance is obtained using a sequence of instructions coming only from class A.

$$P_{P1} = \frac{4\times 10^{9}\, cycles/s}{1 cycle/instruction} = 4\times 10^{9}\, instructions/s$$

For P2, peak performance is obtained using a sequence of instructions coming only from classes 1, B, and C.

$$P_{P2} = \frac{6\times 10^{9}\, cycles/s}{2 cycles/instruction} = 3\times 10^{9}\, instructions/s$$

14. (10 points) The following table shows the instruction type breakdown of a given application.

| Floating-point Instructions | Integer Instructions | Load/Store Instructions | Branch Instructions | CPI (FP) | CPI (INT) | CPI (L/S) | CPI (Branch) |
|---|---|---|---|---|---|---|---|
| $560 \times 10^6$ | $2000 \times 10^6$ | $1280 \times 10^6$ | $2560 \times 10^6$ | 1 | 1 | 4 | 2 |

Assume that the processor has a 2 GHz clock rate. What must the CPI of the L/S instructions be if we want the program to run two times faster if that is the only improvement made?

$$\frac{P_{new}}{P_{old}} = 2 = \frac{ET_{old}}{ET_{new}} = \frac{(560*1+2000*1+1280*4+2560*2)\times 10^{6}}{(560*1+2000*1+1280*x+2560*2)\times 10^{6}}$$

$$2 = \frac{12800}{7680+1280*x}$$

15360 + 2560*x = 12800
2560*x = -2560
x = -1

There is no value of CPI for L/S that will create an increase in performance of 2.