The University of Alabama in Huntsville
Electrical & Computer Engineering Department
CPE 431 01
Test 2
November 2, 2010

Name: _____

Show all work. You will not receive full credit for a problem if you do not show your work!

1. (1 point) _____ is preventing fault occurrence by construction.
2. (1 point) Each disk surface of a magnetic disk is divided into concentric circles, called _____.
3. (1 point) The underlying technology in flash memories is _____
4. (1 point) The process of periodically checking status bits to see whether it is time for the next I/O operation is called _____.
5. (1 point) RAID 1 uses _____ to always provide two copies of all data..
6. (15 points) Virtual memory uses a page table to track the mapping of virtual addresses to physical addresses. Consider this stream of virtual addresses as seen on a system: 20717, 29637, 8849, 36965, 4493, 28674, 20517, 9179, 25632, 21111. Assume 4KB pages, a four-entry fully associative TLB, and true LRU replacement. If pages must be brought in from disk, increment the next largest page number. Given the address stream and shown initial state of the TLB and page table, show the final state of the system. Also list for each reference if it is a hit in the TLB, a hit in the page table, or a page fault.

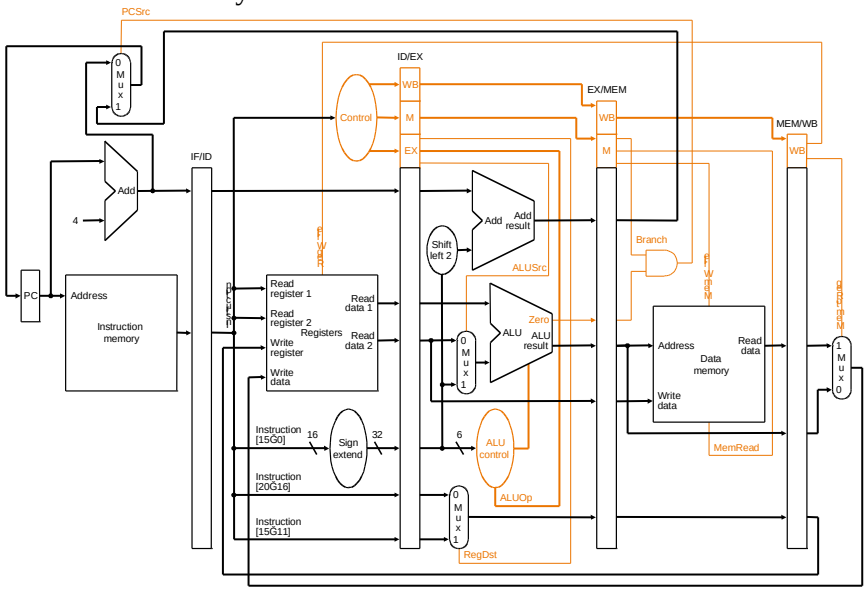
TLB

Valid	Tag	Physical Page Number
1	11	12
1	7	4
1	3	6
0	4	9

Page table

Valid	Physical page or in disk
1	5
0	Disk
0	Disk
1	6
1	9
1	11
0	Disk
1	4
0	Disk
0	Disk
1	3
1	12

7. (20 points) Consider executing the following code on a pipelined datapath like the one shown except that 1)it supports j instructions that complete in the ID stage, 2) it has forwarding from the EX/MEM pipeline register but no forwarding from the MEM/WB pipeline register, 3)it has branch completion in the ID stage. The register file does support writing in the first half cycle and reading in the second half cycle.




```
sort:    addi  $sp, $sp, -20
         sw    $ra, 16($sp)
         sw    $s3, 12($sp)
         sw    $s2, 8($sp)
         sw    $s1, 4($sp)
         sw    $s0, 0($sp)
         add   $s2, $a0, $zero
         add   $s3, $a1, $zero
         add   $s0, $zero, $zero
for1tst: slt   $t0, $s0, $s3
         beq   $t0, $zero, exit1
         addi  $s1, $s0, -1
for2tst: slt   $t0, $s1, $zero
         bne   $t0, $zero, exit2
         add   $t1, $s1, $s1
         add   $t1, $t1, $t1
         add   $t2, $s2, $t1
         ⇒lw   $t3, 0($t2)
         lw    $t4, 4($t2)
         slt   $t0, $t4, $t3
         beq   $t0, $zero, exit2
         add   $a0, $s2, $zero
         add   $a1, $s1, $zero
         jal   swap
         addi  $s1, $s1, -1
         j     for2tst
exit2:   addi  $s0, $s0, 1
         j     for1tst
exit1:   lw    $s0, 0($sp)
         lw    $s1, 4($sp)
         lw    $s2, 8($sp)
         lw    $s3, 12($sp)
         lw    $ra, 16($sp)
         addi  $sp, $sp, 20
         jr    $ra
```

If the `lw $t3` instruction five instructions after the `for2tst` label begins executing in cycle 1 and the `beq $t0, $zero, exit2` is taken, what are the values stored in the following fields of the EX/MEM pipeline register in the 10th cycle? Show the instructions being executed in each stage of the pipeline during each cycle. Assume that before the instructions are executed, the state of the machine was as follows:

The PC has the value 200_{10}, the address of the `lw $t4` instruction

Every register has the initial value 20_{10} plus the register number.

Every memory word accessed as data has the initial value 10000_{10} plus the byte address of the word.

Fill in all of the fields, even if the current instruction in that stage is not using them.

EX/MEM.WB =
EX/MEM.MEM =
EX/MEM.EX =
EX/MEM.TargetAddress =
EX/MEM.Zero =
EX/MEM.ALUOut
EX/MEM.ReadData2
EX/MEM.Write

Cycle	IF	ID	EX	MEM	WB
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					

8. (10 points) Consider the case of a six-deep pipeline where the branch is resolved at the end of the fourth stage for unconditional branches and at the end of the fifth cycle for conditional branches. The program run on this pipeline has the following branch frequencies (as percentages of all instructions) are as follows:

Conditional branches	30%
Jumps and calls	10%
Conditional branches	60% are taken

Assuming that the CPI of the program, neglecting branch hazards, is 1.0, how much slower is the real number, when branch hazards are considered?

9. (15 points) Here is a series of address references given as word addresses: 0, 4, 16, 132, 232, 160, 1024, 30, 140, 3100, 180, 2180. Assuming a direct-mapped cache with four-word blocks and a total size of 32 words that is initially empty and uses LRU, (a) label each reference in the list as a hit or a miss and (b) show the entire history of the cache.

10. (10 points) Average and minimum times for reading and writing to storage devices are common measurements used to compare devices. Using techniques from Chapter 6, calculate values related to read and write time for a disk with the following characteristics.

Average Seek Time	RPM	Disk Transfer Rate	Controller Setup Time	Controller Transfer Rate
14 ms	7200	34 Mbytes/s	2 ms	480 Mbits/s

Calculate the average time to read or write a 4096-byte sector for the disk listed.

11. (10 points) The following code is written in MATLAB, where elements within the same column are stored contiguously. References to which variables exhibit spatial locality? `A` and `B` are both arrays of integers 8000 by 8000.

```
for J=1:8;
   for I=1:8000;
      A(I,J) = B(J,1) + A(J, I);
```

12. (15 points) (a) Identify all of the data dependencies in the following code. (b) How is each data dependency either handled or not handled by forwarding? **Draw a multiple clock cycle style diagram to support your answer.**

```
add   $5, $5, $4
lw    $5, 28($5)
add   $3, $4, $5
sw    $3, 100($5)
add   $7, $3, $4
```