The University of Alabama in Huntsville
Electrical & Computer Engineering Department
CPE 431 01
Test 2
November 23, 2004

Name: _____

1. (5 points) Given the pipelined processor of Chapter 6 with forwarding, determine which instruction is being executed in each stage of the pipeline in cycle 8 of the following instruction sequence if it begins executing in cycle 1

```
1.    addi  $23, $29, 12
2.    sw    $2, 0($29)
3.    sw    $15, 4($29)
4.    sw    $16, 8($29)
5.    muli  $8, $5, 4
6.    add   $7, $4, $2
7.    lw    $15, 0($2)
8.    lw    $16, 4($2)
9.    sw    $17, 0($2)
10.   sw    $18, 4($2)
11.   lw    $2, 0($29)
12.   lw    $15, 4($29)
13.   lw    $16, 8($29)
14.   addi  $29, $29, 12
```

IF _____ ID _____ EX _____ MEM _____ WB _____

2. (15 points) You have been given 50 16K x 16-bit SRAMS to build an instruction cache for a processor with a 32-bit address. You do not have a byte offset. What is the largest size (i.e., the largest size of the data storage area in bytes) direct-mapped instruction cache that you can build with eight-word blocks? Show the breakdown on the address into its cache access components and describe how the various SRAM chips will be used.

3. (10 points) Consider a pipeline for a register-memory architecture. The architecture has two instruction formats: a register-register format and a register-memory format. There is a single memory addressing mode (offset + base register). There is a set of ALU operations as follows:

    ALUop← Rdest,Rsrc1,Rsrc2,offset
    Rdest ← Rsrc1 ALUop Rsrc2
or Rdest ← Rsrc1 ALUop MEM[Rsrc2 + offset]
or
    Rdest ← MEM[Rsrc2 + offset]
or
    MEM[Rsrc2 + offset] ← Rsrc1

where the ALUop is one of the following:

    Add, Subtract, And, Or(with or without offset)
    Load(Rsrc1 omitted)
    Store(Rdest omitted)

Rdest, Rsrc1 and Rsrc2 are registers.

Branches use a full compare of two registers and are PC-relative. Assume that this machine is pipelined so that a new instruction is started every clock cycle. The pipeline structure is

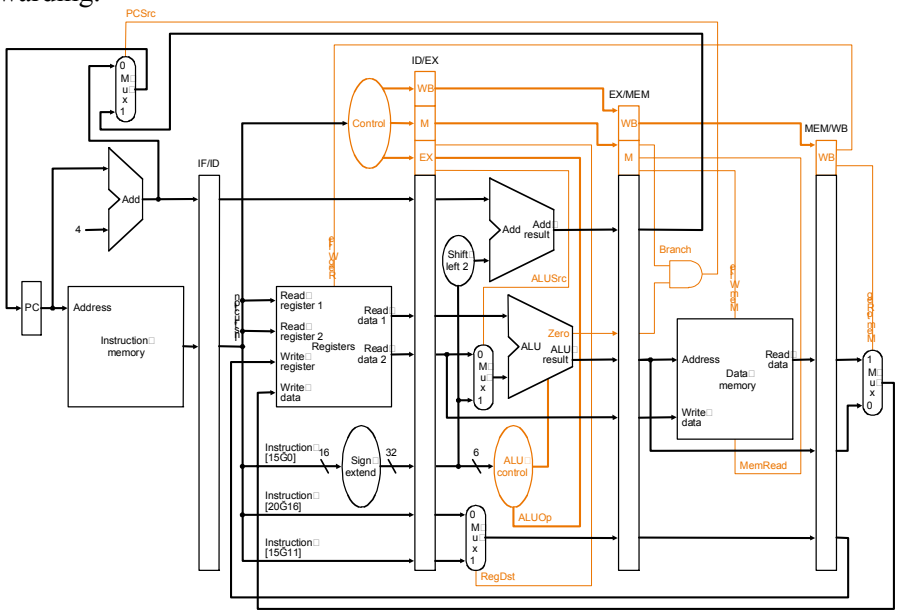
IF	RF	ALU1	MEM	ALU2	WB					
	IF	RF	ALU1	MEM	ALU2	WB				
		IF	RF	ALU1	MEM	ALU2	WB			
			IF	RF	ALU1	MEM	ALU2	WB		
				IF	RF	ALU1	MEM	ALU2	WB	
					IF	RF	ALU1	MEM	ALU2	WB

The first ALU stage is used for effective address calculation for memory references and branches. The second ALU stage is used for operations and branch comparisons. RF is both a decode and register-fetch stage. Assume that when a register read and a register write of the same register occur in the same clock cycle, the write data is forwarded. For the following code fragment:

```
add   $1, $1, 0($15)
add   $1, $1, 4($15)
add   $2 ,$2, 0($1)
add   $2, $2, 4($1)
store $2, 8($1)
```

identify the data dependencies and draw a figure (using the multiple clock style) showing them as lines.

4. (1 point) Assuming a branch is not taken is a crude form of _____.
5. (1 point) MIPS exceptions are collected in the _____ register.
6. (1 point) The _____ is the time to replace a block in the upper level with the corresponding block from the lower level in a hierarchical cache memory system.
7. (1 point) The _____ contain the address information required to identify whether a word in the cache corresponds to the requested word.
8. (1 point) Getting a missing data item early from the internal resources of the pipeline is called _____.
9. (20 points) Consider executing the following code on a pipelined datapath like the one shown which has no forwarding.




```
sort:    addi$sp, $sp, -20
         sw  $ra, 16($sp)
         sw  $s3, 12($sp)
         sw  $s2, 8($sp)
         sw  $s1, 4($sp)
         sw  $s0, 0($sp)
         add $s2, $a0, $zero
         add $s3, $a1, $zero
         add $s0, $zero, $zero
for1tst: slt $t0, $s0, $s3
         beq $t0, $zero, exit1
         addi$s1, $s0, -1
for2tst: slt $t0, $s1, $zero
         bne $t0, $zero, exit2
         add $t1, $s1, $s1
         add $t1, $t1, $t1
         add $t2, $s2, $t1
         lw  $t3, 0($t2)
         lw    $t4, 4($t2)
         slt   $t0, $t4, $t3
         beq   $t0, $zero, exit2
         add   $a0, $s2, $zero
         add   $a1, $s1, $zero
         jal   swap
         addi  $s1, $s1, -1
         j     for2tst
exit2:   addi  $s0, $s0, 1
         j     for1tst
exit1:   lw    $s0, 0($sp)
         lw    $s1, 4($sp)
         lw    $s2, 8($sp)
         lw    $s3, 12($sp)
         lw    $ra, 16($sp)
         addi  $sp, $sp, 20
         jr    $ra
```

If the `add $s0` instruction seven instructions after the `sort` label begins executing in cycle 1 and the `beq $t0, $zero, exit1` is taken, what are the values stored in the following fields of the EX/MEM pipeline register in the 14th cycle? Assume that before the instructions are executed, the state of the machine was as follows:

The PC has the value 200_{10}, the address of the `add $s0` instruction

Every register has the initial value 20_{10} plus the register number.

Every memory word accessed as data has the initial value 10000_{10} plus the byte address of the word.

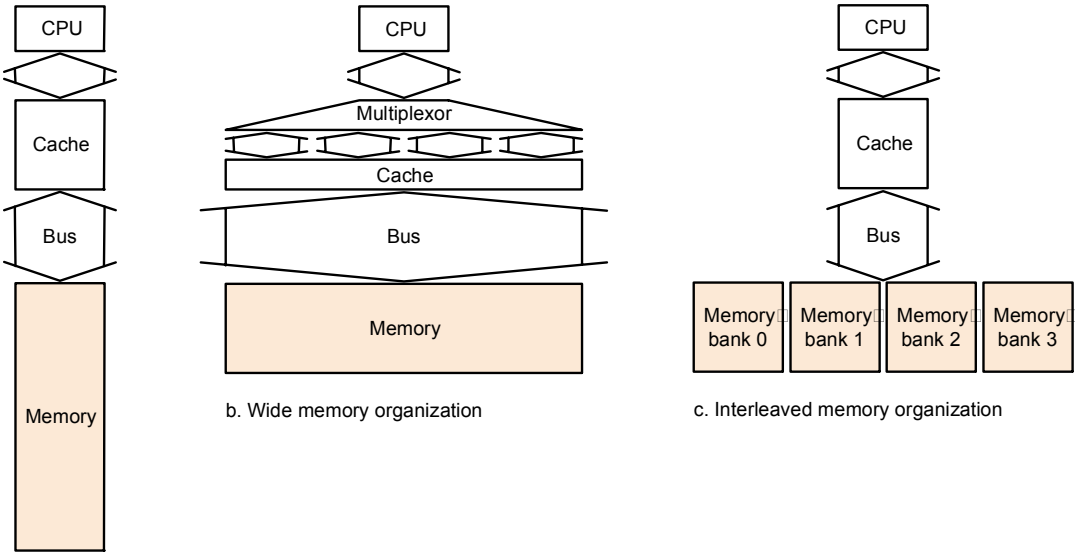
Fill in all of the fields, even if the current instruction in that state is not using them.

EX/MEM.WB =
EX/MEM.MEM =
EX/MEM.Target =
EX/MEM.Zero =
EX/MEM.ALUOut =
EX/MEM.Readdata2 =
EX/MEM.Writerd =

Cycle	IF	ID	EX	MEM	WB
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					

10. (5 points) For an m-stage pipeline, how many cycles does it take to execute n instructions if the pipeline is empty when these instructions begin to execute? _____

11. (15 points) Consider a memory hierarchy using one of the three organizations for main memory shown below. Assume that the cache block size is 32 words, that the width of organization b of the figure is four words, and that the number of banks in organization c is eight. If the main memory latency for a new access is 50 cycles and the transfer time is 3 cycles, what are the miss penalties for organizations a, b and c?



a. One-word-wide memory organization

b. Wide memory organization

c. Interleaved memory organization

12. (15 points) (a) Identify all of the data dependencies in the following code. (b) How is each data dependency either handled or not handled by forwarding? Draw a multiple clock cycle style diagram to support your answer.

```
add   $5, $5, $4
lw    $4, 28($2)
add   $2, $4, $5
sw    $4, 100($2)
add   $3, $2, $4
```

13. (10 points) Here is a series of address references given as word addresses: 1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6. Assuming a direct-mapped cache with four-word blocks and a total size of 64 words that is initially empty, (a) label each reference in the list as a hit or a miss and (b) show the final contents of the cache.