The University of Alabama in Huntsville
Electrical & Computer Engineering Department
CPE 431 01
Test 1
September 27, 2007

Name: _____

1. (1 point) List one of the design principles given in the book _____
   _____

2. (1 point) The fastest growing segment of the processor market is _____

3. (1 point) _____ is a model that renders low-level details of computer systems temporarily invisible to facilitate design of sophisticated systems.

4. (1 point) A _____ is a link to the calling site that allows a procedure to return to the proper address; in MIPS it is stored in register $ra.

5. (1 point) An _____ is a functional program in the format of an object file that contains no unresolved references, relocation information, symbol table, or debugging information.

6. (10 points) MIPS chooses to simplify the structure of its instructions. The way we implement complex instructions is to decompose such complex instructions into multiple simpler MIPS ones. The complex instruction `swap $rs, $rt` can be decomposed into three instructions. If the implementation of the `swap` instruction in hardware will increase the clock period of a single-cycle implementation by 10%, what percentage of `swap` operations in the instruction mix would recommend implementing it in hardware?

7. (10 points) When designing memory systems, it becomes useful to know the frequency of memory reads versus writes as well as the frequency of accesses for instructions versus data. Using the average instruction mix information for MIPS for the program SPEC2000int in the table below, find the following:

a. The percentage of all memory accesses (both data and instruction) that are for data.

b. The percentage of all memory accesses (both data and instruction) that are for reads. Assume that two-thirds of data transfers are loads.

8. (15 points) We with to compare the performance of two different computers: M1 and M2. The following measurements have been made on these computers:

Program	Time on M1	Time on M2
1	2.0 seconds	1.5 seconds
2	5.0 seconds	10.0 seconds

A user has the following requirements for the two computers: P1 must be executed 1600 times each hour. Any remaining time is used to run P2. If the computer has enough performance to execute program 1 the required number of times per hour, then performance is measured by the throughput for program 2? Which computer is faster for this workload and by how much?

9. (10 points) Show the IEEE 754 binary representation for the floating-point number 579.25_{ten} in single and double precision.

10. (15 points) Consider two different implementations, P1 and P2, of the same instruction set. There are six classes of instructions (A, B, C, D, E, and F) in the instruction set. P1 has a clock rate of 4 GHz and P2 has a clock rate of 6 GHz. The average number of cycles for each instruction class for P1 and P2 is as follows:

Class	CPI on P1	CPI on P2
A	1	2
B	2	3
C	3	2
D	4	5
E	3	4
F	2	1

If the number of instructions executed in a certain program is divided equally among the classes of instructions except for class D, which occurs twice as often as each of the others, how much faster is P2 than P1?

11. (20 points) Given the bit pattern:

$$0000\ 0000\ 1001\ 0100\ 0011\ 0000\ 0001\ 1011_2$$

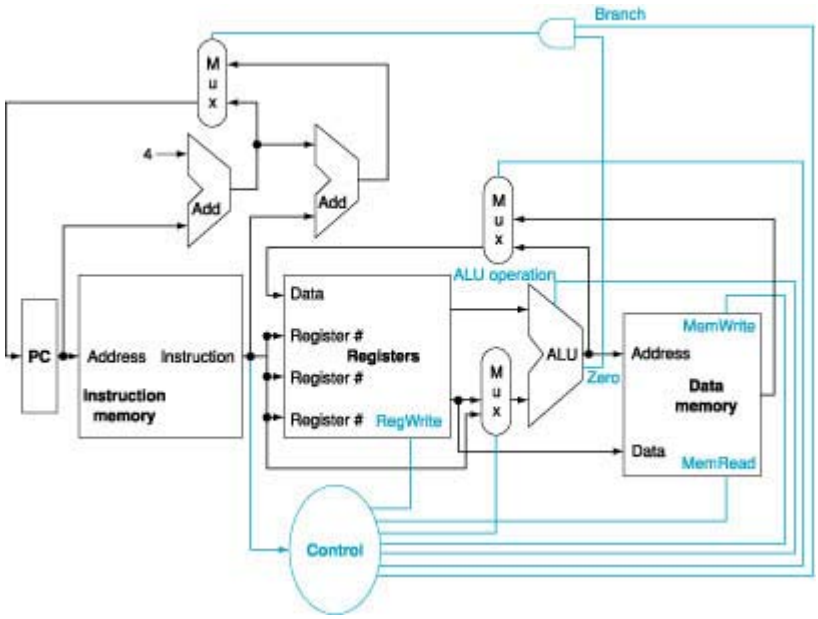
what does it represent, assuming that it is

a. a two's complement integer?
b. an unsigned integer?
c. a single precision floating-point number?
d. a MIPS instruction?

12. (15 points) We wish to add a variant of the `lw` (load word) instruction, which increments the index register after loading word from memory. This instruction (`l_inc`) corresponds to the following two instructions:

```
lw    $rs, L($rt)
addi  $rt, $rt, 1
```

Explain whether it is possible to implement `l_inc` without making any changes to the register file of the single-cycle datapath. If it is not possible, describe the changes that must be made to the register file.



Extra Credit

13. (1 point) An _____ is a word constructed by taking the initial letters of a string of words.

14. (1 point) A _____ is a sequence of instructions without branches and without branch targets or branch labels.