**The University of Alabama in Huntsville**
**Electrical & Computer Engineering Department**
**CPE 431 01**
**Final Exam**
**December 10, 2002**

Name: _____

Posting Code#1: _____

Posting Code#2: _____

1. (3 points) The three C s of caches are  _____, _____ and
_____.

2. (1 point) One addressing mode supported by the MIPS processor is _____.

3. (5 points) Given the bit pattern:

`0000 0000 0000 1000 0101 0011 1100 0000`$_2$

what does it represent, assuming that it is a MIPS instruction?

4. (5 points) Given the pipelined processor of Chapter 6 with forwarding, determine which instruction is being executed in each stage of the pipeline in cycle 11 of the following instruction sequence if it begins executing in cycle 1.

```
1.    addi $23, $29, 12          8.    lw   $16, 4($2)
2.    sw   $2, 0($29)            9.    sw   $17, 0($2)
3.    sw   $15, 4($29)          10.    sw   $18, 4($2)
4.    sw   $16, 8($29)          11.    lw   $2, 0($29)
5.    muli $8, $5, 4            12.    lw   $15, 4($29)
6.    add  $7, $4, $2           13.    lw   $16, 8($29)
7.    lw   $15, 0($2)           14.    addi $29, $29, 12
```

IF _____ ID _____ EX _____ MEM _____ WB _____

5. (15 points) A program repeatedly performs a three-step process: It reads in a 8-KB block of data from disk, does some processing on that data, and then writes out the result as another 8-KB block elsewhere on the disk. Each block is contiguous and randomly located on a single track on the disk. The disk drive rotates at 9600 RPM, has an average seek time of 8 ms, and has a transfer rate of 32 MB/sec. The controller overhead is 2 ms. No other program is using the disk or processor, and there is no overlapping of disk operation with processing. The processing step takes 20 million clock cycles, and the clock rate is 500 MHz. What is the overall speed of the system in blocks processed per second?

6. (1 point) _____ is the hardest problem.

7. (10 points) Consider a virtual memory system with the following properties:
- •40-bit virtual byte address
- •16-KB pages
- •36-bit physical byte address

What is the total size of the page table for each process on this machine, assuming that the valid, protection, dirty, and use bits take a total of 4 bits and that all the virtual pages are in use? (Assume that disk addresses are not stored in the page table.)

8. (10 points)    Suppose we are considering a change to an instruction set. The base machine initially has only loads and stores to memory, and all operations work on the registers. Such machines are called load-store machines (like the MIPS). Measurements of the load-store machine showing the instruction mix and clock cycle counts per instruction are given in the table below:

| Instruction Type | Frequency | Clock cycle count |
|---|---|---|
| ALU ops | 43 % | 1 |
| Loads | 21% | 2 |
| Stores | 12% | 2 |
| Branches | 24% | 2 |

Let s assume that 25% of the arithmetic logic unit (ALU) operations directly use a loaded operand that is not used again.

We propose adding ALU instructions that have one source operand in memory. These new register-memory instructions have a clock cycle count of 2. Suppose that the extended instruction set increases the clock cycle count for branches by 1, but it does not affect the clock cycle time. Would this change improve CPU performance?

9. (15 points) Consider the following idea: Let s modify the instruction set architecture and remove the ability to specify an offset for memory access instructions. Specifically, all load-store instructions with nonzero offsets would become pseudoinstructions and would be implemented using two instructions. For example:

```
addi  $at, $t1, 104    # add the offset to a temporary
lw    $t0, $at         # new way of doing lw $t0, 104 ($t1)
```

(a) (5 points) What changes would you have to make to the single-cycle datapath and control if this simplified architecture were to be used?
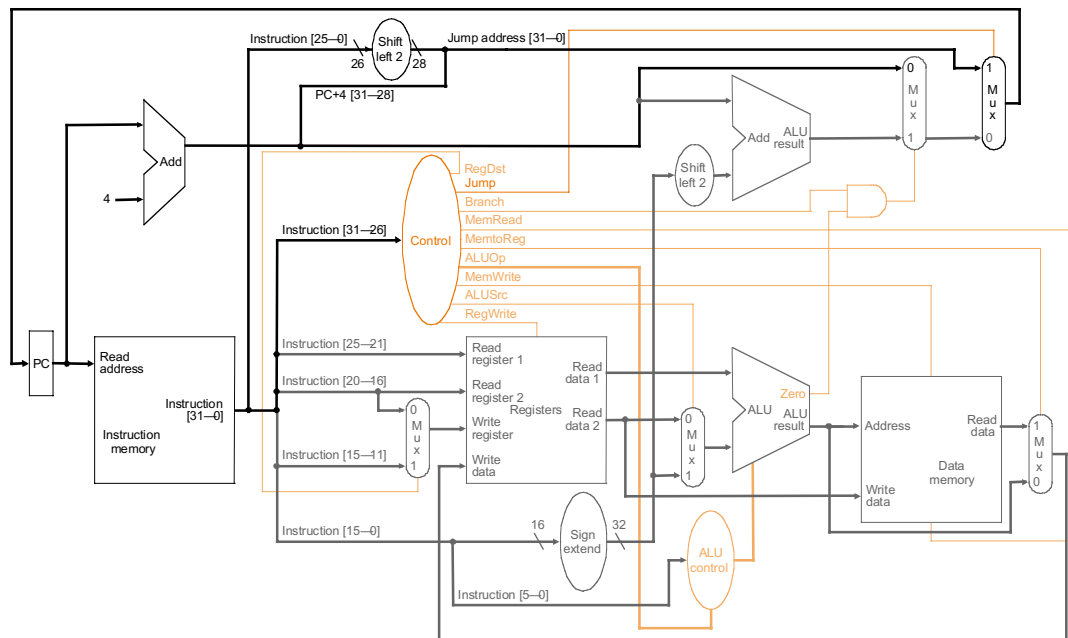


(b) (10 points) If the delay for the instruction  and data memory is 2 ns, the register file delay (read or write) is 1 ns, and the ALU delay is 2 ns, what are the clock cycles required for the original datapath and for the modified datapath? What is the highest percentage of load-store instructions with offsets that could be tolerated without total performance being degraded?

10. (10 points) Use the following code fragment:

```
loop: lw    $1, 0($2)
      addi  $1, $1, 4
      sw    $1, 0($2)
      addi  $2, $2, 4
      bne   $2, $3, loop
```

Assume that the initial value of $2 is $3 — 396 and that this code fragment is run on a machine with a 500-MHz clock that requires the following number of cycles for each instruction:

| Instruction | Cycles |
|---|---|
| addi | 1 |
| add | 2 |
| lw, sw | 3 |
| bne | 4 |

In the worst case, how many seconds will it take to execute this code?

11. (10 points) What size messages would result in ATM outperforming Ethernet by a factor of ten, assuming the following latencies and bandwidths?

| Characteristic | Ethernet | ATM |
|---|---|---|
| Bandwidth from node to network | 1.125 MB/sec | 10 MB/sec |
| Interconnect latency | 15 μs | 50 μs |
| HW latency to/from network | 6 μs | 6 μs |
| SW overhead sending to network | 200 μs | 207 μs |
| SW overhead receiving from network | 241 μs | 360 μs |

12. (15 points) The MicroBlaze embedded soft core is a reduced instruction set computer (RISC) optimized for implementation in Xilinx field programmable gate arrays (FPGAs). It has a 32-bit instruction word with three operands and two addressing modes. MicroBlaze instructions are either Type A or Type B. The instruction formats for each are given below:

| Bits | 0-5 | 6-10 | 11-15 | 16-20 | 20-31 |
|------|-----|------|-------|-------|-------|
| Type A | opcode | Rd | Ra | Rb | 00000000000 |
| Type B | opcode | Rd | Ra | | Immediate |
| | | | | | 16-31 |

For arithmetic/logical instructions, we have:

      Rd ← Ra op Rb, where op is +, -, AND, OR, etc.      add   Rd, Ra, Rb

For loads:

      Rd ← MEM[Ra + Rb]      lw   Rd, Ra, Rb

or      Rd ← MEM[Ra + Immediate]      lw   Rd, Ra, Imm

For stores:

      MEM[Ra + Rb] ← Rd      sw   Rd, Ra, Rb

      MEM[Ra + Immediate] ← Rd      sw   Rd,  Ra, Imm

For beq:

      PC ← Rb if Ra = 0      beq   Ra, Rb

The MicroBlaze has a 3 stage pipeline as follows:

| Fetch | Decode | Execute |
|-------|--------|---------|

The register file is read in the Decode state and the ALU and memory operations take place in the Execute stage. Even without data hazards, the pipeline has stalls. Loads and stores require an additional cycle to complete (a total of 4) and beq requires two extra cycles to complete (a total of 5) if taken. If the beq is not taken, no stalls are required.

For the following MicroBlaze code, how many cycles will it take to execute?

```
add   $5, $7, $9
lw    $9, $5, $3
sw    $9, $5, 200
sub   $5, $5, $5
beq   $5, $2
add   $5, $5, 20
```