The University of Alabama in Huntsville
Electrical & Computer Engineering Department
CPE 431 01
Final Exam
November 30, 2010

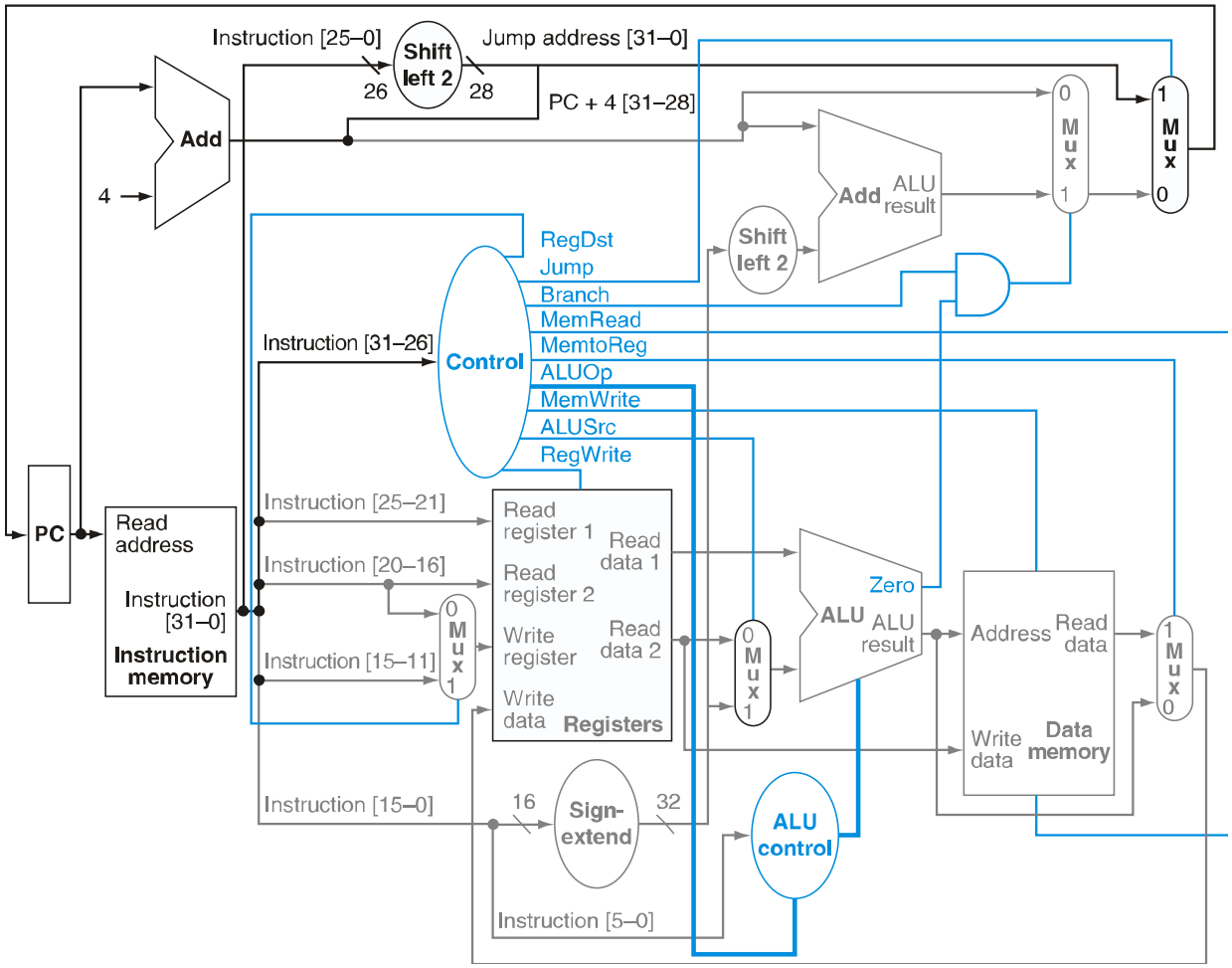
Name: _____

1. (1 point) A _____ is one that offers the programmer a single physical address space across all processors.
2. (1 point) As processors operating in parallel normally share data, they need to coordinate when operating on shared data, this coordination is called _____ .
3. (1 point) _____ allows sharing of functional units of a single processor in an overlapping fashion.
4. (1 point) A virtual memory miss is called a _____.
5. (1 point) _____(True or False) Overhead for communication is one of the reasons that it is difficult to write fast parallel processing programs.

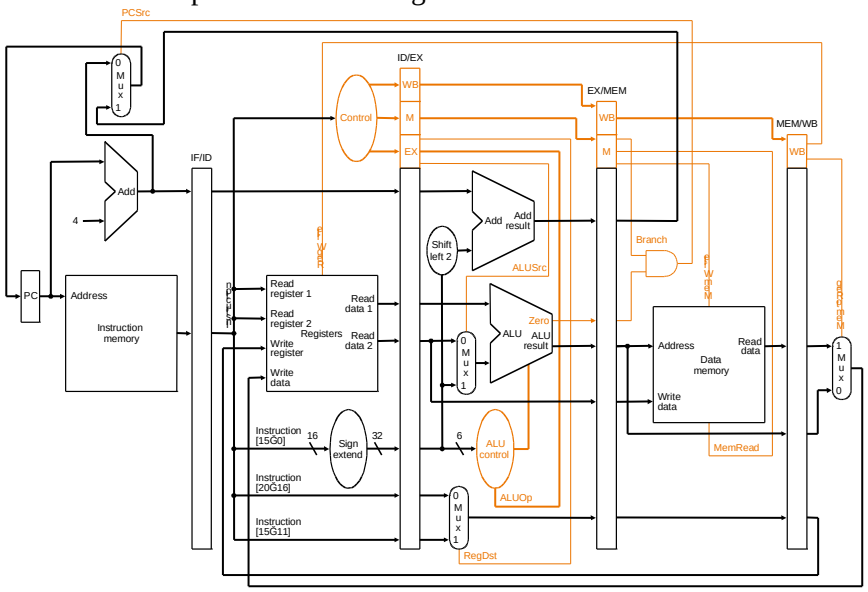
6. (10 points) Consider two different implementations of the same instruction set architecture. There are four classes of instructions, A, B, C, and D. The clock rate and CPI of each implementation are given in the following table. Given a program with 10^6 instructions divided into classes as follows" 10% class A, 20% class B, 50% class C and 20% class D, which implementation is faster?

	Clock rate	CPI Class A	CPI Class B	CPI Class C	CPI Class D
P1	1.5 GHz	1	2	3	4
P2	2 GHz	2	2	2	2

7. (10 points) Consider the following instruction: `swi Rd, Rs(Rt)` whose operation is defined by the following register transfer statement Mem[Rs + Rt] = Rd. What must be changed in the single cycle datapath to add this instruction to the MIPA ISA?



8. (10 points) Consider executing the following code on a pipelined datapath like the one shown which (a)has no forwarding, (b)does support jump and (c) has branch completion in the ID stage. A jump instruction completes in the ID stage.




```
sort:    addi $sp, $sp, -20
         sw   $ra, 16($sp)
         sw   $s3, 12($sp)
         sw   $s2, 8($sp)
         sw   $s1, 4($sp)
         sw   $s0, 0($sp)
         add  $s2, $a0, $zero
         add  $s3, $a1, $zero
         add  $s0, $zero, $zero
for1tst: slt  $t0, $s0, $s3
         beq  $t0, $zero, exit1
         addi $s1, $s0, -1
for2tst: slt  $t0, $s1, $zero
         bne  $t0, $zero, exit2
         add  $t1, $s1, $s1
         add  $t1, $t1, $t1
         add  $t2, $s2, $t1
         lw   $t3, 0($t2)
         lw   $t4, 4($t2)
         slt  $t0, $t4, $t3
         beq  $t0, $zero, exit2
         add  $a0, $s2, $zero
         add  $a1, $s1, $zero
         jal  swap
         addi $s1, $s1, -1
         j    for2tst
exit2:   addi $s0, $s0, 1
         j    for1tst
exit1:   lw   $s0, 0($sp)
         lw   $s1, 4($sp)
         lw   $s2, 8($sp)
         lw   $s3, 12($sp)
         lw   $ra, 16($sp)
         addi $sp, $sp, 20
         jr   $ra
```

If the `addi $s1` instruction one instruction before the `for2tst` label begins executing in cycle 1 and the `bne $t0, $zero, exit2` is taken, what are the instructions in each stage of the pipeline in the 14th cycle? If there is a bubble in any stage of the pipeline, also indicate which instruction was there before it became a bubble.

IF: _____

ID: _____

EX: _____

MEM: _____

WB _____

Cycle	IF	ID	EX	MEM	WB
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					

9. (10 points) Assume that the variables `f`, `g`, `h`, `i`, and `j` are assigned to registers `$s0`, `$s1`, `$s2`, `$s3`, and `$s4`, respectively. Assume that the base address of the arrays `A` and `B` are in registers `$s6` and `$s7`, respectively. Additionally, A and B are arrays of integers. What is the corresponding MIPS assembly code for the following C statement?

f = g – A[B[4]]

10. (5 points) What MIPS instruction does the following collection of bits represent?

0x8D080040

11. (5 points) What is the minimum number of bits needed to represent -150 in 2's complement? What is that representation in hexadecimal?

12. (10 points) Here is a series of address references given as word addresses: 1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6. Assuming a two-way set associative cache with two word blocks and a total size of 16 words that is initially empty, (a) label each reference in the list as a hit or a miss and (b) show the entire history of the cache

13. (10 points) Mean Time Between Failures (MTBF), Mean Time To Replacement (MTTR), and Mean Time To Failure (MTTF) are useful metrics for evaluating the reliability and availability of a storage resource. Explore these concepts by answering the questions about a device with the following metrics.

MTTF	MTTR
5 Years	10 days

(a) Calculate the MTBF for the devices.
(b) Calculate the availability for this device.

14. (10 points) Consider the following portions of two different programs running at the same time on three processors in a symmetric multicore processor (SMP). Assume that before this code is run, w is 2, x is -2 and y and z are 1. w, x, y, and z are type `int`.

Core 1: `y = 5/z;`
Core 2: `w = x + y + 1;`
Core 3: `z = w*x + y;`

What are all the possible resulting values of w, x, y, and z? Show all possible interleavings of instructions and the resulting values of w, x, y, and z.

15. (5 points) Represent -16.0 in single precision floating-point format.

16. (10 points) The following code is written in MATLAB, where elements within the same column are stored contiguously. References to which variables exhibit spatial locality? I and J are both arrays of integers 8000 by 8000.

```
for J=1:8;
   for I=1:8000;
      A(I,J) = B(J,1) + A(J, I);
```