

**The University of Alabama in Huntsville**  
**ECE Department**  
**CPE 431 01**  
**Test 1**  
**October 3, 2017**

Name: \_\_\_\_\_

**You *must* show your work to receive full credit: You may use additional sheets of paper for your work, please put your name on each additional sheet.**

Remember:  $ET = IC * CPI * CT$

1. (1 point) When a planned instruction cannot execute in the proper cycle because the hardware does not support the combination of instructions that are set to execute, it is due to a \_\_\_\_\_.
2. (1 point) An \_\_\_\_\_ is a value used to delineate the location of a specific data element within a memory array.
3. (1 point) \_\_\_\_\_ numbers are numbers expressed in base 16.
4. (1 point) The \_\_\_\_\_ is the field that denotes the operation and format of an instruction.
5. (1 point) A \_\_\_\_\_ is a link to the calling site that allows a procedure to return to the proper address; in MIPS it is stored in register \$ra.
6. (10 points) Consider a computer running a program that requires 250 s, with 70s spent executing FP instructions, 85 s executing L/S instructions, and 40 s spent executing branch instructions. By how much is the total time reduced if the time for INT operations is reduced by 20%

7. (15 points) Translate the following C code to MIPS. Assume that the variables `f`, `g`, `h`, `i` and `j` are given and are assigned to registers `$s0`, `$s1`, `$s2`, `$s3`, and `$s4`, respectively. Assume that the base address of the arrays `A` and `B` are in registers `$s6` and `$s7`, respectively. Assume that the elements of the arrays `A` and `B` are 4-byte words:

**`B[i+j] = A[8]`**

8. (15 points) For a benchmark assume an execution time of 1040 s, CPI of 2.59, and clock rate of 3.5 GHz. If the execution time is reduced by an additional 10% without affecting the CPI and with a clock rate of 4 GHz, determine the number of instructions.

9. (5 points) Unconditional branches are not part of the MIPS assembly language. Show the MIPS I instruction(s) that can be used to have the same effect as an unconditional branch.

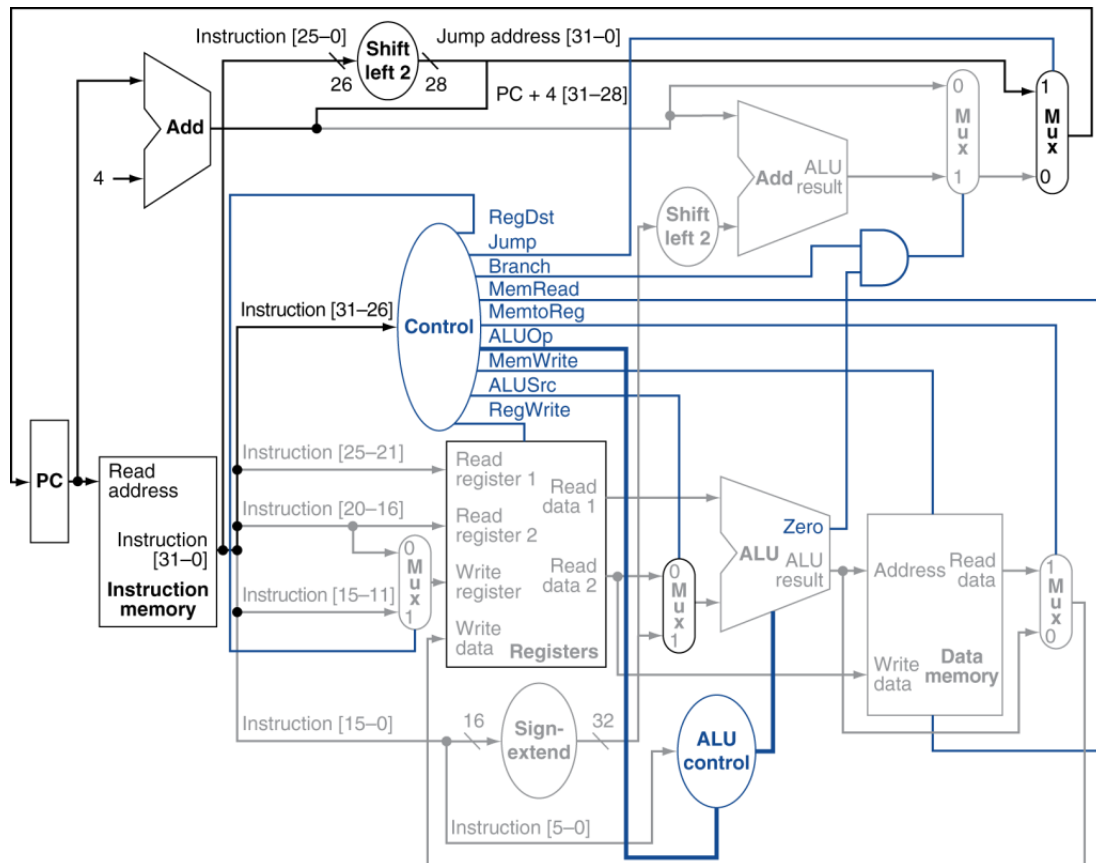
10. (10 points) A MIPS processor fetches the following instruction word:

0001 0000 1000 0101 0000 0001 0010 1100

Assume that data memory is all zeros and that the processor's registers have the following values at the beginning of the cycle in which the above instruction word is fetched.

r0	r1	r2	r3	r4	r5	r6	r8	r12	r31
0	-1	2	-3	-4	10	6	8	2	-16

What instruction is this and what is the output of the sign-extend, Zero, and the ALU result for this instruction word?



Sign Extend: \_\_\_\_\_

Zero: \_\_\_\_\_

ALU result: \_\_\_\_\_

11. (15 points) In this exercise, we examine how data dependences affect execution in the basic 5-stage pipeline. Refer to the following sequence of instructions:

```
add    $s2, $s2, $s1
sw     $s2, 0($t1)
lw     $s1, -4($s1)
add    $s2, $s2, $s1
```

Assume there is no forwarding in this pipelined processor. Indicate hazards and add nop instructions to eliminate them.

12. (10 points) In this exercise, we examine how pipelining affects the clock cycle time of the processor. Problems in this exercise assume that individual stages of the datapath have the following latencies:

IF	ID	EX	MEM	WB
300 ps	250 ps	180 ps	350 ps	200 ps

Also, assume that instructions executed by the processor are broken down as follows:

alu	beq	lw	sw
45%	20%	20%	15%

What is the clock cycle time in a pipelined and non-pipelined processor?

13. (15 points) Write down the hexadecimal representation of the decimal number -1468.265625 in both the IEEE 754 single and double precision formats.