The University of Alabama in Huntsville
Electrical & Computer Engineering Department
CPE 431 01
Final Exam
December 10, 2012

Name: _____

1. (1 point) Processors that are part of an SMP need to coordinate when sharing data, this process is called _____.
2. (1 point) _____ are collections of commodity computers connected via standard networks..
3. (1 point) An SMP only needs one copy of the _____.
4. (1 point) _____ multithreading switches between threads on each instruction, often done round robin.
5. (1 point) One reason that it is difficult to write fast parallel processing programs is _____.
6. (10 points) The following problems deal with translating from C to MIPS. Assume that t he variables f, g,h, `i` and `j` are assigned to registers `$s0`, `$s1`, `$s2`, `$s3`, and `$s4`, respectively. Assume that the base address of the arrays `A` and `B` are in registers `$s6` and `$s7`, respectively. Assume that the elements of the arrays `A` and `B` are 4-byte words. Write the MIPS statements that accomplish this function.

```
B[i] = A[i] + B[i];
```

7. (15 points) Here is a series of address references given as word addresses: 1, 4, 8, 5, 20, 17, 19, 56, 209, 11, 4, 43, 5, 36, 8, 16. Assuming a direct mapped cache with two word blocks and a total size of 16 words that is initially empty, (a) label each reference in the list as a hit or a miss and (b) show the entire history of the cache

8. (5 points) Represent 351285.75 as a double precision floating point number.Express your answer in hexadecimal.

9. (10 points) Mean Time Between Failures (MTBF), Mean Time To Replacement (MTTR), and Mean Time To Failure (MTTF) are useful metrics for evaluating the reliability and availability of a storage resource. Explore these concepts by answering the questions about a device with the following metrics.

MTTF	MTTR
3 Years	12 days

(a) Calculate the MTBF for the devices.
(b) Calculate the availability for this device.

10. (15 points) A program repeatedly performs a three-step process: It reads in a 8-KB block of data from disk, does some processing on that data, and then writes out the result as another 8-KB block elsewhere on the disk. Each block is contiguous and randomly located on a single track on the disk. The disk drive rotates at 9600 RPM, has an average seek time of 8 ms, and has a transfer rate of 32 MB/sec. The controller overhead is 2 ms. No other program is using the disk or processor, and there is no overlapping of disk operation with processing. The processing step takes 20 million clock cycles, and the clock rate is 500 MHz. What is the overall speed of the system in blocks processed per second?

11. (15 points) The following table shows the number of instructions for a program.

	Arithmetic	Store	Load	Branch	Total
	750	150	600	100	1600

Assume that arithmetic instructions take 1 cycle, load and store 4 cycles, and branches 3 cycles and that the program executes on a 2 GHz processor. If the number of load instructions can be reduced by 40 %, what is the speedup and the CPI?

12. (5 points) What is the value of the following 32 bits if they represent a single precision floating point number?

0x8880B340

13. (10 points) The MicroBlaze embedded soft core is a reduced instruction set computer (RISC) optimized for implementation in Xilinx field programmable gate arrays (FPGAs). It has a 32-bit instruction word with three operands and two addressing modes. MicroBlaze instructions are either Type A or Type B. The instruction formats for each are given below:

Bits	0-5	6-10	11-15	16-20	20-31
Type A	opcode	Rd	Ra	Rb	00000000000
Type B	opcode	Rd	Ra	Immediate	
				16-31	

For arithmetic/logical instructions, we have:

Rd ← Ra op Rb, where op is +, -, AND, OR, etc. `add Rd, Ra, Rb`

For loads:

Rd ← MEM[Ra + Rb] `lw Rd, Ra, Rb`

or Rd ← MEM[Ra + Immediate] `lw Rd, Ra, Imm`

For stores:

MEM[Ra + Rb] ← Rd `sw Rd, Ra, Rb`

MEM[Ra + Immediate] ← Rd `sw Rd, Ra, Imm`

For beq:

PC ← Rb if Ra = 0 `beq Ra, Rb`

The MicroBlaze has a 3 stage pipeline as follows:

Fetch	Decode	Execute

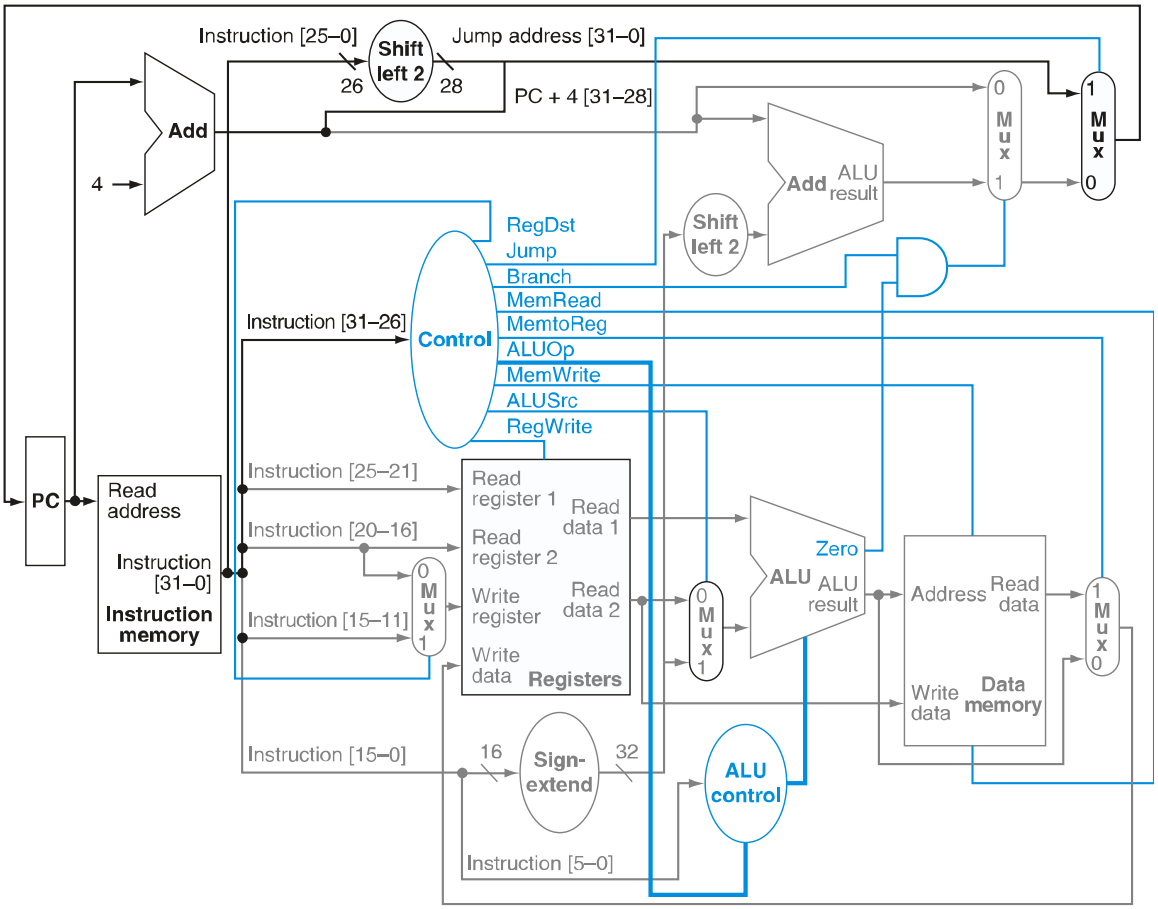
The register file is read in the Decode state and the ALU and memory operations take place in the Execute stage. Even without data hazards, the pipeline has stalls. Loads and stores require an additional cycle to complete (a total of 4) and beq requires two extra cycles to complete (a total of 5) if taken. If the beq is not taken, no stalls are required.

For the following MicroBlaze code, how many cycles will it take to execute?

```
add   $5, $7, $9
lw    $9, $5, $3
sw    $9, $5, 200
sub   $5, $5, $5
beq   $5, $2
add   $5, $5, 20
```

14. (10 points) In this exercise, we examine how latencies of individual components of the datapath affect the clock cycle time of the entire datapath, and how these components are utilized by instructions. For problems in this exercise, assume the following latencies for logic blocks in the datapath:

	I-Mem	Add	Mux	ALU	Regs	D-Mem	Sign-Extend	Shift-Left-2	Control
	200 ps	80 ps	20 ps	120 ps	120 ps	300 ps	15 ps	10 ps	240 ps



What is the clock cycle for this datapath?