The University of Alabama in Huntsville
ECE Department
CPE 431 01
Test 2
November 14, 2019

Name: _____

1. (1 point) _____ locality states that items close to items referenced recently will be referenced.
2. (1 point) Miss is to cache as _____ is to physical memory.
3. (1 point) _____ storage retains information when power is removed.
4. (1 point) A _____ hazard occurs when a planned instruction cannot execute in the proper clock cycle because the hardware does not support the combination of instructions that are set to execute.
5. (1 point) An _____ is an unscheduled event that disrupts program execution.
6. (10 points) The following code is written in MATLAB, where elements within the same column are stored contiguously. Do `A(j, i)` and `A(i, j)` exhibit spatial locality? temporal locality? Explain your answers. A, B, and C are all arrays of integers 8000 by 8000.

```
for i = 1:8000
  for j = 1:8000
      A(i,j ) = B(j, 1) + A(j, i) + C(1, i);
```

7. (20 points) Here is a series of address references given as byte addresses: 118, 483, 2069, 321, 368, 1505, 812, 2832, 373, 1411, 511, 122, 690, 4820, 1714, 1508, 2070, 1080. Assuming a two-way set associative-mapped cache with 2-word blocks and a total size of 32 32-bit words that is initially empty and uses LRU, (a) label each reference in the list as a hit or a miss and (b) show the entire history of the cache, including tag and data.

Byte Address (Decimal)	Byte Address (Hexadecimal)	Byte Address (Binary)	Hit/Miss
118	76	0000 0000 0111 0110	
483	1E3	0000 0001 1110 0011	
2069	815	0000 1000 0001 0101	
321	141	0000 0001 0100 0001	
368	170	0000 0001 0111 0000	
1505	5E1	0000 0101 1110 0001	
812	32C	0000 0011 0010 1100	
2832	B10	0000 1011 0001 0000	
373	175	0000 0001 0111 0101	
1411	583	0000 0101 1000 0011	
511	1FF	0000 0001 1111 1111	
122	7A	0000 0000 0111 1010	
690	2B2	0000 0010 1011 0010	
1508	5E4	0000 0101 1110 0100	
2070	816	0000 1000 0001 0110	
1080	438	0000 0100 0011 1000	

8. (20 points) Consider the execution of the following loop in a statically scheduled superscalar processor that has full forwarding. Additionally, any branches are resolved in the EX stage.

```
Loop:  lw   $t0, 0($s1)
       lw   $t4, 0($s2)
       mul  $t0, $t0, $t4
       add  $t0, $t3, $t0
       addi $s1, $s1, -8
       addi $s2, $s2, -8
       bne  $s1, $zero, Loop
```

a. (15 points) Unroll this loop so that three iterations of it are done at once and schedule it for maximum performance on a 2-issue static superscalar processor that has one slot for R-type/branch instructions and one slot for lw/sw instructions. Assume that the loop always executes a number of iterations that is a multiple of 3. You can use registers **$10** through **$20** when changing the code to eliminate dependences.

b. (5 points) Calculate the number of cycles for the original and for the unrolled, scheduled code and the speedup of unrolled, scheduled compared to the original.

Cycle	R-type/branch	lw/sw
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		

9. (10 points) Consider an SEC code that protects 8 bit words with 4 parity bits. If we read the value 0x294, is there an error? If so, correct the error.

10. (15 points) Virtual memory uses a page table to track the mapping of virtual addresses to physical addresses. The following table is a stream of virtual addresses as seen on a system. Assume 16 KiB pages, byte addressing, a four-entry fully associative TLB, and true LRU replacement. If pages must be brought in from disk, increment the next largest page number. Given the address stream, and the shown initial state of the TLB and page table, show the final state of the system. Also list for each reference if it is a hit in the page table, or a page fault.

TLB

Valid	Tag	Physical Page Number
1	11	12
1	7	4
1	3	6
0	4	9

Page table

VPN	Valid	Physical page or in disk
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	11
6	0	Disk
7	1	4
8	0	Disk
9	0	Disk
10	1	3
11	1	12
12	0	Disk

Address	TLB Hit/Miss	Page Table Hit/Miss	Page Fault Y/N
92,158			
52,250			
120,000			
119,200			
28,156			
73,004			
63,998			
20,000			

11. (10 points) Assume that the following MIPS code is executed on a pipelined processor with a 5-stage pipeline, full forwarding, and a predict-not-taken branch predictor:

```
            lw    r2, 0(r1)
label1:     beq   r2, r0, label2     # not taken once, then taken
            lw    r3, 0(r2)
            beq   r3, r0, label1     #taken
            add   r1, r3, r1
label2:     sw    r1, 0(r2)
```

Draw the pipeline execution diagram for this code, assuming there are no delay slots and that branches execute in the EX stage.

Cycle	IF	ID	EX	MEM	WB
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					

12. (10 points) Calculate the total number of bits required for a cache with the parameters listed below, assuming a 32-bit address and byte addressability. Include valid and dirty bits.

Cache Data Size: 256 KiB
Cache Block Size: 8 32-bit words
Cache Set Associativity: 8-way