The University of Alabama in Huntsville
Electrical & Computer Engineering Department
CPE 431 01
Final Exam
December 4, 2008

Name: _____

1. (1 point) A _____ is a thin disk sliced from a silicon crystal ingot.
2. (1 point) A _____ is a set of computers connected over a local area network that function as a single large multiprocessor.
3. (1 point) A _____ is a systems program that places an object program in main memory so that it is ready to execute.
4. (1 point) The _____ is the register containing the address of the instruction in the program being executed.
5. (1 point) _____(True or False) The clock frequency of a pipelined processor is determined by the slowest stage.

6. (10 points) The table below shows the number of floating-point operations executed in two different programs and the runtime for those programs on three different machines:

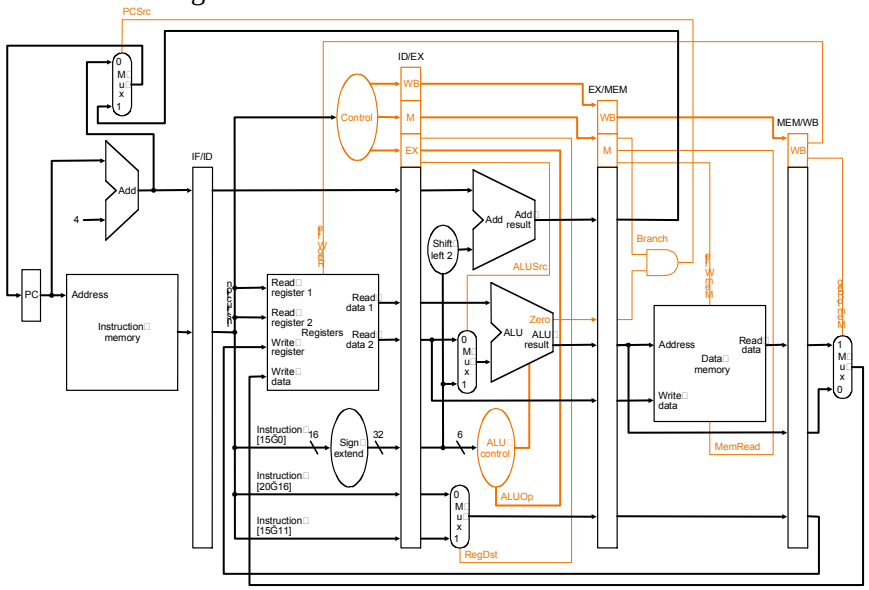
Program	Floating-point operations	Execution time in seconds		
		Computer A	Computer B	Computer C
1	10,000,000	1	10	20
2	100,000,000	1000	100	20

One user has told you that the two programs above constitute the bulk of his workload, but he does not run them equally. The user wants to determine how the three machines compare when the workload consists of different mixes of these programs. Suppose the total number of FLOPS executed in the workload is equally divided among the two programs. Find which machine is fastest for this workload and by how much.

7. (5 points) Write a minimal sequence of actual MIPS instructions to accomplish the samething as the following pseudoinstruction:

```
clear $t5
```

8. (10 points) Consider executing the following code on a pipelined datapath like the one shown which has no forwarding.




```
sort:    addi$sp, $sp, -20
         sw  $ra, 16($sp)
         sw  $s3, 12($sp)
         sw  $s2, 8($sp)
         sw  $s1, 4($sp)
         sw  $s0, 0($sp)
         add $s2, $a0, $zero
         add $s3, $a1, $zero
         add $s0, $zero, $zero
for1tst: slt $t0, $s0, $s3
         beq $t0, $zero, exit1
         addi$s1, $s0, -1
for2tst: slt $t0, $s1, $zero
         bne $t0, $zero, exit2
         add $t1, $s1, $s1
         add $t1, $t1, $t1
         add $t2, $s2, $t1
         lw  $t3, 0($t2)
         lw    $t4, 4($t2)
         slt   $t0, $t4, $t3
         beq   $t0, $zero, exit2
         add   $a0, $s2, $zero
         add   $a1, $s1, $zero
         jal   swap
         addi  $s1, $s1, -1
         j     for2tst
exit2:   addi  $s0, $s0, 1
         j     for1tst
exit1:   lw    $s0, 0($sp)
         lw    $s1, 4($sp)
         lw    $s2, 8($sp)
         lw    $s3, 12($sp)
         lw    $ra, 16($sp)
         addi  $sp, $sp, 20
         jr    $ra
```

If the `add $s2` instruction three instructions before the `for1tst` label begins executing in cycle 1 and the `beq $t0, $zero, exit2` is not taken, what are the values stored in the following fields of the IF/ID pipeline register in the 15th cycle? Assume that before the instructions are executed, the state of the machine was as follows:

The PC has the value 400_{10}, the address of the `add $s2` instruction
Every register has the initial value 30_{10} plus the register number.
Every memory word accessed as data has the initial value 1000_{10} plus the byte address of the word.

Fill in all of the fields, even if the current instruction in that stage is not using them.

IF/ID.Instruction
IF/ID.PCInc =

Cycle	IF	ID	EX	MEM	WB
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					

9. (10 points) Using the MIPS program shown, determine the instruction format for each instruction and the decimal values of each instruction field.

```
      addi  $v0, $zero, 0     # Initialize count
loop: lw    $v1, 0($a0)       # Read next word from source
      sw    $v1, 0($a1)       # Write to destination
      addi  $a0, $a0, 4       # Advance pointer to next source
      addi  $a1, $a1, 4       # Advance pointer to next destination
      beq   $v1, $zero, loop  # Loop if word copied != zero
```

10. (5 points) For an m-stage pipeline, how many cycles does it take to execute n instructions if the pipeline is empty when these instructions begin to execute? _____

11. (10 points) Here is a series of address references given as word addresses: 1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6. Assuming a direct-mapped cache with four-word blocks and a total size of 16 words that is initially empty, (a) label each reference in the list as a hit or a miss and (b) show the final contents of the cache.

12. (10 points) Consider the case of a six-deep pipeline where the branch is resolved at the end of the third stage for unconditional branches and at the end of the fifth cycle for conditional branches. The program run on this pipeline has the following branch frequencies (as percentages of all instructions) are as follows:

    Conditional branches 20%

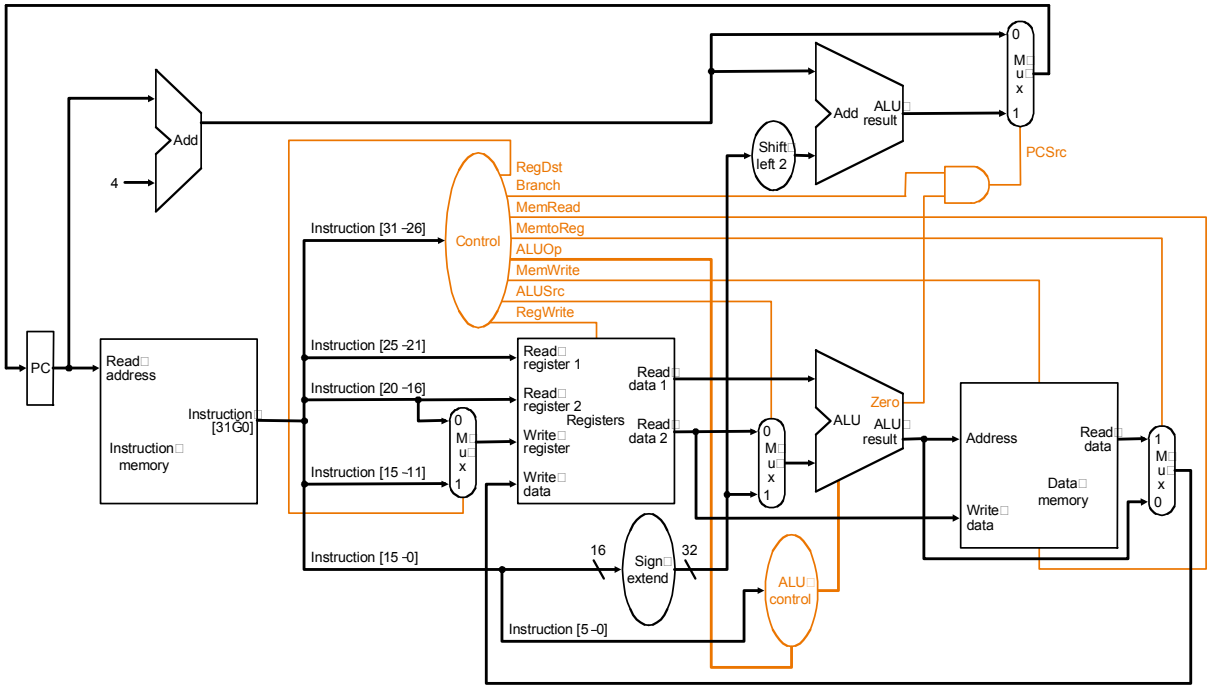
    Jumps and calls 5%

60 % of the conditional branches are taken. Assuming that the CPI of the program, neglecting branch hazards, is 1.0, how much slower is the real number, when branch hazards are considered?

13. (5 points)What single precision floating-point number does the following collection of 32 bits represent?

```
1111 1100 1010 1111 1111 0000 0000 0000
```

14. (10 points) Describe the effect that a single stuck-at1 fault (i.e., regardless of what it should be, the signal is always 1) would have for the signals shown below, in the single-cycle datapath in Figure 5.17 on page 307. Which instructions, if any, will not work correctly? Explain why. Consider each of the following faults separately: RegDst = 0, ALUSrc =0, MemtoReg = 0, Zero = 0.



- RegDst s-a-0:
- ALUSrc s-a-0:
- MemtoReg s-a-0:
- Zero s-a-0:

Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALU Op1	ALU Op0
R-format	1	0	0	1	0	0	0	1	0
`lw`	0	1	1	1	1	0	0	0	0
`sw`	d	1	d	0	0	1	0	0	0
`beq`	d	0	d	0	0	0	1	0	1

d = don't care

15. (10 points) A secret agency simultaneously monitors cellular phone conversations and multiplexes the data onto a network with a bandwidth of 10 MB/sec and an overhead latency of 250 μs per 5 KB message. Calculate the transmission time per message and determine whether there is sufficient bandwidth to support this application. Assume that the phone conversation data consists of 4 bytes sampled at a rate of 5 KHz

16. (10 points) Consider a write-back cache used for a processor with a bus and memory system as described in the book on page 665 (assume that writes require the same amount of time as reads). The time to transfer 8-word blocks is 49 cycles and the time to transfer 16-word blocks is 57 cycles. Additionally, the following performance measurements have been made: The cache miss rate is 0.05 misses per instruction for block sizes of 8 words. The cache miss rate is 0.03 misses per instruction for block sizes of 16 words. For either block size, 40% of the misses require a write-back operation, while the other 60% require only a read.

Assuming that the processor is stalled for the duration of a miss (including the write-back time if a write-back is needed), find the number of cycles per instruction that are spent handling cache misses for each block size. (Hint: First compute the miss penalty.)