The University of Alabama in Huntsville
Electrical & Computer Engineering Department
CPE 431 01
Final Exam
November 30, 2017

Name: _____

You must show your work to receive full credit!!

1. (1 point) _____ locality states that an item referenced is likely to be referenced if its neighbor is referenced.
2. (1 point) _____ are programs specifically chosen to measure performance.
3. (1 point) _____ are networks of off-the-shelf, whole computers.
4. (1 point) A _____ protocol maintains consistency in the value of data between several processors.
5. (1 point) _____ (True or False) Overhead for communication is one of the reasons that it is difficult to write fast parallel processing programs.
6. (8 points) What number does 0xE09B AC00 represent, assuming the IEE 754 single precision format?

7. (15 points) Here is a series of address references given as hexadecimal word addresses: 21, 4, 8, 5, 20, 37, 19, 5E, 209, 11, 4, 43, 5, 3E, 8, 16, 59, 187, 2E8, 30. Assuming a direct mapped cache with four word blocks, a total size of 16 words that is initially empty, (a) label each reference in the list as a hit or a miss and (b) show the entire history of the cache, including tag and data.

Word Address (Hexadecimal)	Word Address (Decimal)	Binary	Miss/Hit
0x21	33	0000 0000 0010 0001	
0x4	4	0000 0000 0000 0100	
0x8	8	0000 0000 0000 1000	
0x5	5	0000 0000 0000 0101	
0x20	32	0000 0000 0010 0000	
0x37	55	0000 0000 0011 0111	
0x19	25	0000 0000 0001 1001	
0x5E	86	0000 0000 0101 1110	
0x209	521	0000 0010 0000 1001	
0x11	17	0000 0000 0001 0001	
0x4	4	0000 0000 0000 0100	
0x43	67	0000 0000 0100 0011	
0x5	5	0000 0000 0000 0101	
0x3E	62	0000 0000 0011 1110	
0x8	8	0000 0000 0000 1000	
0x16	22	0000 0000 0001 0110	
0x59	89	0000 0000 0101 1001	
0x187	391	0000 0001 1000 0111	
0x2E8	744	0000 0010 1110 1000	
0x30	48	0000 0000 0011 0000	

8. (10 points) Consider the following portions of three programs running at the same time on three processors in a symmetric multicore processor (SMP). Assume that before this code is run, w is 4 x is -2 and y is 2 and z is 3. w, x, y, and z are type `int`. What are all the possible outcomes of executing these instructions?

Core 1: `y = 5/z + w;`
Core 2: `x = (x + y)/w + 1;`
Core 3: `z = w*(x – y) + z;`

9. (10 points) One of the biggest impediments to widespread use of virtual machines is the performance overhead incurred by running a virtual machine. Listed below are various performance parameters and application behavior.

Base CPI	Privileged O/S Accesses per 10,000 Instructions	Performance Impact to Trap to the Guest O/S	Performance Impact to Trap to VMM	I/O Accesses per 10,000 Instructions	I/O Access Time (Includes Time to Trap to Guest O/S)
1.5	120	15 cycles	175 cycles	30	1100 cycles

(a) (3 points) Calculate the CPI for the system listed above assuming that there are no accesses to I/O.
(b) (3 points) What is the CPI if the VMM performance impact doubles?
(c) (4 points) If a virtual machine software company wishes to obtain a 10% performance degradation, what is the longest possible penalty to trap to the VMM?

10. (10 points) Consider program P, which runs on a 2 GHz machine M in 10 seconds. An optimization is made to P, replacing all instances of multiplying a value by 8 (mult X, X, 8) with three instructions that set X to X + X thrice (add X, X; add X, X; add X, X) Call this new optimized program P'. The CPI of a multiply instruction is 6, and the CPI of an add is 1. After recompiling, the program now runs in 8.5 seconds on machine M. How many multiplies were replaced by the new compiler?

11. (7 points) The following list provides parameters of a virtual memory system.

Virtual Address (bits)	Physical DRAM Installed	Page Size	PTE Size (byte)
47	16 GiB	16 KiB	4

Using a multilevel page table can reduce the physical memory consumption of page tables, by only keeping active PTEs in physical memory.

(a) (5 points) How many levels of page tables will be needed in this case?

(b) (2 points) how many memory references are needed for address translation if missing in TLB?

12. (20 points) Consider the following loop in C and this MIPS assembly version. $s6 is the pointer to the base of array A and $s3 holds the value of y.

```
for (i = 0; i < 120; i++)
   A[i] = A[i] + y

        addi   $t0, $s6, 480          # $t0 ← &A[119]
        addi   $t1, $s6, $zero        # $t1 ← &A[0]
Loop:   lw     $t2, 0($t1)            # $t2 ← A[i]
        add    $t2, $t2, $s3          # $t2 ← A[i] + y
        sw     $t2, 0($t1)            # A[i] ← A[i] + y
        addi   $t1, $t1, 4            # $t1 ← &A[i+1]
        bne    $t0, $t1, Loop
```

Calculate the number of cycles it takes to execute this complete code snippet if

(a) (3 points) There is full forwarding and the bne completes in the EX stage

(b) (3 points) There is EX/MEM forwarding only and the bne completes in the EX stage

(c) (3 points) There is MEM/WB forwarding only and the bne completes in the EX stage

Then,

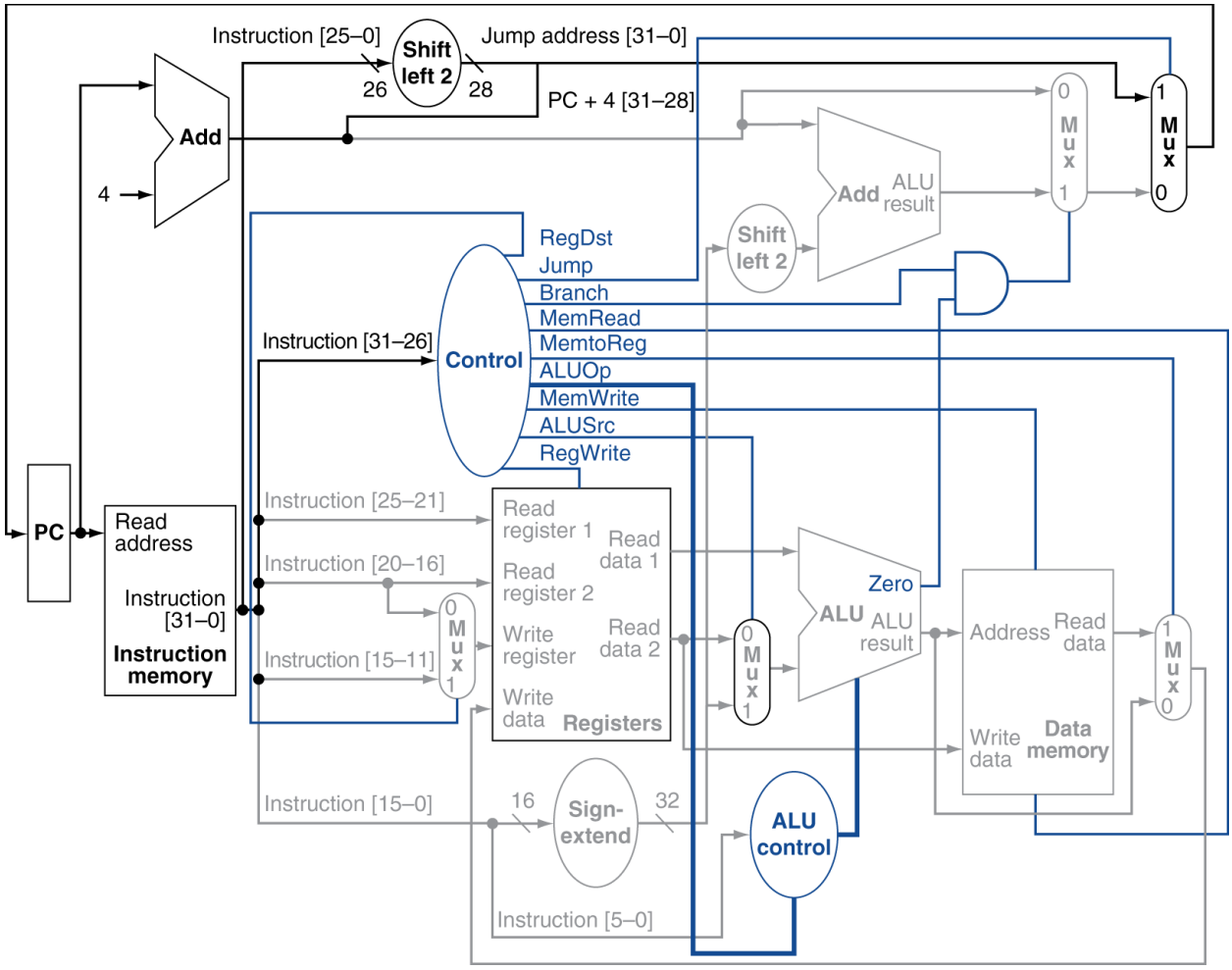
(d) (9 points) unroll this loop so that two iterations of the loop are done at a time and schedule the unrolled code for execution with full forwarding and branch completion in the EX stage.

(e) (2 points) Compare the execution times of the original unrolled code from part (a) and the unrolled, scheduled code from part (d).

13. (15 points) Consider the following idea: Let's modify the instruction set architecture and remove the ability to specify an offset for memory access instructions. Specifically, all load-store instructions with nonzero offsets would become pseudoinstructions and would be implemented using two instructions. For example:

```
addi $at, $t1, 104        # add the offset to a temporary
lw   $t0, $at             # new way of doing lw $t0, 104 ($t1)
```

(a) (5 points) Show the changes to the single-cycle datapath and control if this simplified architecture is used.



Instruction	RegDst	ALUSrc	Memto Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUOp0	
R-format	1	0	0	1	0	0	0	1	0	
lw	0	1	1	1	1	0	0	0	0	
sw	d	1	d	0	0	1	0	0	0	
beq	d	0	d	0	0	0	1	0	1	

d-don't care

(b) (6 points) If the delay for the instruction memory is 300 ps, the data memory is 200 ps, the register file delay (read or write) is 100 ps, the control (not ALU control) is 300 ps, and the ALU delay is 400 ps, and all other delays are neglible, what are the clock cycle times required for the original datapath and for the modified datapath?

(c) (4 points) What is the highest percentage of load-store instructions with offsets that could be tolerated without total performance being degraded?