The University of Alabama in Huntsville
ECE Department
CPE 431 01
Test 1 Solution
Fall 2019

You *must* show your work to receive full credit: You may use additional sheets of paper for your work, please put your name on each additional sheet.
Remember: ET = IC*CPI*CT

1. (1 point) Floating-point numbers are represented in _**scientific**_ notation.

2. (1 point) More fraction bits give you more _**precision**_.

3. (1 point) _**True**_ (True or False) The algorithm chosen can affect performance.

4. (2 points) A typical workload specifies both the _**programs**_ run and their _**frequencies**_.

5. (10 points) Write down the hexadecimal representation of the decimal number -52451.75 in the IEEE 754 double precision format.

```
/16        0   12              x2    0.75
/16       12   12              x2    1.5           1
/16      204   14              x2    1.0           1
/16     3278    3
/16    52451
```

$1100\ 1100\ 1110\ 0011.11 = 1.1001\ 1001\ 1100\ 0111\ 1 \times 2^{15}$
S = 1, EXP + BIAS = 15 + 1023 = 1038 = 100 0000 1110
Fraction = 1001 1001 1100 0111 1000
1100 0000 1110 1001 1001 1100 0111 1000 = 0xC0E9 9C78 0000 0000

6. (10 points) Translate the following C code to MIPS. Assume that the variables `f`, `g`, `h`, `i`, and `j` are given and are assigned to registers `$s0`, `$s1`, `$s2`, `$s3`, and `$s4`, respectively. Assume that the base address of the arrays A and B are in registers `$s6` and `$s7`, respectively. Assume that the elements of the arrays A and B are 4-byte words:

```
B[i] = A[j] + 12
```

```
sll    $t0, $s4, 2
add    $t0, $s6, $t0
lw     $t0, 0($t0)
addi   $t0, $t0, 12
sll    $t1, $s3, 2
add    $t1, $s7, $t1
sw     $t0, 0($t1)
```

7. (5 points) Assume the following register contents:

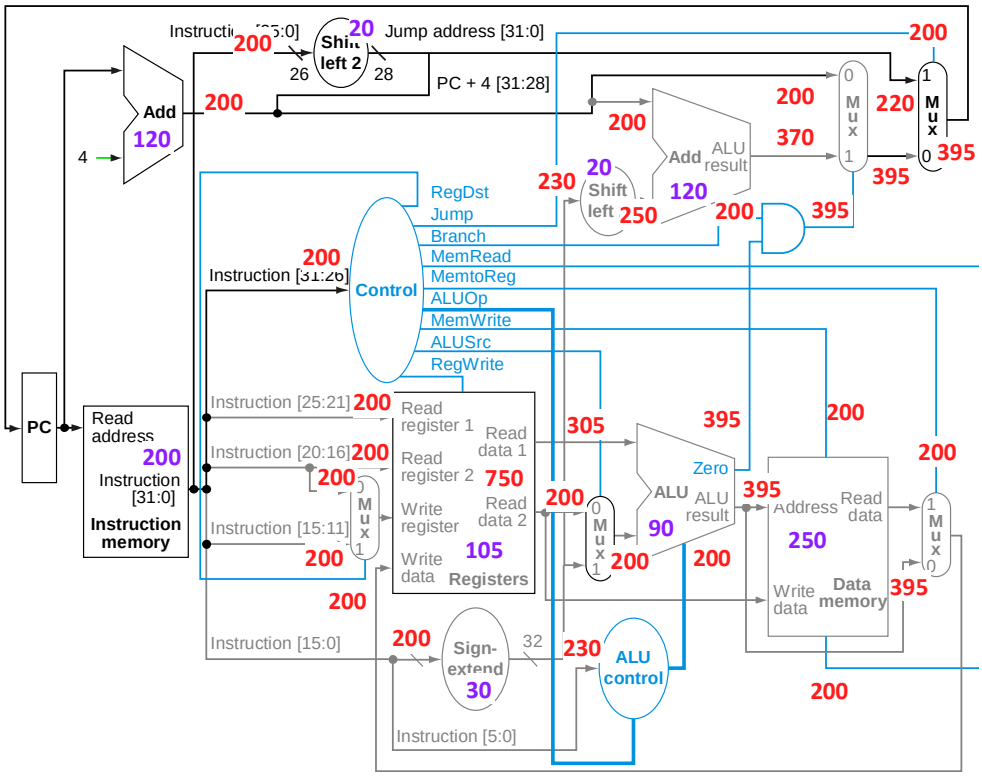
```
$t0 = 0xAAAAAAAA
$t1 = 0x12345678
```

What is the value of `$t2` for the following sequence of instructions?

```
sll   $t2, $t0, 5
andi  $t2, $t2, -1
$t0 = 1010 1010 1010 1010 1010 1010 1010 1010
$t2 (sll)=        0101 0101 0101 0101 0101 0101 0100 0000
-1(zero extend) = 0000 0000 0000 0000 1111 1111 1111 1111
$t2 (andi)      = 0000 0000 0000 0000 0101 0101 0100 0000
                = 0x0000 5540
```

8. (15 points) Assume the following latencies for logic blocks in the datapath: Any components not listed have zero delay. What is the clock cycle for this datapath? Show all of your work.

I-Mem	Add	ALU	Regs	D-Mem	SignExtend	Shift-Left-2
200 ps	120 ps	90 ps	105 ps	250 ps	30 ps	20 ps



Clock cycle = 750 ps

9. (5 points) If the current value of the PC is 0x0000 0000, can you use a single branch instruction to get to the PC address 0x0000 0EF2?

0x0000 0EF2 is not divisible by 4 so we cannot branch to it. If it were divisible by 4, it would be in range.

10. (15) Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes of instructions according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.2 GHz and CPIs of 1, 2, 4, and 3, and P2 with a clock rate of 3 GHz and CPIS of 1, 2, 3, and 4.

(a) (9 points) Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

CPI_{P1} = 0.1*1 + 0.2*2 + 0.5*4 + 0.2*3 = 3.1, CPI_{P2} = 0.1*1 + 0.2*2 + 0.5*3 + 0.2*4 = 2.8

$$\frac{P_{P1}}{P_{P2}} = \frac{ET_{P2}}{ET_{P1}} = \frac{IC_{P2} * CPI_{P2} * CT_{P2}}{IC_{P1} * CPI_{P1} * CT_{P1}} = \frac{IC_{P2} * CPI_{P2} * CR_{P1}}{IC_{P1} * CPI_{P1} * CR_{P2}} = \frac{1E6 * 2.8 * 2.2}{1E6 * 3.1 * 3} = 0.66$$

$$\therefore P2\ is\ faster$$

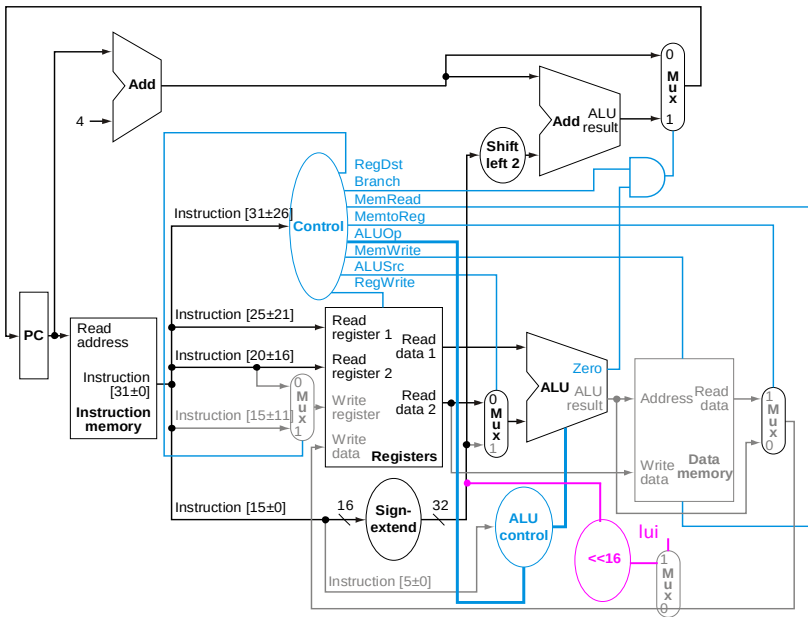
(b) (6 points) Find the clock cycles required in both cases.

$CC_{P1} = IC_{P1} * CPI_{P1}$ = 1 E6 * 3.1 = 3.1 E6 cycles, $CC_{P2} = IC_{P2} * CPI_{P2}$ = 1 E6 * 2.8 = 2.8 E6 cycles

11. (15 points) Add the `lui` (load upper immediate) instruction which uses the I format to the single-cycle datapath shown in the figure below. Add any necessary datapaths and control signals and show the necessary additions to the table of control signals given. An example `lui` instruction, its RTL, and the instruction fields are shown below.

```
lui   $t1, 22
$t1 ← 22 * 2^16
```

15	0	9	22



Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALU Op1	ALU Op0	lui
R-format	1	0	0	1	0	0	0	1	0	**0**
lw	0	1	1	1	1	0	0	0	0	**0**
sw	d	1	d	0	0	1	0	0	0	**0**
beq	d	0	d	0	0	0	1	0	1	**0**
lui	**0**	**d**	**d**	**1**	**d**	**0**	**0**	**d**	**d**	**1**

d – don't care

12. (20 points) Assume there is no forwarding in a five stage MIPS pipelined processor. Neglect pipeline fill.

(a) (10 points) Indicate hazards and add nop instructions to eliminate them.

```
(a)    or   $s0, $t2, $s1
(b)    lw   $s5, 0($s0)
(c)    and  $t1, $s5, $s0
(d)    sw   $t1, 0($s0)
```

Hazards: (a)-(b), (a)-(c), (a)d), (b)-(c), (c)-(d)

```
or   $s0, $t2, $s1
nop
nop
lw   $s5, 0($s0)
nop
nop
and  $t1, $s5, $s0
nop
nop
sw   $t1, 0($s0)
```

(b) (5 points) What is the total execution time of this instruction sequence with only ALU-ALU forwarding?

Cycle	IF	ID	EX	MEM	WB
	or $s0				
	lw $s5	or $s0			
	and $t1	lw $s5	or $s0		
	sw $t1	and $t1	lw $s5	or $s0	
1	sw $t1	and $t1	bubble	lw $s5	or $s0
2	sw $t1	and $t1	bubble	bubble	lw $s5
3		sw $t1	and $t1	bubble	bubble
4			sw $t1	and $t1	bubble
5				sw $t1	and $t1
6					sw $t1

ALU-ALU Forwarding Only: 6 cycles as indicated by the table (neglecting pipeline fill)

(c) (5 points) What is the speedup over a no-forwarding pipeline?

Cycle	IF	ID	EX	MEM	WB
	or $s0				
	nop	or $s0			
	nop	nop	or $s0		
	lw $s5	nop	nop	or $s0	
1	nop	lw $s5	nop	nop	or $s0
2	nop	a nop	lw $s5	nop	nop
3	and $t1	nop	nop	lw $s5	nop
4	nop	and $t1	nop	nop	lw $s5
5	nop	nop	and $t1	nop	nop
6	sw $t1	nop	nop	and $t1	nop
7		sw $t1	nop	nop	and $t1
8			sw $t1	nop	nop
9				sw $t1	nop
10					sw $t1

No Forwarding: 10 cycles (neglecting pipeline fill)

Speedup = $ET_{\text{No Forwarding}}/ET_{\text{ALU-ALU Forwarding}}$ = 10 cycles/6 cycles = 1.67