

The University of Alabama in Huntsville
Electrical & Computer Engineering Department
CPE 431 01
Final Exam
November 29, 2018

Name: _____

You must show your work to receive full credit!!

1. (1 point) _____ level parallelism utilizes multiple processors by running independent programs simultaneously.
2. (1 point) _____ multi-threading is a version of hardware multithreading that implies switching between threads only after significant events.
3. (1 point) A _____ is a synchronization device that allows only one processor to access data at a time.
4. (2 points) The two common data sharing mechanisms for multiprocessors are _____ and _____.
5. (8 points) What number does 0xC39B A000 0000 0000 represent, assuming the IEEE 754 double precision format? Express the answer in decimal.

6. (15 points) Here is a series of address references given as hexadecimal word addresses: 21, 4, 8, 5, 20, 37, 19, 5E, 209, 11, 4, 43, 5, 3E, 16, 59, 42, 30. Assuming a direct mapped cache with two word blocks, a total size of 16 words that is initially empty, (a) label each reference in the list as a hit or a miss and (b) show the entire history of the cache, including tag and data.

Word Address (Hexadecimal)	Word Address (Decimal)	Binary	Miss/Hit
0x21	33	0000 0000 0010 0001	
0x4	4	0000 0000 0000 0100	
0x8	8	0000 0000 0000 1000	
0x5	5	0000 0000 0000 0101	
0x20	32	0000 0000 0010 0000	
0x37	55	0000 0000 0011 0111	
0x19	25	0000 0000 0001 1001	
0x5E	94	0000 0000 0101 1110	
0x209	521	0000 0010 0000 1001	
0x11	17	0000 0000 0001 0001	
0x4	4	0000 0000 0000 0100	
0x43	67	0000 0000 0100 0011	
0x5	5	0000 0000 0000 0101	
0x3E	62	0000 0000 0011 1110	
0x18	8	0000 0000 0001 1000	
0x16	22	0000 0000 0001 0110	
0x59	89	0000 0000 0101 1001	
0x42	66	0000 0000 0100 0010	
0x30	48	0000 0000 0011 0000	

7. (9 points) Consider the following portions of three programs running at the same time on three processors in a symmetric multicore processor (SMP). Assume that before this code is run, the `int` variables `w`, `x`, `y`, `z`, are 4, 2, 2, 3, respectively. What are all the possible outcomes of executing these instructions?

Core 1: $y = 5 + w/z;$

Core 2: $x = (x * y) + w;$

Core 3: $z = w * (x - y) + z;$

8. (5 points) Assume that registers `$s0` and `$s1` hold the values `0xFFFF_FFFF` and `0xFFFF_F800`, respectively and that these values represent signed integers.
- (3 points) What is the value of `$t0` for the following assembly code?
`add $t0, $s0, $s1`
 - (2 points) Is the result in `$t0` the desired result, or has there been overflow?

9. (5 points) If the current value of the PC in a MIPS processor is $0 \times 0000_0600$, can you use a single branch instruction to get to the PC address $0 \times 2001_4924$? Explain your answer.

10. (8 points) Multilevel caching is an important technique to overcome the limited amount of space that a first level cache can provide while still maintaining its speed. Consider a processor with the following parameters.

Base CPI, no memory stalls	Processor speed	Main memory access time	First-level cache miss rate per instruction	Second-level cache, direct-mapped speed	Global miss rate with second-level cache, direct-mapped	Second-level cache, eight-way set associative speed	Global miss rate with second-level cache, eight-way set associative
1.5	2 GHz	100 ns	7 %	12 cycles	3.5 %	28 cycles	1.5 %

A designer wants to use the second level eight-way set associative cache and add a third level cache. The third level cache takes 40 cycles to access and will reduce the global miss rate to 0.9%. What is the CPI for the total system with the addition of this third level cache?

11. (6 points) The following list provides parameters of a virtual memory system.

Virtual Address (bits)	Physical DRAM Installed	Page Size	PTE Size (byte)
52	64 GiB	8 KiB	8

Using a multilevel page table can reduce the physical memory consumption of page tables, by only keeping active PTEs in physical memory.

- (a) (5 points) How many levels of page tables will be needed in this case?
(b) (1 point) how many memory references are needed for address translation if missing in TLB?

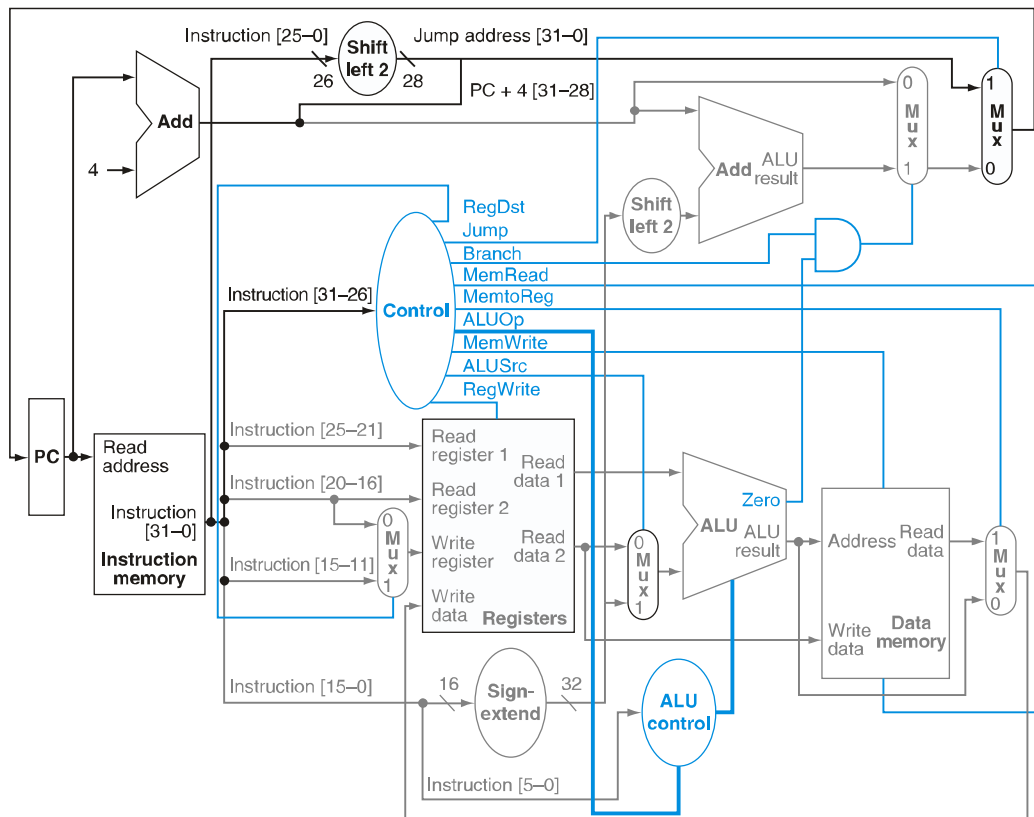
12. (4 points) Assume that individual stages of a MIPS datapath have the following latencies:

IF	ID	EX	MEM	WB
250 ps	350 ps	150 ps	400 ps	200 ps

- a. (3 points) What is the clock cycle time in a pipelined and non-pipelined processor?
b. (1 point) If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor?

13. (10 points) Add the instruction `jal` (jump and link) to the single-cycle datapath shown in the figure below. The `jal` instruction is a J-type instruction and its operation is defined below. Add any necessary datapaths and control signals and show the necessary additions to the table of control signals given.

`jal jump_address` $PC \leftarrow \text{jump_address}$
 $\$ra \leftarrow PC + 8$



Instruction	RegDst	ALUSrc	MemtoReg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUOp0	
R-format	1	0	0	1	0	0	0	1	0	
lw	0	1	1	1	1	0	0	0	0	
sw	d	1	d	0	0	1	0	0	0	
beq	d	0	d	0	0	0	1	0	1	

14. (10 points) Consider adding an addressing mode to MIPS that allows arithmetic instructions to directly access memory, as is found on the 80x86. The primary benefit is that fewer instructions will be executed because we won't have to first load a register. The primary disadvantage is that the cycle time will have to increase to account for the additional time to read memory. Consider adding a new instruction:

```
addm $t2, 100($t3) # $t2 = $t2 + Memory[$t3 + 100]
```

Assume that the new instruction will cause the cycle time to increase by 15 %. Use the instruction frequencies given, and assume that three-fifths of the data transfers are loads and the rest are stores. Assume that the new instruction affects only the clock speed, not the CPI. What percentage of loads must be eliminated for the machine with the new instruction to have at least the same performance?

Instruction Class	Frequency
Arithmetic	48 %
Data Transfer	33 %
Conditional branch	17 %
Jump	2 %

15. (15 points) (a) (5 points) Identify all of the data dependencies in the following code. (b) (10 points) How is each data dependency either handled or not handled by **forwarding from the EX/MEM pipeline register only**? Draw a multiple clock cycle style diagram to support your answer.

```
a    add    $5, $5, $4
b    lw     $4, 28($5)
c    add    $2, $4, $6
d    sw     $4, 100($5)
e    add    $3, $2, $7
```