The University of Alabama in Huntsville
Electrical & Computer Engineering Department
CPE 431 01
Test 1
September 29, 2009

Name: _____

1. (1 point) State one of the design principles: _____.
2. (1 point) A form of representation of an instruction composed of fields of binary numbers is an _____
3. (1 point) The program that instigates a procedure and provides the necessary parameter values is the _____ .
4. (1 point) The register that is reserved to point to the static area is called the _____.
5. (1 point) A systems program that places an object program in main memory so that it is ready to execute is a _____.
6. (10 points) For the following assembly code fragment, what is the total number of MIPS instructions executed?

```
      addi  $t1, $zero, 100
LOOP: lw    $s1, 0($s0)
      add   $s2, $s2, $s1
      addi  $s0, $s0, 4
      subi  $t1, $t1, 1
      bne   $t1, $zero, LOOP
```

7. (5 points) Show the IEEE 754 binary representation for the floating-point number 1.5_{ten} in single precision.

8. (20 points) Consider two different implementations, P1 and P2, of the same instruction set. There are five classes of instructions (A, B, C, D, and E) in the instruction set. P1 has a clock rate of 4GHz, and P2 has a clock rate of 6 GHz. The average number of cycles for each instruction class for P1 and P2 are listed in the following table

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Class	CPI on P1	CPI on P2
A	1	2
B	2	2
C	3	2
D	4	4
E	5	4

If the number of instructions executed in a certain program is divided equally among the classes of instructions except for class A, which occurs twice as often as each of the others, how much faster is P2 than P1?

9. (10 points) What IEEE 754 floating point number does the following bit pattern represent?

1100 1101 1001 0100 0000 0000 0000 0001

10. (10 points) The CPI of the different instruction types is given in the following table.

Arithmetic	Load/Store	Branch
1	10	4

Assume the following instruction breakdown given for executing a program.

	Instructions (in millions)
Arithmetic	500
Load/Store	300
Branch	100

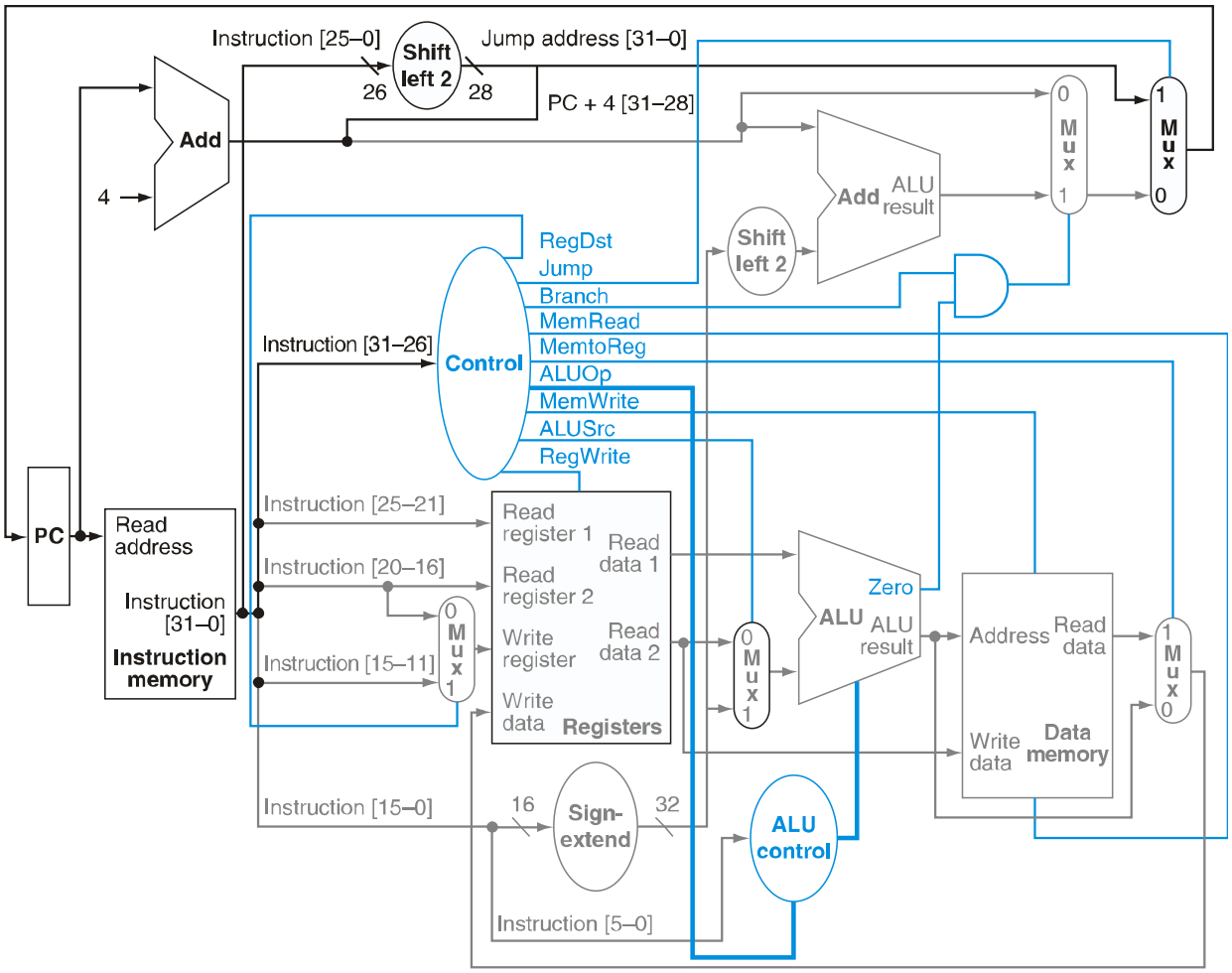
Suppose that we find a way to double the performance of arithmetic instructions? What is the overall speed-up of our machine?

11. (15 points) Assume that the logic blocks used to implement the datapath have the following latencies:

I-Mem	Add	Mux	ALU	Regs	D-Mem	Sign-Extend	Shift-left-2	ALU Ctrl
500 ps	150 ps	100 ps	180 ps	220 ps	1000 ps	90 ps	20 ps	55 ps

Further, assume that the time needed by the control unit to generate individual control signals is as follows:

RegDst	Jump	Branch	MemRead	MemtoReg	ALUOp	MemWrite	ALUsrc	RegWrite
720 ps	730 ps	600 ps	400 ps	700 ps	200 ps	710 ps	200 ps	800 ps



What is the clock cycle time of the processor?

12. (15 points) Assume that individual stages of the datapath have the following latencies:

IF	ID	EX	MEM	WB
200 ps	150 ps	120 ps	190 ps	140 ps

Instead of a single-cycle organization, we can use a multi-cycle organization where each instruction takes multiple cycles but one instruction finishes before another is fetched. In this organization, an instruction only goes through the stages it actually needs (e.g., sw only takes four cycles because it does not need the WB stage). What are the clock cycle times for a single-cycle organization, a multiple-cycle organization and a pipelined organization?

13. (10 points) For a color display using 16 bits for each of the primary colors (red, green, blue) per pixel and with a resolution of 1280 x 800 pixels, what should be the size (in bytes) of the frame buffer to store a frame? If a computer has a main memory of 8 GB, how many frames could it store, assuming the memory contains no other information?