The University of Alabama in Huntsville
ECE Department
CPE 431 01
Test 1
September 27, 2018

Name: _____

You *must* show your work to receive full credit: You may use additional sheets of paper for your work, please put your name on each additional sheet.
Remember: ET = IC*CPI*CT

1. (1 point) A _____ is a program specifically chosen to measure performance.

2. (1 point) A program that manages the resources of a computer for the benefit of the programs that run on that machine is a(n) _____.

3. (1 point) To specify a register choice from a register file with 256 registers requires _____ bits.

4. (1 point) Performance is _____ related to execution time.

5. (1 point) The address specified in a branch, which becomes the new program counter is the branch is taken, is known as the _____ address.

6. (15 points) Translate the following C code to MIPS. Assume that the variables `f`, `g`, `h`, `i`, and `j` are given and are assigned to registers `$s0`, `$s1`, `$s2`, `$s3`, and `$s4`, respectively. Assume that the base address of the arrays A and B are in registers `$s6` and `$s7`, respectively. Assume that the elements of the arrays A and B are 4-byte words:

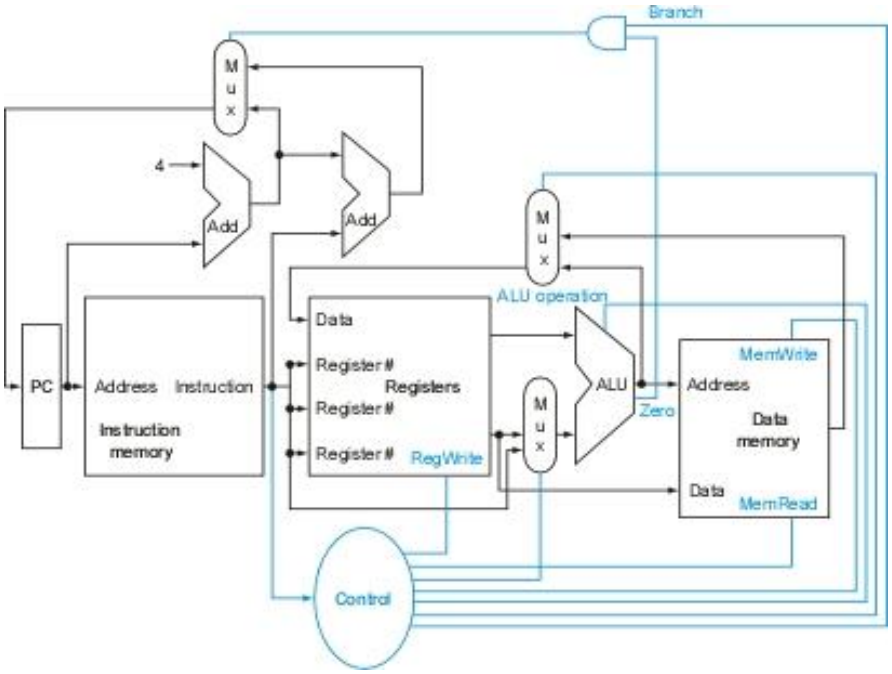
```
B[i] = A[A[j]]
```

7. (15 points) MIPS chooses to simplify the structure of its instructions. The way we implement complex instructions is to decompose such complex instructions into multiple simpler MIPS ones. The complex instruction `swap $rs, $rt` can be decomposed into three instructions. If the implementation of the swap instruction in hardware will increase the clock period of a single-cycle implementation by 10%, what percentage of `swap` operations in the instruction mix would recommend implementing it in hardware?

8. (10 points) Write down the hexadecimal representation of the decimal number 3967.4453125 in the IEEE 754 double precision format.

9. (25 points) When processor designers consider a possible improvement to the processor datapath, the decision usually depends on the cost/performance trade-off. three problems, assume that we are starting with a datapath from Figure 4.2, where I-Mem, Add, Mux, ALU, Regs, D-Mem, and Control blocks have latencies of 420 ps, 90 ps, 25 ps, 130 ps, 200 ps, 380 ps, and 500 ps, respectively, and costs of 1000, 30, 10, 100, 200, 2000, and 500, respectively. Consider the addition of a multiplier to the ALU. This addition will add 300 ps to the latency of the ALU and will add a cost of 600 to the ALU. The result will be 5% fewer instructions executed since we will no longer need to emulate the MUL instruction.

(a) (15 points) What is the clock cycle time with and without this improvement?



(b) (10 points) What is the ratio of cost/performance after the improvement to the cost/performance before the improvement?

10. (5 points) For a pipeline with m stages, how many cycles does it take to execute n instructions?

11. (10 points) What number does 0xF43B 0000 represent as an IEEE 754 floating point number?

12. (15 points) We wish to add a variant of the `lw` (load word) instruction, which increments the index register after loading word from memory. This instruction (`l_inc`) corresponds to the following two instructions:

```
lw    $rs, L($rt)
addi  $rt, $rt, 1
```

Explain whether it is possible to implement `l_inc` without making any changes to the register file of the single-cycle datapath. If it is not possible, describe the changes that must be made to the register file.