The University of Alabama in Huntsville
ECE Department
CPE 431 01
Test 1
October 4, 2016

Name: _____

You *must* show your work to receive full credit: You may use additional sheets of paper for your work, please put your name on each additional sheet.
Remember: ET = IC*CPI*CT

1. (1 point) _____ states that the performance enhancement possible with a given improvement is limited by the amount that the improved feature is used.

2. (1 point) The layout of the instruction is called the _____.

3. (1 point) _____ are programs specifically chosen to measure performance.

4. (1 point) A _____ is a link to the calling site that allows a procedure to return to the proper address; in MIPS it is stored in register `$ra`.

5. (1 point) _____ occurs when a number can't be represented in a computer.

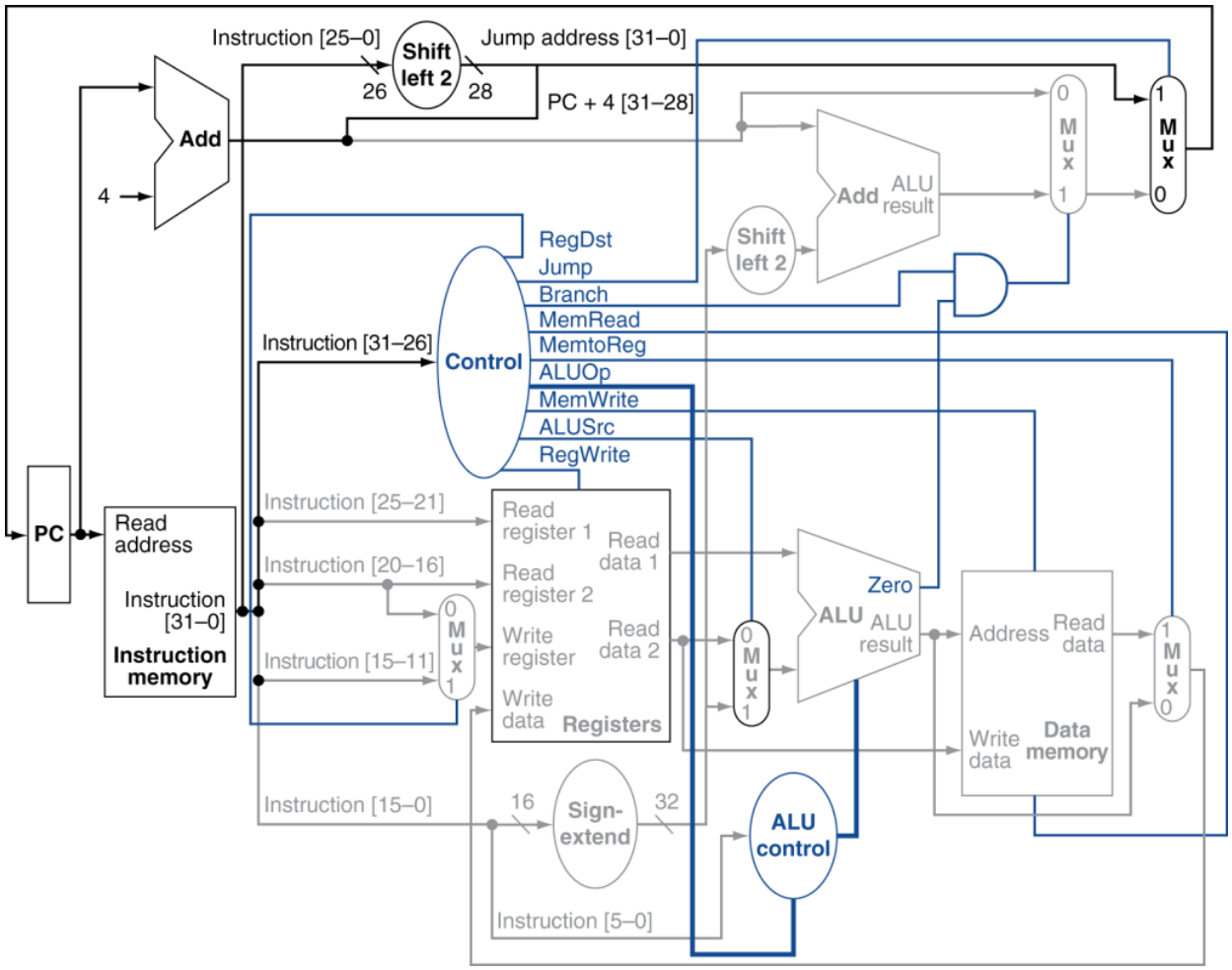
6. (10 points) MIPS chooses to simplify the structure of its instructions. It implements complex instructions by decomposing them into multiple simpler MIPS ones. The complex instruction `swap $rs, $rt` can be decomposed into three instructions. If the implementation of the swap instruction in hardware will increase the clock period of a single-cycle implementation by 10%, what percentage of swap operations in the instruction mix would recommend implementing it in hardware?

7. (15 points) Translate the following C code to MIPS. Assume that the variables `f`, `g`, `h`, `i` and `j` are given and are assigned to registers `$s0`, `$s1`, `$s2`, `$s3`, and `$s4`, respectively. Assume that the base address of the arrays A and B are in registers `$s6` and `$s7`, respectively. Assume that the elements of the arrays A and B are 4-byte words:

```
B[8] = A[i + j]
```

8. (15 points) Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes of instructions according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.75 GHz and CPIS of 1, 2, 2, and 3, and P2 with a clock rate of 3 GHz and CPIS of 1, 1, 2, and 3.
   (a) Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 15% class A, 20% class B, 45% class C, and 20% class D, which implementation is faster?
   (b) What clock rate must be achieved by the slower processor to make it as fast as the other with no other changes?

9. (15 points) Add the instruction `slt` to the single-cycle datapath shown in the figure below. Add any necessary datapaths and control signals and show the necessary additions to the table of control signals given.



Instruction	RegDst	ALUSrc	Memto Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUOp0	
R-format	1	0	0	1	0	0	0	1	0	
lw	0	1	1	1	1	0	0	0	0	
sw	d	1	d	0	0	1	0	0	0	
beq	d	0	d	0	0	0	1	0	1	

d-don’t care

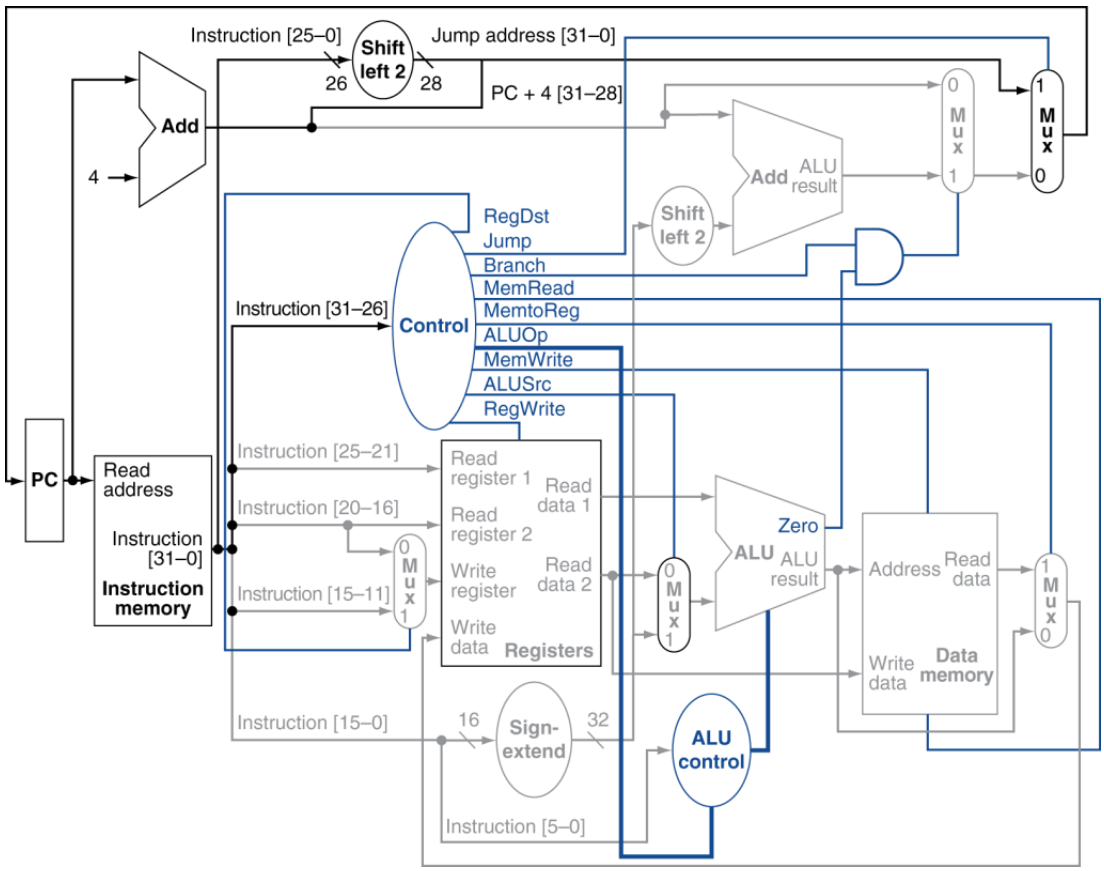
10. (10 points) A MIPS processor fetches the following instruction word:

`0000 0000 0000 0010 0000 1010 1000 0000`

Assume that data memory is all zeros and that the processor's registers have the following values at the beginning of the cycle in which the above instruction word is fetched.

r0	r1	r2	r3	r4	r5	r6	r8	r12	r31
0	-1	2	-3	-4	10	6	8	2	-16

What instruction is this and what is the output of the sign-extend for this instruction word?



11. (20 points) In this exercise, we assume that the following MIPS code is executed on a pipelined processor with a 5-stage pipeline, full forwarding, and a predict-taken branch predictor. Draw the pipeline execution diagram for this code, assuming there are no delay slots and that branches execute in the EX stage.

```
         add   $t1, $t1, $t0
         lw    $t2, 0($t1)
label1:  beq   $t2, $zero, label2    # not taken once, then taken
         lw    $t3, 0($t2)
         sw    $t3, 0($t1)
         beq   $t3, $zero, label1    # taken
         add   $t1, $t3, $t1
label2:  sw    $t1, 0($t2)
```

Cycle	IF	ID	EX	MEM	WB
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					
21					

12. (10 points) Write down the hexadecimal representation of the decimal number 1297.71875 assuming the IEEE 754 single precision format.