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## Upgrade of the ALICE muon trigger electronics

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**ABSTRACT:** The ALICE muon trigger is a large scale detector based on single gap bakelite RPCs. An upgrade of the electronics is needed in order to withstand the increase of luminosity after the LHC Long Shutdown-2 in 2018-2019. The detector will be read out at the minimum bias rate of 100 kHz in Pb–Pb collisions (including a safety factor of 2), two orders of magnitude above the present design. For the most exposed RPCs and in the present conditions of operation, the total integrated charge could be as high as 100 mC/cm<sup>2</sup> with rates up to 100 Hz/cm<sup>2</sup>, which is above the present limit for safe operation. In order to overcome these limitations, upgrade projects of the Front-End (FE) and Readout Electronics are scheduled. The readout upgrade at high rate with low dead time requires changing most of the present electronics. It involves a new design for the 234 Local cards receiving the LVDS signals from the FE electronics and the 16 Regional concentrator cards. The readout chain is completed by a single Common Readout Unit developed for most ALICE sub-detectors. The new architecture of the muon trigger readout will be briefly presented. The present FE electronics, designed for the streamer mode, must be replaced to prevent ageing of the RPCs in the future operating conditions. The new FE called FEERIC (for Front-End Electronics Rapid Integrated Circuit) will have to perform amplification of the analog input signals. This will allow for RPC operation in a low-gain avalanche mode, with a much smaller charge deposit (factor 3-5) in the detector as compared to the present conditions. The purpose is to discriminate RPC signals with a charge threshold around 100 fC, in both polarities, and with a time jitter below 1 ns. We will describe the FE card and FEERIC ASIC features and first prototype performance, report on test results obtained on a cosmic test bench and discuss ongoing developments.

**KEYWORDS:** Front-end electronics for detector readout; Resistive-plate chambers; Trigger detectors

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## 1 ALICE muon trigger upgrade

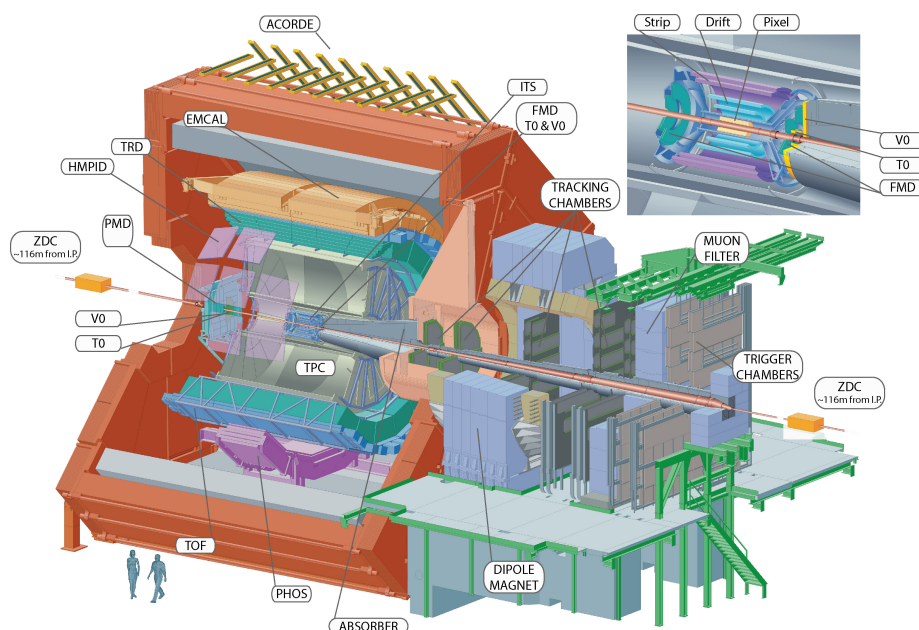
### 1.1 ALICE upgrade strategy

ALICE (A Large Ion Collider Experiment) is the only detector dedicated to heavy ion collisions at the CERN LHC. It is designed to investigate high-density, high-temperature strongly interacting matter, and the transition to Quark-Gluon Plasma (QGP) [1].

The ALICE collaboration plans a major upgrade of the detector during the LHC Long Shutdown 2 (LS2), which is at present foreseen to start in summer 2018. The scientific goals of this upgrade together with a basic description of the detector upgrade plans can be found in a Letter of Intent (LoI) [2], that was endorsed by the LHCC in September 2012.

The present ALICE detector is shown in figure 1. A detailed description of the detector can be found in [3] and its performance is summarised in [4]. ALICE will collect  $1 \text{ nb}^{-1}$  Pb–Pb collision data for a total integrated luminosity of  $1 \text{ nb}^{-1}$  before LS2, at peak luminosities of  $L=10^{27} \text{ cm}^{-2}\text{s}^{-1}$ , corresponding to a collision rate of 8 kHz. Hardware triggers based on event multiplicity, calorimeter energy and track  $p_T$  provide event selectivity that allows sampling of the full luminosity. The maximum readout rate of the present ALICE detector is limited to about 500 Hz of Pb–Pb events.

The physics objective of the upgrade aimed at precision measurements of the QGP properties, which will be accessible essentially through measurements of heavy-flavour transport parameters, quarkonia down to zero  $p_T$  and low mass di-leptons. Since these processes do not exhibit signatures



**Figure 1.** 3D ALICE schematic

that can be selected efficiently by hardware triggers, all events fulfilling a zero-bias (minimum bias) trigger condition will be collected.

The ALICE upgrade strategy is therefore based on collecting more than  $10 \text{ nb}^{-1}$  of Pb–Pb collisions at luminosities up to  $L = 6.10^{27} \text{ cm}^{-2}\text{s}^{-1}$  corresponding to collision rates of 50 kHz, where each collision is shipped to the online systems, either upon a minimum bias trigger or in a self-triggered or continuous fashion. The LoI considers in addition the collection of  $6 \text{ pb}^{-1}$  of pp collisions at the equivalent Pb–Pb nucleon energy as well as  $50 \text{ nb}^{-1}$  of p–Pb collisions, both at a levelled collision rate of 200 kHz.

The ALICE upgrade consists mostly in replacing the present Inner Tracking System, the Time Projection Chamber detectors and in upgrading the ALICE sub-detector electronics to read out 50 kHz Pb–Pb collision data at the rate of 50 kHz, as well as implementing a new online system that is capable of receiving and processing the full detector information.

The upgrade plan relative to the project discussed here is detailed in the Technical Design Report for the Upgrade of the ALICE Readout and Trigger System [5].

## 1.2 Muon trigger upgrade

Heavy quarkonia (from  $J/\psi$  and  $\Upsilon$  family) and open heavy-flavour particles (charm and bottom quarks) are sensitive probes of the QGP. Their muonic decays are measured in the forward muon spectrometer. The spectrometer is equipped with a muon tracker composed of cathode pad chambers, a dipole magnet, various absorbers and a muon trigger (MTR) based on Resistive Plate Chambers (RPC).

The MTR detector is currently providing the selection of high  $p_T$  single muon and di-muon events. The upgrade trigger strategy does not require a muon trigger anymore since all events will be read upon the interaction trigger before online selections. Consequently the current MTR

**Table 1.** Expected counting rates of the RPCs.

collision type	pp	Pb–Pb
collision rate (kHz)	200	100
$\sqrt{s_{NN}}$ (TeV)	14	5.5
mean–peak hits/s/cm <sup>2</sup>	6 - 15	75 - 125

detector will become a muon identifier in the context of the upgrade. Still, the present muon trigger detector will play a crucial role as the muon identifier, since the large ( $\approx 15\%$ ) contamination of hadron tracks reconstructed by the tracking system can only be removed by requiring tracks to have hits in the trigger chambers, which are located downstream of a 7 interaction lengths iron wall (figure 1).

The MTR is composed of 4 planes of 2 mm single gap bakelite RPC detectors, organized in two stations of two planes located at 16 m and 17 m from the interaction point. The total detection area is about 140 m<sup>2</sup>. The RPC signals are collected by means of a total of 21000 strips, each of them being connected to a Front-End (FE) electronics channel. The signals from the FE electronics are propagated to the 234 Local cards, acting as the readout interface and in charge of the first stage of the trigger decision. Readout is performed by two readout cards interfaced to the Local cards by means of 16 Regional cards. The muon trigger detector performance during LHC Run I is discussed in [6].

As explained above, it has been decided to read the muon spectrometer for each minimum bias trigger with the goal of maximizing the muon physics potential. The readout rate will be more than one order of magnitude larger than that of the initial design. This requires the replacement of all muon trigger readout electronics, including Local, Regional and readout cards.

The FE Electronics must also be replaced with the motivation of slowing down the ageing of the RPCs. The present FE chip called ADULT [7] will be replaced by a new ASIC, FEERIC (Front-End Electronics Rapid Integrated Circuit). Unlike ADULT, FEERIC will perform amplification of the analog signals from the RPCs. The RPCs will be operated in “genuine” avalanche mode (like in ATLAS [8] and CMS [9]) with a significant reduction of the charge produced in the gas, hence limiting ageing effects. The target is to operate the new FE with a threshold corresponding to a fast charge  $q \approx 100$  fC. Preliminary estimates show that the total charge per pulse should be decreased to  $Q \approx 10\text{--}30$  pC (vs.  $Q \approx 100$  pC with ADULT). The RPC ageing should consequently be slowed down by a factor estimated between 3 and 5, while the maximum counting rate capability is expected to increase from 50 Hz/cm<sup>2</sup> to 200 Hz/cm<sup>2</sup>, which is above expectations (table 1).

## 2 ASIC development

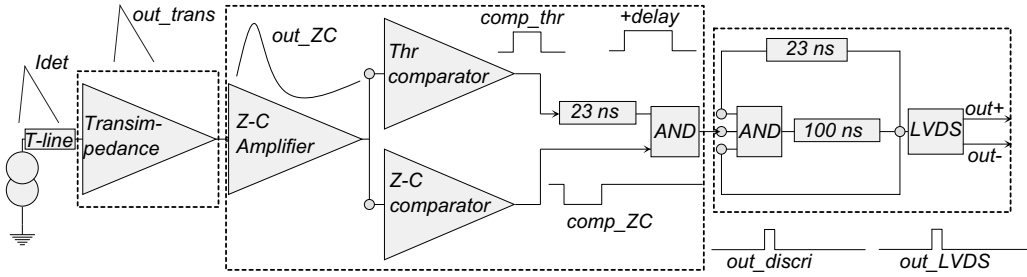
### 2.1 Requirements

The FE electronics is located on the RPC detectors. The requirements for the FE ASIC are listed in table 2. Since there is no existing ASIC with all the requested characteristics, the development of a new ASIC was required.

A first prototype was developed in 2012–2013 and tested in October 2013. A second prototype was developed late 2013 and tested in May 2014.

**Table 2.** Requirements of the FE ASIC.

feature	value or type
pulse polarity	positive or negative
# of channels	8
power consumption / channel	< 100 mW
input impedance	< 50 $\Omega$
dynamic range	20 fC < $q$ < 3 pC
time resolution	< 1 ns
time walk	< 2 ns
one-shot	100 ns
output format	LVDS
signal shape	square pulse $23 \pm 3$ ns

**Figure 2.** FEERIC Single Channel Block Diagram.

## 2.2 FE ASIC design

FEERIC is an 8-channel ASIC designed in the AMS 0.35  $\mu\text{m}$  CMOS technology, which is low-cost and robust. The functional single-channel block-diagram of FEERIC is represented in figure 2.

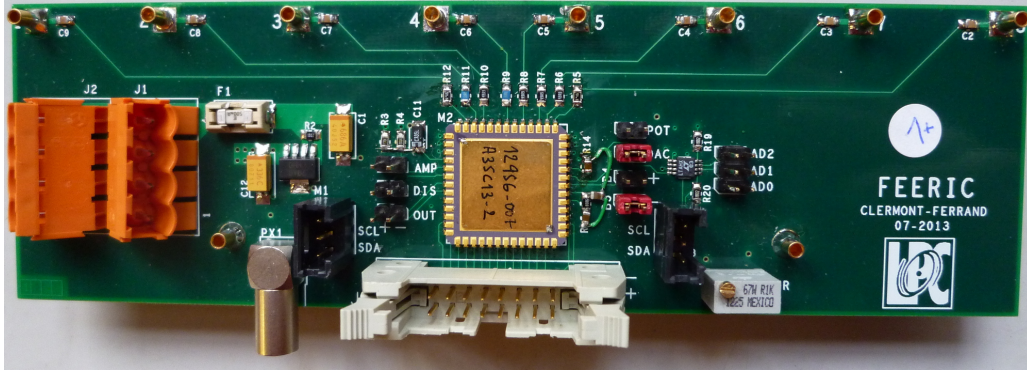
It is composed of a transimpedance amplifier stage, a zero-crossing discriminator to limit time walk effects, and a one-shot which prevents retriggering during 100 ns. The design is discussed in more detail in [10]. The design and simulations were done using the Cadence<sup>®</sup> package.

### 2.2.1 Amplifier

The amplifier stage is realized using an operational transconductance amplifier with a feedback loop including a resistor (which sets the gain) in parallel with a capacitor (for stability). The RC time constant is 500 ps, which is lower than the charge collection time (a few ns). The input impedance is low, so a resistor must be added in series in the board for impedance matching. With these characteristics, the amplifier stage is functionally a transimpedance amplifier. A challenging requirement is the low noise level at the amplifier output. The main sources of intrinsic noise are the two input transistors of the differential pair. Their size and biasing current have been tuned in order to match the requirements.

The gain was set in simulation to 0.4 mV/fC in version 1 and 1 mV/fC in version 2 to fulfill the requirements of dynamic range and bandwidth (which impacts timing precision). The intrinsic noise level is evaluated to 1 fC rms (equivalent noise charge). The input capacitance was set to





**Figure 3.** FEERIC-proto1 board.

10 pF in simulation, to account for electrical parasitics (chip and board pads, PCB tracks). The RPC strips behave like a transmission line and thus are not considered to contribute directly to this input capacitance.

### 2.2.2 Zero-crossing discriminator

The time response is affected by 2 dispersion factors: a random component (jitter) and a deviation related to the pulse amplitude (walk).

The principle of the zero-crossing discriminator is to minimize the walk component by using an amplitude-independent time reference (while keeping the jitter as low as possible with low noise and fast slope). This is implemented by a differentiating shaper which transforms the amplifier output into a bipolar signal that crosses the baseline at a time corresponding to the peak of the amplifier output signal. This time is not expected to vary with charge, as long as the amplifiers are in linear regime. The shaping stage is an operational amplifier with differentiating RC feedback loop.

It is followed by 2 comparators, one for time reference with a threshold equal to the baseline, the other for amplitude selection. The output of the zero-crossing discriminator is a logical "and" between the zero-crossing comparator output and the threshold comparator output with extended duration to have a sufficient overlap of the two logic pulses. This structure ensures that the output signal occurs at a time determined only by the zero-crossing discriminator.

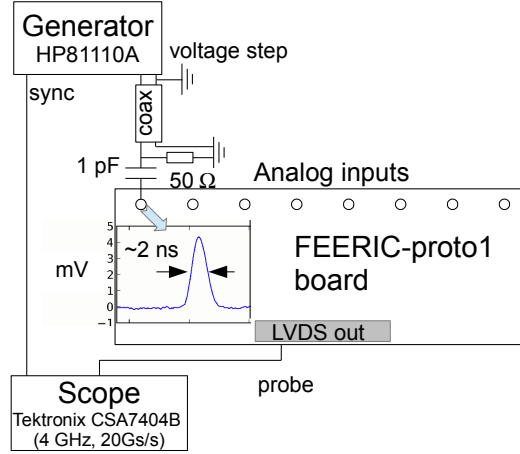
### 2.2.3 One-shot and LVDS driver

The one-shot is implemented by a logic gate and delays to set the output width to 23 ns while preventing any retriggering during 100 ns. It is followed by a LVDS output stage which drives  $\pm 3.5$  mA into a 100  $\Omega$  differential line.

## 3 Prototype FE board and test results

### 3.1 Board description

The prototype FE board, called FEERIC-proto1 (figure 3), supports one FEERIC ASIC (8 channels) and its environment (linear regulators, voltage levels, configuration). It has the same dimension as the present FE boards installed on RPCs in ALICE cavern.



**Figure 4.** Test setup.

The board is powered by a 0/+3.5 V supply. The inputs of FEERIC are AC coupled to the strips (via  $C=100$  nF) and the impedance is approximately matched to the strips thanks to  $50\ \Omega$  series resistors, while the input impedance of FEERIC is low by design.

Jumper switches are used to set manually polarity and board address.

The discriminator threshold can be set by means of a Digital to Analog Converter (DAC) controlled via a serial bus ( $I^2C$ ). Up to 8 boards can be chained on the same bus line. The bus requires only 3 conductor lines, which allows to reuse the connectors and cables of the current analog threshold distribution.

### 3.2 Tests

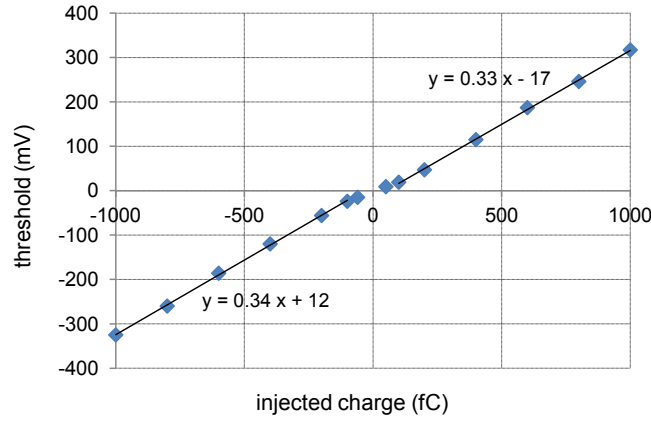
A test setup (figure 4) was used to characterize the amplification gain and timing performance of FEERIC. In order to inject short impulsive signals with controlled charge on the inputs, an injector board was made, which connects the input pins to a coaxial LEMO connector via 1 pF capacitors. A pulse generator is connected to the injector board via a coaxial LEMO cable (adapted on both nodes). When a voltage step  $\Delta V$  is applied to the injector board, the current through the 1 pF capacitor is a pulse signal with charge  $Q = C\Delta V$  and duration equal to the rise time of the voltage step, which is about 2 ns.

The board-level power consumption per channel is 70 mW with a 3.5 V power supply. Figure 5 shows the relation between the injected charge and the maximal threshold to ensure triggering. The gain is 0.33 mV/fC in test (from linear regressions in the positive and negative domains) and 0.4 mV/fC in simulation. The constant terms in the linear regressions are compatible with the noise threshold.

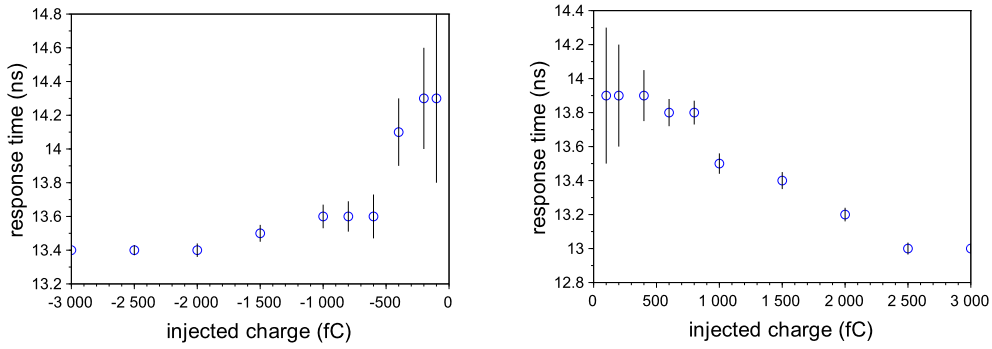
The noise level at the amplifier output is 2 mV RMS (corresponding to 6 fC). The difference with the simulated noise of 1 fC is probably due to a contribution of the board and its environment. The minimal threshold to eliminate random triggerings is 8 mV (24 fC), which is quite satisfactory. When the input is connected to the injection setup, the threshold above noise reaches 15-18 mV (45-54 fC).

The cross-talk is less than 2% for an input charge of  $\pm 3.5$  pC and a threshold of  $\pm 20$  mV.





**Figure 5.** Gain linearity: threshold vs. pulse charge.



**Figure 6.** Timing: response time vs. pulse charge for negative (left) and positive charge (right).

The timing performance was characterized by measuring the response time (mean and standard deviation) for several values of injected charge and a fixed threshold of  $\pm 20$  mV (60 fC). The results are shown in figure 6 for both polarities. The error bars indicate the time jitter, while the variation of the mean response time with injected charge is the time walk. The jitter is  $< 500$  ps (rms) for  $q > 100$  fC, and the time walk is 900 ps for  $100 \text{ fC} < q < 3000 \text{ fC}$ .

As a summary, table 3 compares the main required and measured performance. Tests on RPCs of FEERIC-proto1 boards are ongoing on a cosmic bench in order to quantify the performance relative to efficiency, cluster size and resolution.

### 3.3 Second version of ASIC and board

A second version called FEERIC-proto2 with a larger gain (1 mV/fC) and improved layout of the ASIC and board was designed. The purpose is to install and test FEERIC-proto2 cards on one RPC in ALICE cavern during LHC run 2 (expected to start early 2015). The ASIC was submitted in December 2013 to foundry, and the board was produced in April 2014.

The board layout is divided in 3 areas: inputs, analog and logic circuits to minimize the noise on FEERIC inputs.

**Table 3.** Requirements and performance of FEERIC-proto1 (ASIC and board). The time performance is given for  $q > 100$  fC because the signal to noise ratio in our test environment is too low for significant time performance measurement for lower charges.

figure	required	measured
power consumption (mW)	$< 100$	70
amplification (mV/fC)	0.4	0.33
time jitter (rms) for $q > 100$ fC	$< 1\text{ ns}$	$< 500\text{ ps}$
time walk for $100\text{ fC} < q < 3000\text{ fC}$	$< 2\text{ ns}$	900 ps

The board also includes:

- a pulse injector circuit for functional verification during operation,
- variable delays on the LVDS logic outputs to compensate for different cable lengths from FE to Local cards,
- an I<sup>2</sup>C bus interface enabling to chain up to 32 boards on the same bus line.

This version is currently (May 2014) under functional testing.

## 4 Conclusion

A vast upgrade program of the ALICE detector is ongoing. In this context, the readout and Front-End Electronics of the muon trigger will be replaced. The new Front-End, FEERIC, should slow down ageing of the RPCs by performing amplification of the analog input signal, thus limiting the RPC operating voltage.

FEERIC, an 8-channel FE ASIC for the ALICE muon trigger RPCs, has been designed in the AMS 0.35  $\mu\text{m}$  CMOS technology. The first prototype board with FEERIC features a global power consumption per channel of 70 mW for 3.5 V power supply, a gain of 0.33 mV/fC and a time resolution better than 500 ps rms (for an input charge of  $\pm 100$  fC). The performance exceeds the requirements for operation in ALICE. A second prototype with higher gain is currently under test. The board is designed to operate on a RPC in ALICE cavern during LHC run 2 (2015) for long-term testing.

## Acknowledgments

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