

# Readout Chain Muon Identifier

*Readout architecture, functionalities and prototypes*

## ALICE MUON MEETING 2017

*Grotta Giusti, Tuscany, Italy 15 May 2017*

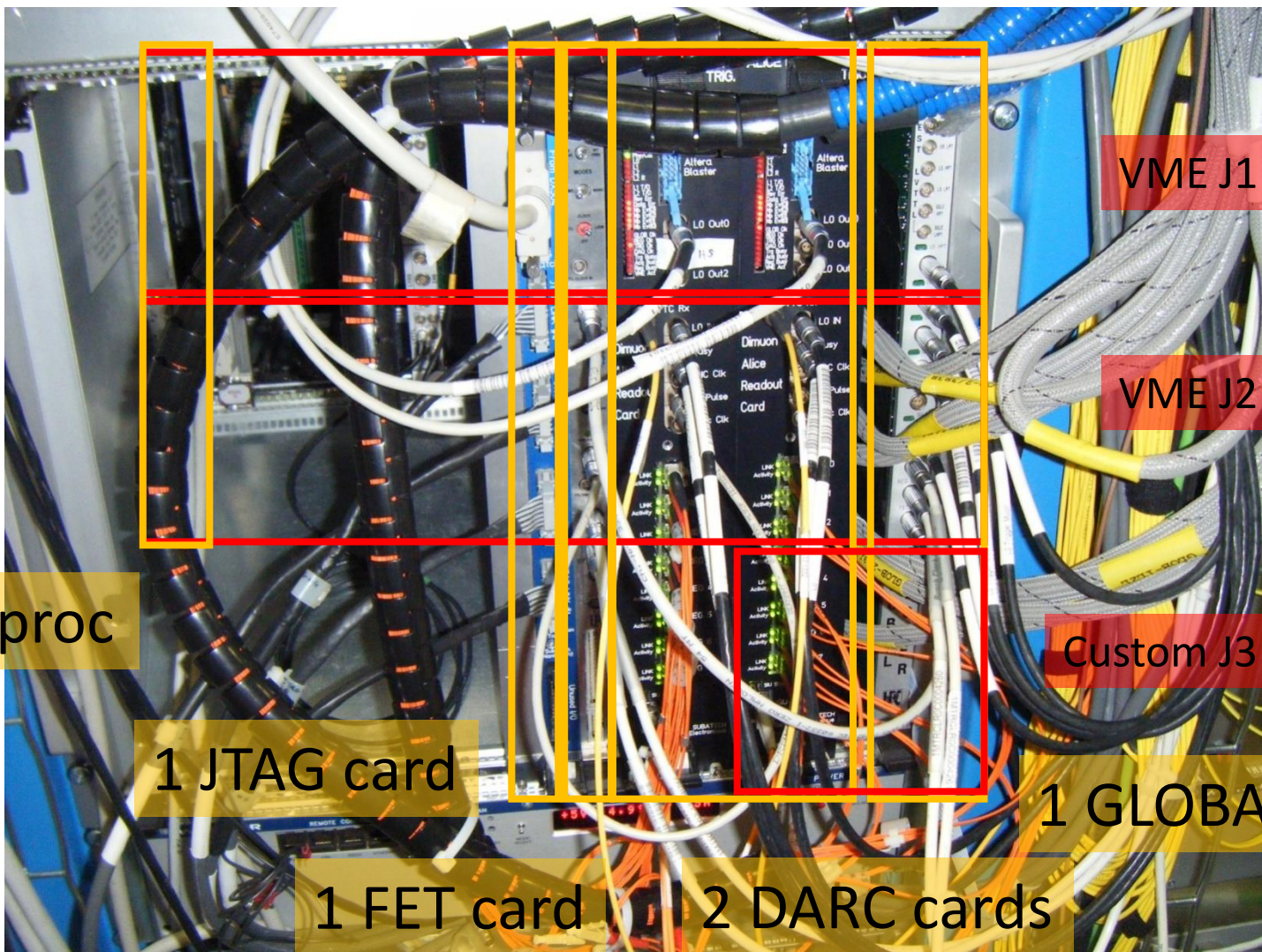
# Readout Chain Muon Identifier

*Readout architecture, functionalities and prototypes*

## Architecture

# Readout Chain Muon Identifier

*Actual Muon Trigger readout chain (1/3)*



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15-May-2017 v2

J.-L. Béney, S. Martinez, P. Pichot, Ch. Renard, Alice-Muon-Trigger-Upgrade  
<http://www-subatech.in2p3.fr/~electro/projets/alice/dimuon/trigger/upgrade/>

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# Readout Chain Muon Identifier

*Actual Muon Trigger readout chain (2/3)*



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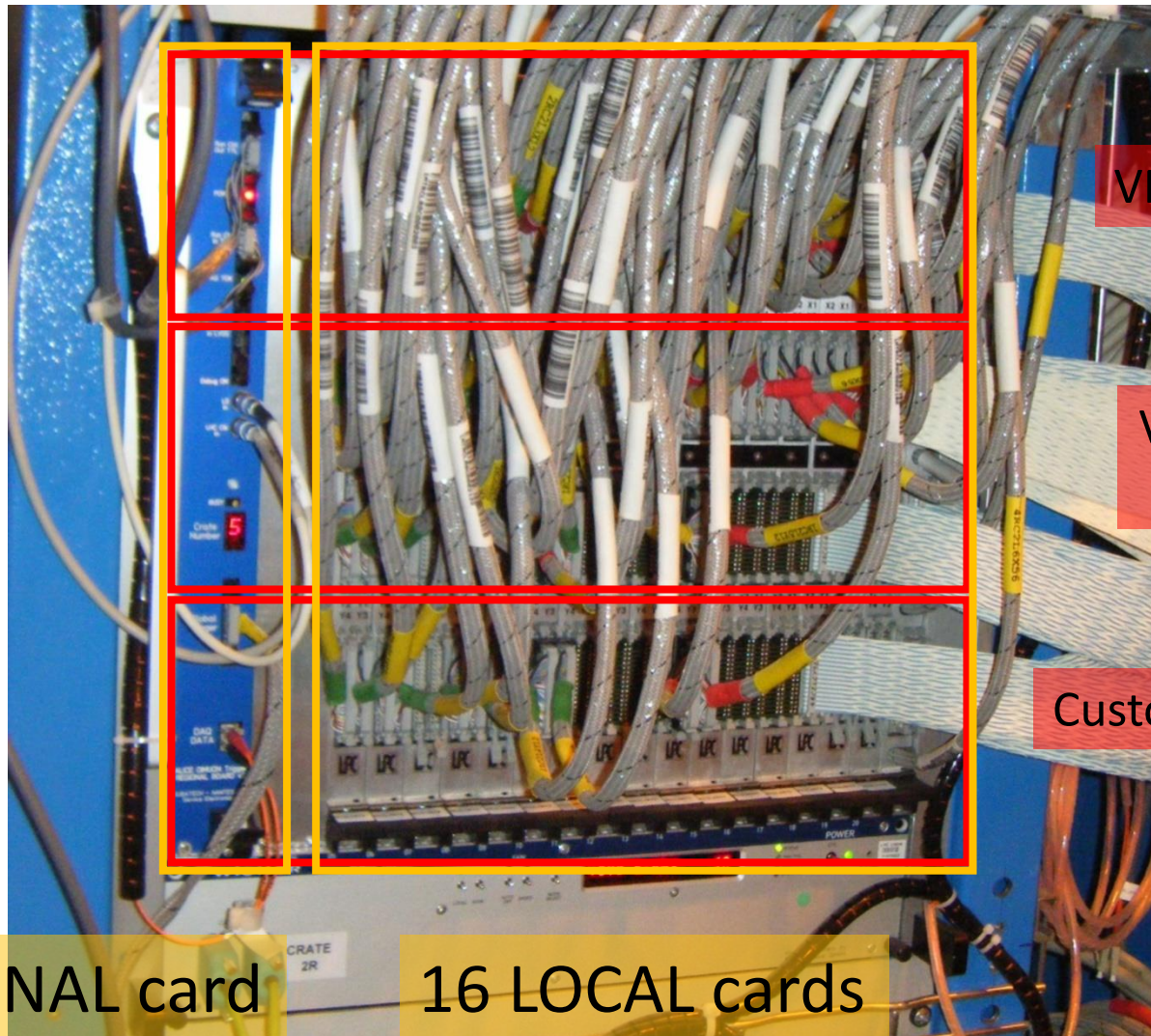
J.-L. Béney, S. Martinez, P. Pichot, Ch. Renard, Alice-Muon-Trigger-Upgrade  
<http://www-subatech.in2p3.fr/~electro/projets/alice/dimuon/trigger/upgrade/>

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# Readout Chain Muon Identifier

*Actual Muon Trigger readout chain (3/3)*



VME J1 backplane

VME J2 + custom  
backplane

Custom J3 backplane

1 REGIONAL card

16 LOCAL cards

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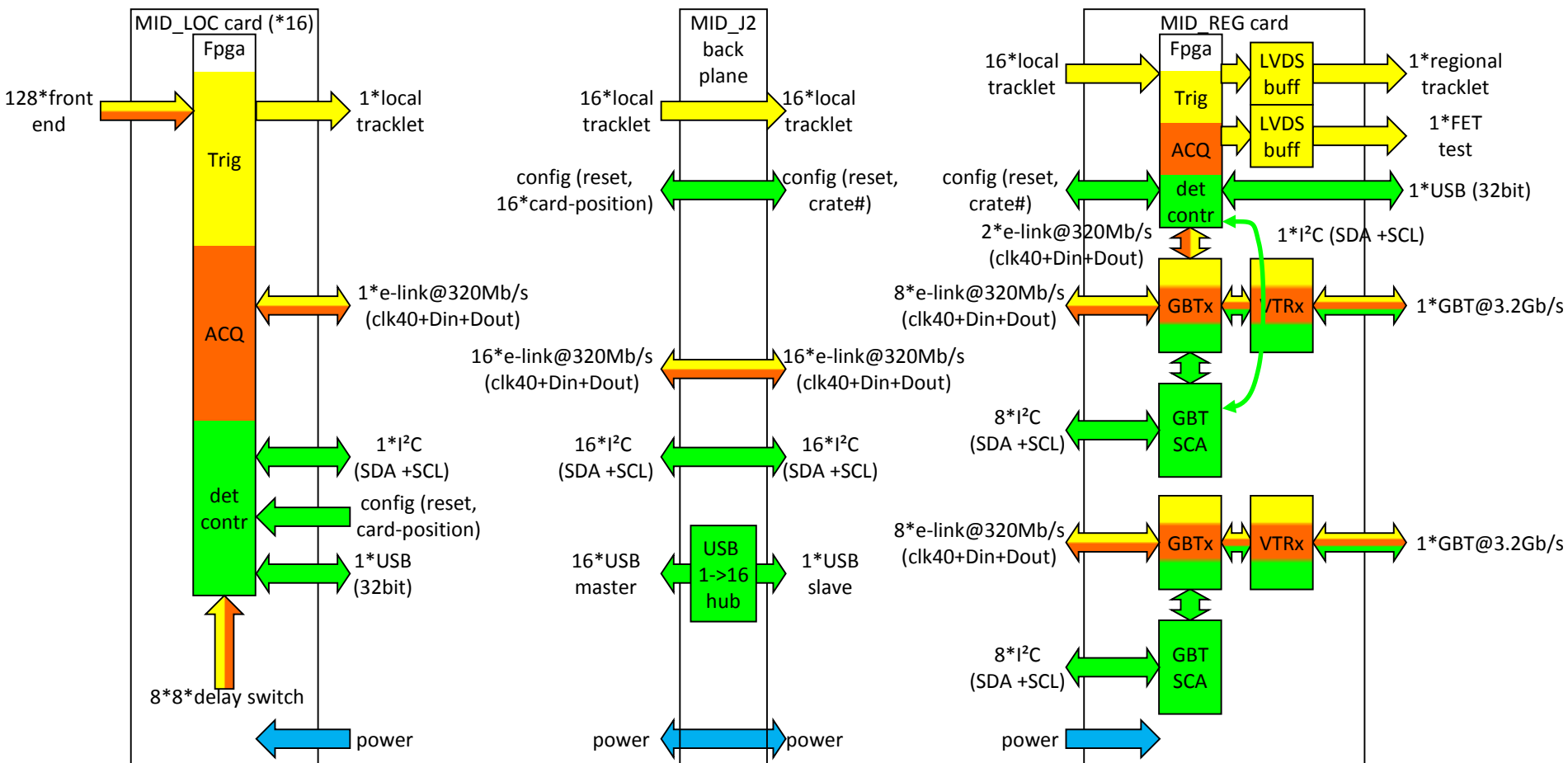
J.-L. Béney, S. Martinez, P. Pichot, Ch. Renard, Alice-Muon-Trigger-Upgrade  
<http://www-subatech.in2p3.fr/~electro/projets/alice/dimuon/trigger/upgrade/>

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# Readout Chain Muon Identifier

*REGIONAL crate upgrade (EDR on 16 June 2015)*



LOCAL with 128 LVDS inputs, 1 e-link@320Mb/s (clock@40MHz), 1 I<sup>2</sup>C, 1 FPGA, 1 LVDS output, 1 LHC-clock, 8x8 delay switch, power, config, USB3.0

J2 with 16 LVDS lines, 16 e-link@320Mb/s, REGIONAL with 16 LVDS inputs, 16 e-link@320Mb/s (clock@40MHz), 2 GBTx, 2 GBT-SCA, 2 GBT links @3.2Gb/s, 1 FPGA, 1 LVDS output, power, config, USB3.0, 1-to-2 USB3.0 hub

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## *MID data flow (continuous readout)*

*Slide from Pascal Dupieux LPC-Clermont*

- ❑ RPC counting rate (hence data flow) dominated by single background hits

Pb-Pb $\sqrt{s}=5.5$ TeV, <b>100 kHz</b>		p-p $\sqrt{s}=14$ TeV, 200 kHz	
RPC counting rate (mean)	RPC counting rate (peak)	RPC counting rate (mean)	RPC counting rate (peak)
<b>75 Hit/s/cm<sup>2</sup></b>	<b>125 Hit/s/cm<sup>2</sup></b>	6 Hit/s/cm <sup>2</sup>	15 Hit/s/cm <sup>2</sup>

- ❑ Re-evaluation (2016) of the data flow : thesis of Victor Feuillard
    - Takes into account the data format proposed for MID
    - Based on real data : Pb-Pb 2015@5TeV and p-p 2016@13 TeV
    - Makes use of the dead-time free scalers registered continuously during the runs
- => **available bandwidth sufficient with large safety margins at all levels**

Pb-Pb $\sqrt{s}=5.5$ TeV, <b>100 kHz</b>		p-p $\sqrt{s}=14$ TeV, 200 kHz
Total data flow to CRU	Mean (max.) data flow per link Local-Regional	Total data flow to CRU
<b>3 Gbit/s</b> (100 Gbit/s available)	<b>8 (20) Mbit/s</b> (320 Mbit/s available)	<b>0,3 Gbit/s</b>

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# Readout Chain Muon Identifier

*Readout architecture, functionalities and prototypes*

## Functionalities



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*REGIONAL crate upgrade (heartbeat<sup>[1][2]</sup>)*

*Behaviour of the cards when receiving heartbeat triggers*

TRIGGER	CRU	Code sent by CRU to FEE	REGIONAL	LOCAL
<b>SOC</b> (Start Of Continuous)	Update internal Orbit and BCID counters Transmit command to all e-links <b>Reset internal bunch counter</b>	0x80	<b>Reset internal bunch counter</b> Reset acquisition FIFO <b>Assert "Active" bit</b> Start writing PHY events into acquisition FIFO ( <b>First event = SOC</b> )	<b>Reset internal bunch counter</b> Reset acquisition FIFO <b>Assert "Active" bit</b> Start writing PHY events into acquisition FIFO ( <b>First event = SOC</b> )
<b>EOC</b> (End Of Continuous)	Update internal Orbit and BCID counters Transmit command to all e-links <b>Reset internal bunch counter</b>	0x40	<b>Reset internal bunch counter</b> <b>De-assert "Active" bit</b> Stop writing PHY events into acquisition FIFO ( <b>Last event = EOC</b> )	<b>Reset internal bunch counter</b> <b>De-assert "Active" bit</b> Stop writing PHY events into acquisition FIFO ( <b>Last event = EOC</b> )
<b>PAUSE</b> (reject)	Update internal Orbit and BCID counters Transmit command to all e-links <b>Reset internal bunch counter</b>	0x20	<b>Reset internal bunch counter</b> <b>Assert "Rejecting" bit</b> Stop writing PHY events into acquisition FIFO ( <b>Last event = PAUSE</b> )	<b>Reset internal bunch counter</b> <b>Assert "Rejecting" bit</b> Stop writing PHY events into acquisition FIFO ( <b>Last event = PAUSE</b> )
<b>RESUME</b> (accept)	Update internal Orbit and BCID counters Transmit command to all e-links <b>Reset internal bunch counter</b>	0x10	<b>Reset internal bunch counter</b> <b>De-assert "Rejecting" bit</b> Start writing PHY events into acquisition FIFO ( <b>First event = RESUME</b> )	<b>Reset internal bunch counter</b> <b>De-assert "Rejecting" bit</b> Start writing PHY events into acquisition FIFO ( <b>First event = RESUME</b> )
<b>CALIBRATE</b>	Update internal Orbit and BCID counters Transmit command to all e-links <b>Reset internal bunch counter</b>	0x08	<b>Reset internal bunch counter</b> Write one event = CALIBRATE into acquisition FIFO Send LVDS pulse to Front-End Test cards	<b>Reset internal bunch counter</b> Write one event = CALIBRATE into acquisition FIFO
<b>SPARE</b>	Update internal Orbit and BCID counters Transmit command to all e-links <b>Reset internal bunch counter</b>	0x04	<b>Reset internal bunch counter</b> Write one event = SPARE into acquisition FIFO	<b>Reset internal bunch counter</b> Write one event = SPARE into acquisition FIFO
<b>RESET</b>	Update internal Orbit and BCID counters Transmit command to all e-links <b>Reset internal bunch counter</b>	0x02	<b>Reset internal bunch counter</b> Stop writing PHY events into acquisition FIFO <b>De-assert "Active" bit &amp; "Rejecting" bit</b> Reset acquisition FIFO Write one event = RESET into acquisition FIFO	<b>Reset internal bunch counter</b> Stop writing PHY events into acquisition FIFO <b>De-assert "Active" bit &amp; "Rejecting" bit</b> Reset acquisition FIFO Write one event = RESET into acquisition FIFO
<b>HC</b> (Health Check) or T_Fstart	Update internal Orbit and BCID counters Transmit command to all e-links <b>Reset internal bunch counter</b>	0x01	<b>Reset internal bunch counter</b> Write one event = HC into acquisition FIFO	<b>Reset internal bunch counter</b> Write one event = HC into acquisition FIFO

[1] O<sup>2</sup> Project CWG4. Proposal of an Heartbeat trigger for ALICE Run 3. Technical report, The ALICE Collaboration, 2013

[2] O<sup>2</sup> project WP1. Raw data and trigger message format preliminary proposal, R. Divià CERN/ALICE, 27 April 2017

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# Readout Chain Muon Identifier

*REGIONAL crate upgrade (MID\_LOC data format)*

*MID\_LOC data format at each e-link input in CRU*

Coding of <b>SOC, EOC, RESET</b> events in <b>LOCAL</b>	Number of bits	Coding of <b>CALIBRATE</b> events in <b>LOCAL</b>	Number of bits	Coding of <b>PAUSE, RESUME, SPARE, HC</b> events in <b>LOCAL</b>	Number of bits	Coding of <b>self triggered physics</b> event in <b>LOCAL</b>	Number of bits
START BIT (always '1')	1	START BIT (always '1')	1	START BIT (always '1')	1	START BIT (always '1')	1
CARD TYPE (always '1'=LOCAL)	1	CARD TYPE (always '1'=LOCAL)	1	CARD TYPE (always '1'=LOCAL)	1	CARD TYPE (always '1'=LOCAL)	1
LOCAL BUSY ('0'=OK; '1'=FIFO full)	1	LOCAL BUSY ('0'=OK; '1'=FIFO full)	1	LOCAL BUSY ('0'=OK; '1'=FIFO full)	1	LOCAL BUSY ('0'=OK; '1'=FIFO full)	1
LOCAL DECISION (tracklet)	1	LOCAL DECISION (tracklet)	1	LOCAL DECISION (tracklet)	1	LOCAL DECISION (tracklet)	1
ACTIVE ('0'=OFF; '1'=ON)	1	ACTIVE ('0'=OFF; '1'=ON)	1	ACTIVE ('0'=OFF; '1'=ON)	1	ACTIVE (always '1'=ON)	1
REJECTING ('0'=OFF; '1'=ON)	1	REJECTING ('0'=OFF; '1'=ON)	1	REJECTING ('0'=OFF; '1'=ON)	1	REJECTING (always '0'=OFF)	1
MASKED ('0'=OFF; '1'=ON)	1	MASKED ('0'=OFF; '1'=ON)	1	MASKED ('0'=OFF; '1'=ON)	1	MASKED ('0'=OFF; '1'=ON)	1
OVERWRITTEN ('0'=OFF; '1'=ON)	1	OVERWRITTEN ('0'=OFF; '1'=ON)	1	OVERWRITTEN ('0'=OFF; '1'=ON)	1	OVERWRITTEN ('0'=OFF; '1'=ON)	1
<b>SOC</b>	1	<b>SOC</b> (always '0')	1	<b>SOC</b> (always '0')	1	Always '0'	8
<b>EOC</b>	1	<b>EOC</b> (always '0')	1	<b>EOC</b> (always '0')	1		
<b>PAUSE</b> (always '0')	1	<b>PAUSE</b> (always '0')	1	<b>PAUSE</b>	1		
<b>RESUME</b>	1	<b>RESUME</b>	1	<b>RESUME</b>	1		
<b>CALIBRATE</b> (always '0')	1	<b>CALIBRATE</b>	1	<b>CALIBRATE</b> (always '0')	1		
<b>SPARE</b>	1	<b>SPARE</b>	1	<b>SPARE</b>	1	Internal bunch counter	16
<b>RESET</b>	1	<b>RESET</b> (always '0')	1	<b>RESET</b> (always '0')	1		
<b>HC</b>	1	<b>HC</b>	1	<b>HC</b>	1		
Internal bunch counter	16	Internal bunch counter	16	Internal bunch counter	16		
LOCAL board position in crate (0-15)	4	LOCAL board position in crate (0-15)	4	LOCAL board position in crate (0-15)	4		
Status: "0xF"	4	Data: "0xF"	4	Always '0'	4	Data: Non zero detector plane(s) (1 bit / word)	4
Status: Masks on inputs [(X4, Y4), (X3, Y3), (X2, Y2), (X1, Y1)]	32*4	Data: all strip patterns [(X4, Y4), (X3, Y3), (X2, Y2), (X1, Y1)]	32*4	N/A	0	Data: Non zero strip pattern(s) [(X4, Y4), (X3, Y3), (X2, Y2), (X1, Y1)]	32*i (i=1 to 4)
Total number of bits	168	Total number of bits	168	Total number of bits	40	Total number of bits	40+ 32*i (i=1 to 4)
Bunches needed to send	21	Bunches needed to send	21	Bunches needed to send	5	Bunches needed to send	9 to 21

# Readout Chain Muon Identifier

*REGIONAL crate upgrade (MID\_REG data format)*

*MID\_REG data format at each e-link input in CRU*

Coding of <b>SOC, EOC, RESET</b> events in <b>REGIONAL</b>	Number of bits	Coding of <b>PAUSE, RESUME, CALIBRATE, SPARE, HC</b> events in <b>REGIONAL</b>	Number of bits	Coding of <b>self triggered physics</b> event in <b>REGIONAL</b>	Number of bits
START BIT (always '1')	1	START BIT (always '1')	1	START BIT (always '1')	1
CARD TYPE (always '0'=REGIONAL)	1	CARD TYPE (always '0'=REGIONAL)	1	CARD TYPE (always '0'=REGIONAL)	1
REGIONAL BUSY ('0'=OK; '1'=FIFO full)	1	REGIONAL BUSY ('0'=OK; '1'=FIFO full)	1	REGIONAL BUSY ('0'=OK; '1'=FIFO full)	1
REGIONAL DECISION (tracklet)	1	REGIONAL DECISION (tracklet)	1	REGIONAL DECISION (tracklet)	1
ACTIVE ('0'=OFF; '1'=ON)	1	ACTIVE ('0'=OFF; '1'=ON)	1	ACTIVE (always '1'=ON)	1
REJECTING ('0'=OFF; '1'=ON)	1	REJECTING ('0'=OFF; '1'=ON)	1	REJECTING (always '0'=OFF)	1
MASKED ('0'=OFF; '1'=ON)	1	MASKED ('0'=OFF; '1'=ON)	1	MASKED ('0'=OFF; '1'=ON)	1
OVERWRITEN ('0'=OFF; '1'=ON)	1	OVERWRITEN ('0'=OFF; '1'=ON)	1	OVERWRITEN ('0'=OFF; '1'=ON)	1
<b>SOC</b>	1	<b>SOC</b> (always '0')	1	Always '0'	8
<b>EOC</b>	1	<b>EOC</b> (always '0')	1		
<b>PAUSE</b> (always '0')	1	<b>PAUSE</b>	1		
<b>RESUME</b>	1	<b>RESUME</b>	1		
<b>CALIBRATE</b>	1	<b>CALIBRATE</b>	1		
<b>SPARE</b>	1	<b>SPARE</b>	1		
<b>RESET</b>	1	<b>RESET</b> (always '0')	1		
<b>HC</b>	1	<b>HC</b>	1		
Internal bunch counter	16	Internal bunch counter	16	Internal bunch counter	16
REGIONAL crate number (0-15)	4	REGIONAL crate number (0-15)	4	REGIONAL crate number (0-15)	4
Status: Masks on tracklet inputs	4	Always '0'	4	Data: All tracklet inputs	4
N/A	0	N/A	0	N/A	0
Total number of bits	40	Total number of bits	40	Total number of bits	40
Bunches needed to send	5	Bunches needed to send	5	Bunches needed to send	5

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*REGIONAL crate upgrade (DCS)*

*Control registers (GBT-SCA-I<sup>2</sup>C) foreseen in the cards*

	REGIONAL (x16)		LOCAL (x256)
r-	ID	ID	ID
r-	Date	Date	Date
r-	Status	Status	Status
rw	Config	Config	Config
rw	masks	masks	masks
rw			Masks
rw			Masks
rw			masks
r-	GBTx0 switches & status	GBTx1 switches & status	Delay switches Xi
r-			Delay switches Yi



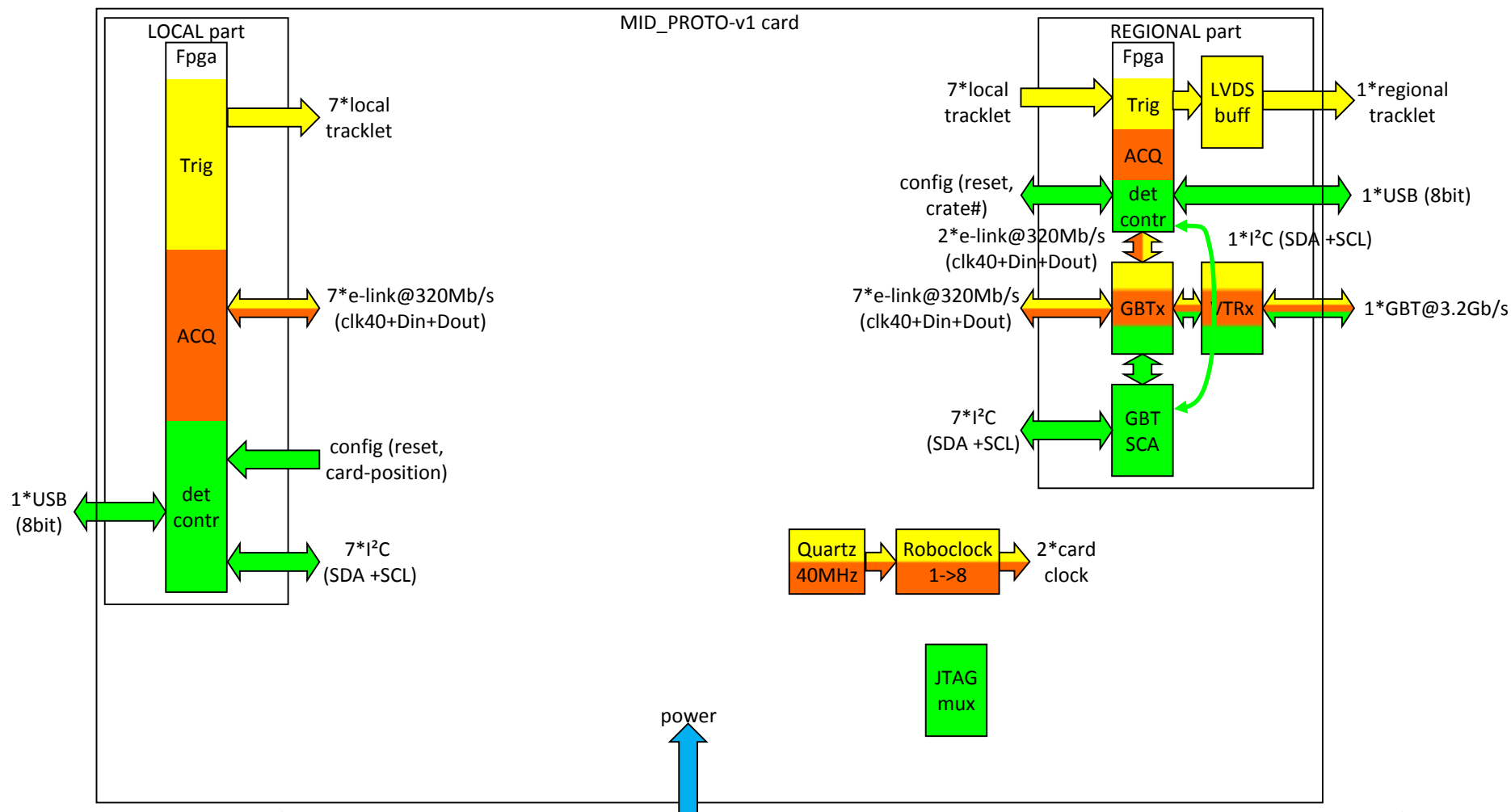
# Readout Chain Muon Identifier

*Readout architecture, functionalities and prototypes*

## Prototypes

# Readout Chain Muon Identifier

## REGIONAL crate upgrade (prototype)



“LOCAL” with 7 e-link@320Mb/s (clock@40MHz),  
7 I<sup>2</sup>C, 1 FPGA, 7 LVDS output,  
config, USB (8bit)

“REGIONAL” with 7 LVDS inputs, 9 e-link@320Mb/s  
(clock@40MHz), 1 GBTx, 1 GBT-SCA, 8 I<sup>2</sup>C,  
1 GBT links @3.2Gb/s, 1 FPGA, 1 LVDS output, config, USB (8bit)

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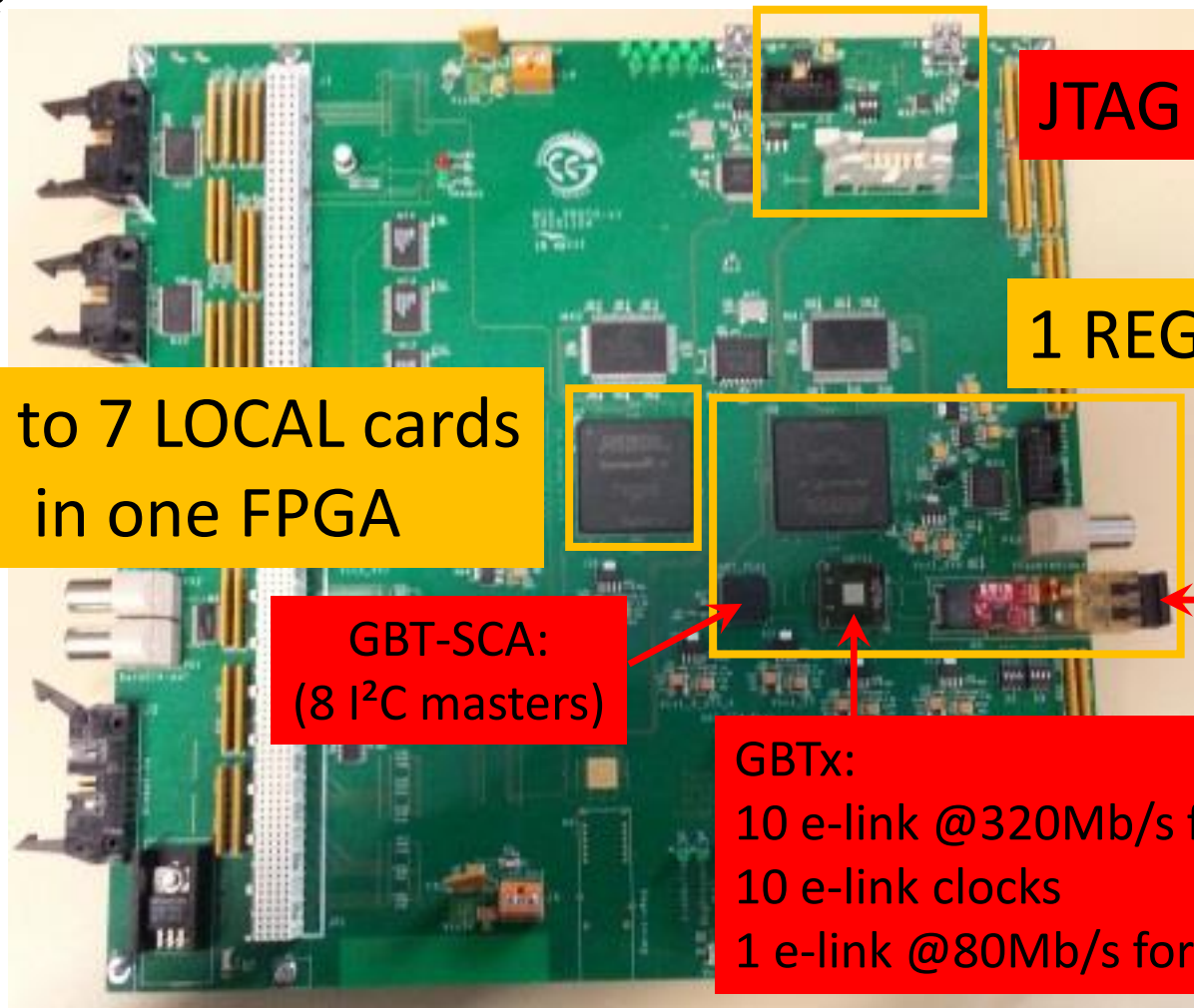
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# Readout Chain Muon Identifier

*REGIONAL crate upgrade (prototype)*

At SUBATECH since  
21 January 2016



JTAG mux

1 REGIONAL card

Up to 7 LOCAL cards  
in one FPGA

GBT-SCA:  
(8 I<sup>2</sup>C masters)

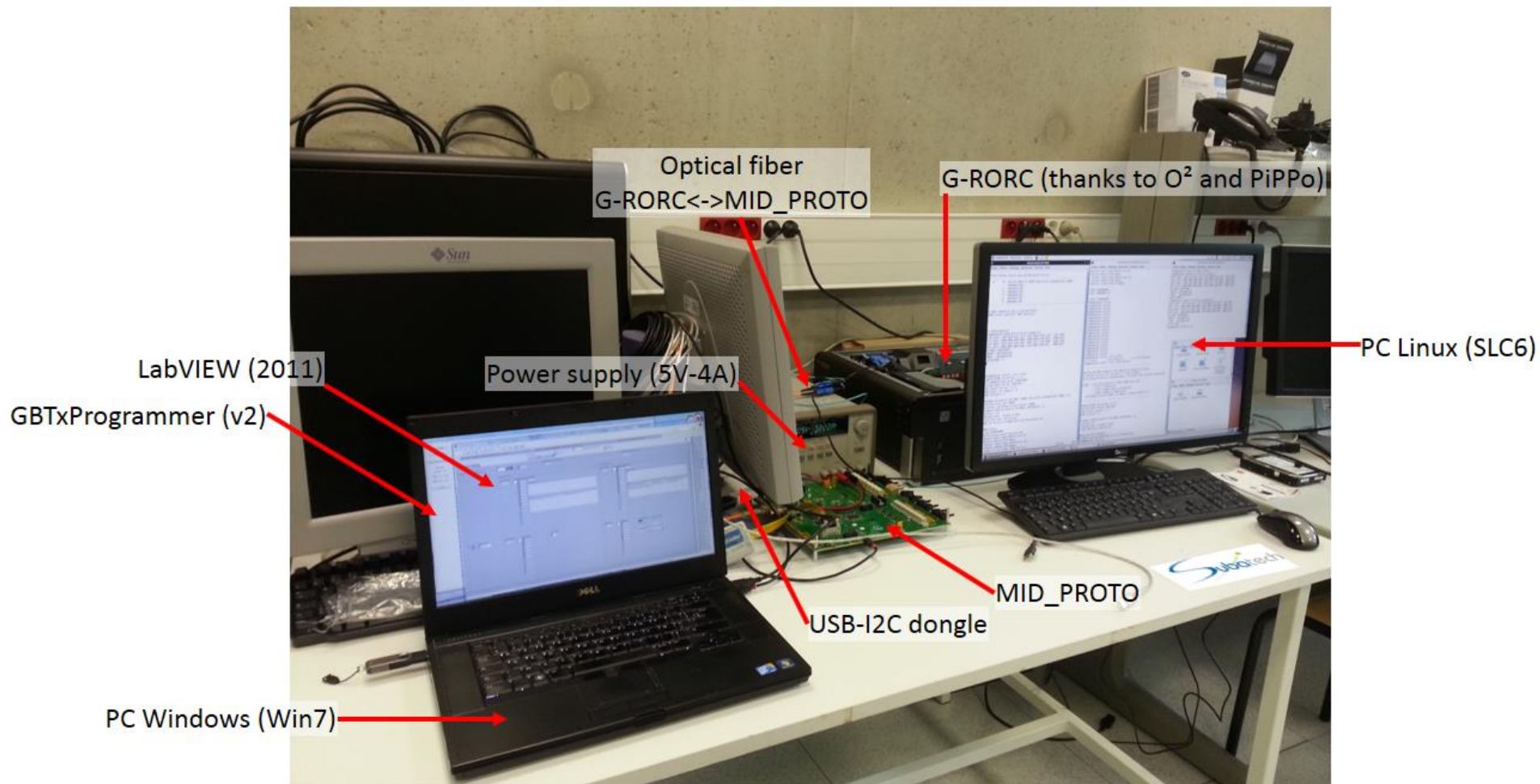
VTRx

GBTx:  
10 e-link @320Mb/s full duplex  
10 e-link clocks  
1 e-link @80Mb/s for GBT-SCA

# Readout Chain Muon Identifier

*REGIONAL crate upgrade (prototype)*

*Tests summary (1/2)*



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# Readout Chain Muon Identifier

*REGIONAL crate upgrade (prototype)*

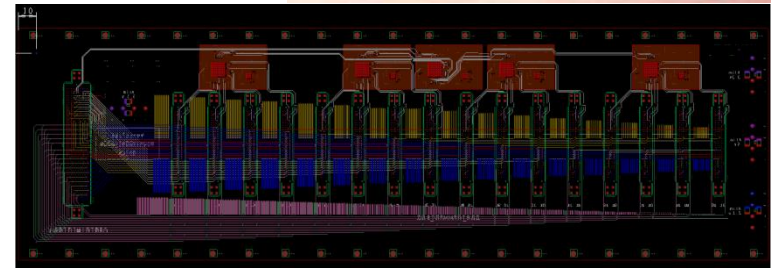
*Tests summary (2/2)*

- ✓ Firmware simulated in VHDL testbench
  - ✓ continuous readout
  - ✓ heartbeat triggers
  - ✓ USB debug
  - ✓ I<sup>2</sup>C detector-control
  
- MID\_PROTO-v1 card with G-RORC as testbench
  - G-RORC lent by ALICE-DAQ (Pierre Vande Vyvre & Filippo Costa)
  - Recent version of DATE installed in PC (Frédéric Lefèvre)
  - G-RORC installed in PC (Jean-Luc Beney)
  - Installed firmware developed by ALICE-O<sup>2</sup> (Filippo Costa)
  - Write on disk events corresponding to answers to heartbeat triggers
  - Write on disk events corresponding to self-trigger on incoming signals
  - Write and read-back a register in GBT-SCA

# Readout Chain Muon Identifier

*REGIONAL crate upgrade ()*  
*Next steps*

- MID\_PROTO-v1 card with G-RORC as testbench
  - Write a script to test DCS using GBT-SCA-I<sup>2</sup>C
- MID\_LOC-v1 card (Christophe & Patrice)
  - ✓ 3 cards at SUBATECH
  - Finalise Firmware under simulation
- MID\_REG-v1 card (Christophe & Patrice)
  - CAD progressing well
  - Finalise Firmware under simulation
- MID\_J2 card-v1 (Christophe & Stéphane)
  - CAD files ready for fab
  - Purchase order signed
  - 5 weeks delay for fab
- Replace the G-RORC by a CRU as testbench



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# Readout Chain Muon Identifier

*REGIONAL crate upgrade ()*

*Good News*

- A team from South Africa joined the MID
  - They have engineers working on the user firmware for MID in the CRU

*See next presentation*

*Thanks for your attention*

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*Readout architecture, functionalities and prototypes*

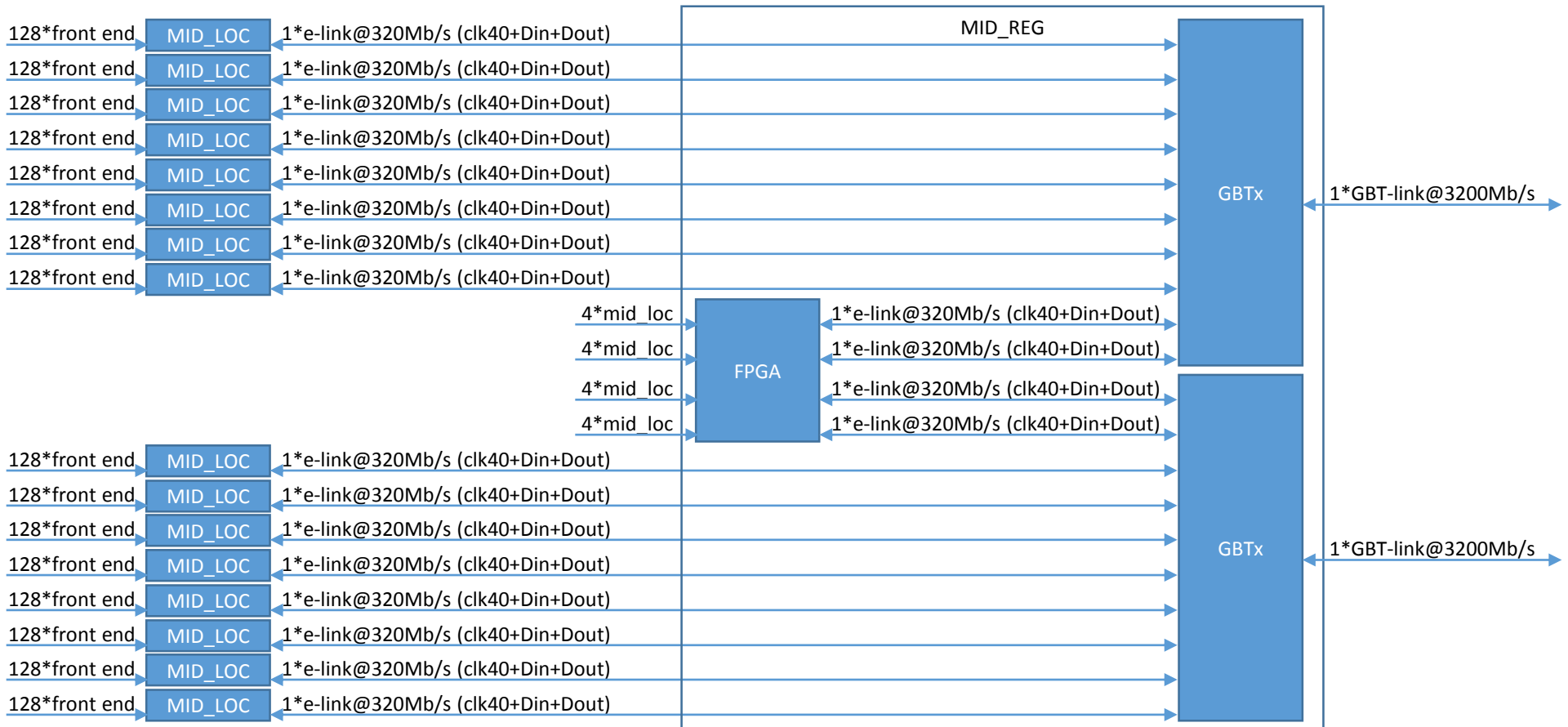
## Backup



# Readout Chain Muon Identifier

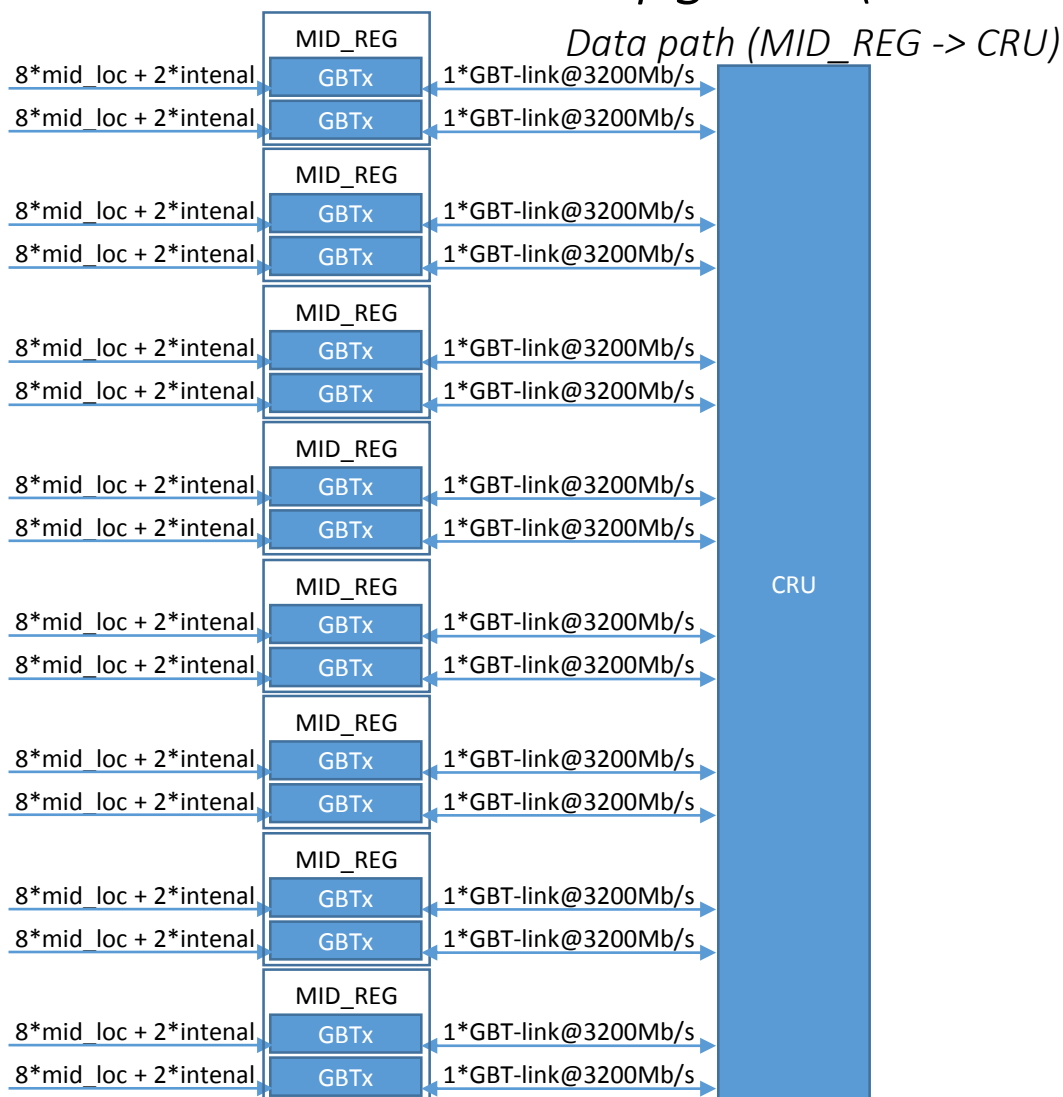
*REGIONAL crate upgrade (EDR on 16 June 2015)*

*Data path (Front-End -> MID\_LOC -> MID\_REG)*



# Readout Chain Muon Identifier

*REGIONAL crate upgrade (EDR on 16 June 2015)*



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# Readout Chain Muon Identifier

*REGIONAL crate upgrade ()*  
*CRUs needed*

2 CRUs of type “24/24” in the counting room

1 with 16 bidir GBT links to I36

1 with 16 bidir GBT links to O36

1 CRU of type “24/24” in South Africa

for user firmware development/maintenance in CRU

1 CRU of type “24/24” in Nantes

for firmware development/maintenance in readout electronics