Abstract

A Large Ion Collider Experiment (ALICE) at the Large Hadron Collider at CERN is upgrading some of its sub-detectors, with new front-end electronics to handle the expected higher Pb–Pb collision-rates in the next running period (Run 3) foreseen to start in 2022. The upgrade requires in part, of new sub-detectors for the central system while other existing sub-detectors belonging to the Muon spectrometer system such as the Muon Identifier (MID) will employ a continuous readout of the data from the front-end electronics, in contrast to the previous triggered readout. The devices currently use for the sub-detector readout chain can only run in triggered mode and must be replaced.

At the centre of the readout upgrade is the new approach based on the Common Readout Unit (CRU) developed to meet the ALICE requirements.

A new 8-channel integrated circuit called FEERIC has been designed to match the requirements of MID sub-detector. The FEERIC device contains a charge sensitive amplifier, a pulse shaper, and a 10-bit 10MHz analogue to digital converter for each channel and a common digital signal processor part. The digital signal processor provides various signal filtering and conditioning operations to improve on the data compression ability. The acquisition can be done in either triggered or continuous mode and the data is offloaded through 320 Mbps differential serial links, allowing a data throughput of up to 3.2 Gbps transmitted to the CRU.

The key aim of this thesis has been to plan, build, evaluate and validate the user logic component of the CRU firmware to meet the needs of the MID sub-detector. Innovative methods have been used to reduce the bandwidth produced by the sub-detector readout electronics, as well as adaptations to facilitate data handling later in the processing chain. Research procedures, simulations, evaluation methods, and applied methods are used to build a consistent prototype design.

Acronyms

ADC	-	Analog Digital Converter
ALICE	-	A Large Ion Collider Experiment
LHC	-	Large Hadron Collider
NRF	-	National Research Foundation
LABS	-	Laboratory for Accelerator Based Science
FPGA	-	Field Programmable Gate Array

Chapter 1

Introduction

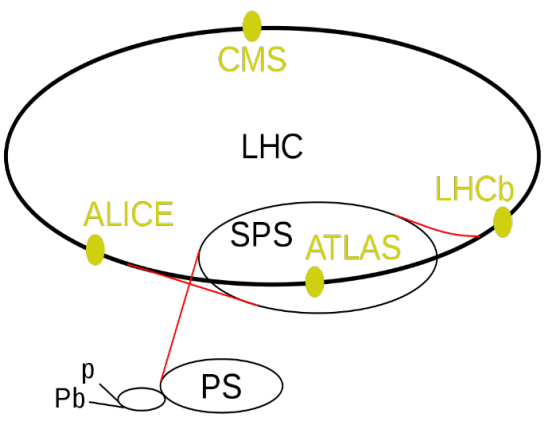
The unique properties of Field Programmable Gate Array (FPGA) such as high-speed, high brightness, extreme collimation, polarization, and time structure, have enabled a number of new and important techniques since the early days of their use in the 1960s. Today's FPGA are the products of several generations of advances technology and are often identified as one of the main components used in the readout chain of detectors in high-energy physics experiments.

The proposed enhancement of the ALICE detector performance will enable detailed and quantitative characterization of the high density, high temperature phase of strongly interacting matter, together with the exploration of new phenomena in QCD. In the following we outline the physics motivation for running the LHC with heavy ions at high luminosities and summarize the performance gains expected with the upgraded ALICE detector.

1.1 Background

1.1.1 ALICE experiment

CERN is the world's leading laboratory for scientific research located on the border of Switzerland and France. CERN houses the Large Hadron Collider (LHC). The LHC is about 100 meters below the surface and 27 kilometres in circumference. It produces particle beams i.e. proton-proto (p-p), proton-lead (p-pb) and lead-lead (pb-pb) at ultra-relativistic energies to create, amongst other, a highly dense form of matter reminiscent of the early universe a microsecond after the big bang. Spread along the LHC ring are four individual experiments positioned around the four collision points where the beams collide. As shown in Figure 1.1, one of these experiments is A Large Ion Collider Experiment (ALICE).



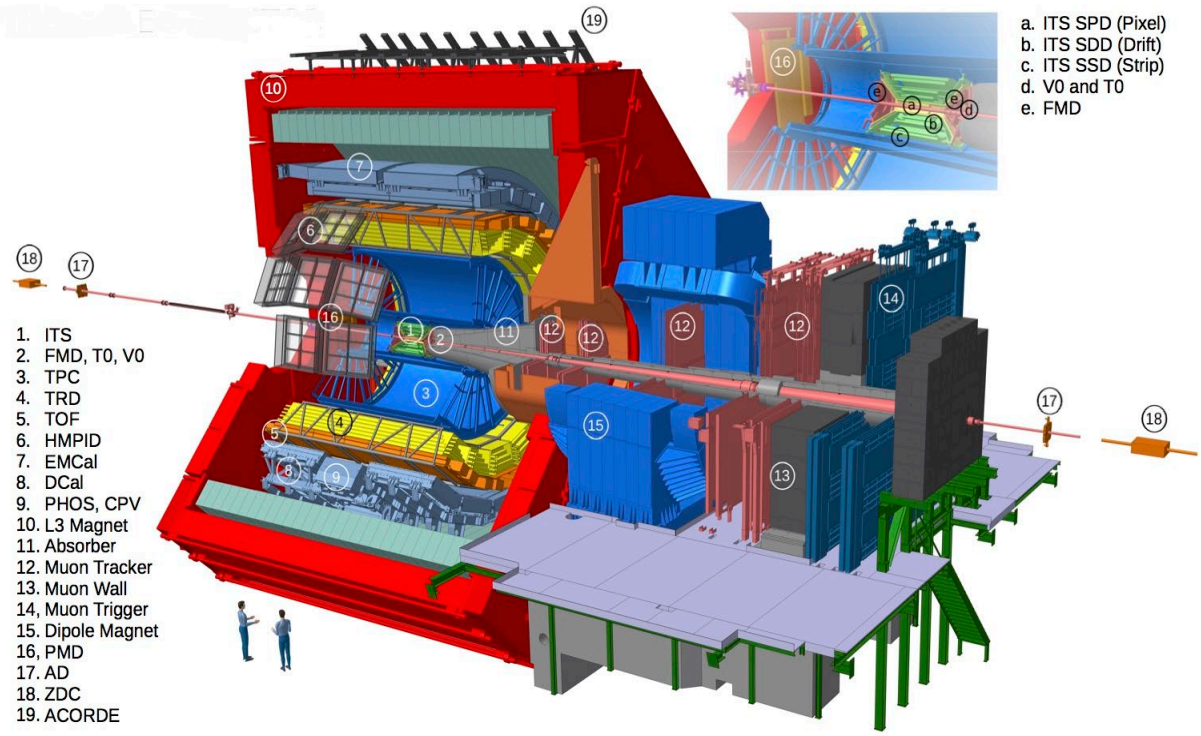
LHC ring and its four main experiment, ALICE, ATLAS, LHCb and CMS

1.1.2 Physics goals

For few millions of seconds after the big bang, the universe consisted of hot soup of elementary particles called quark and gluons. A few microseconds later, those particles began cooling to form protons and neutrons, the fundamental of matter. Over the past decades, scientists around the world are trying to re-create that soup, known as the Quark-Gluon Plasma (QGP) by smashing particles together with enough energy to produce a temperature higher than the centre of the sun. By keeping the temperature and the density high enough, scientists can obtain a new phase of matter where quarks and muons are deconfined to QGP, such conditions can be created in high energy heavy-ion collisions at the CERN LHC more precisely in the ALICE experiment. ALICE is the only detector at the CERN LHC dedicated to the study of interacting matter, in particular the properties of the QGP.

1.1.2 Detector and sub-detectors

In order to reconstruct and identify a myriad of particles created in the collisions, the ALICE detector shown in Figure 1.1, is using a set of 19 sub-detectors extended over a length of 26m and 16m in height and width, weighing over 10 000 tons. The sub-detectors provide information about the mass, the velocity and the electrical sign of the particles and each is designed to study a different aspect of the particles created in the collisions.



Schematic overview of the ALICE detector with its sub-detectors.

ALICE detector consists of two main regions: the central barrel region and the forward region known as the muon spectrometer.

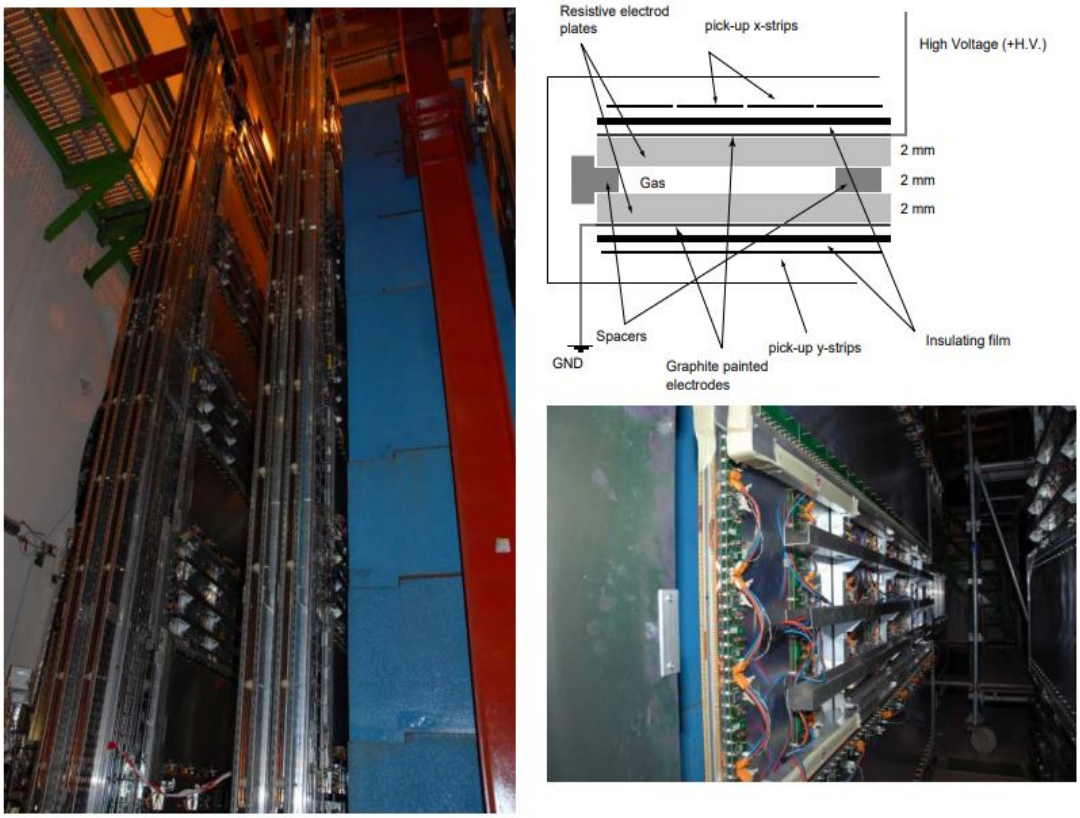
The central barrel is covered by a solenoid L3 magnet, and it contains the Inner Tracking System (ITS) composed of six layers of silicon detectors: Silicon Pixel Detector (SPD), Silicon Detector Drift (SDD) and Silicon Strip Detector (SSD). The ITS is enveloped by a circular Time Projection Chamber (TPC), three particles identification arrays of Time of Flight (TOF), a ring imaging of Cherenkov High Momentum Particle Identification Detector (HMPID) and a Transition Radiation Detector (TRD). The surface layer contains the Electromagnetic Calorimeters (EMCal), and the Photon Spectrometer (PHOS). Small-scale sub-detectors used for global event identification and triggering such as the Zero Degree Calorimeter (ZDC), Photon Multiplicity Detector (PMD), Forward Multiplicity Detector (FMD), T0 and V0 are located away from the interaction point. On the three upper faces of the solenoid L3 magnet is A Cosmic Ray Detector (ACORDE). It consists of an array of plastic scintillator counters and together with the muon spectrometer, they provide accurate information about cosmic rays.

The muon spectrometer is designed to measure muon production from the decays of quarkonia, low mass vector mesons, heavy flavor hadrons and bosons [ ]. The quarkonia is detected in their dimuon decay channel in the angular acceptance of 171˚- 178˚, corresponding to the pseudo rapidity region $-4.0 < \eta < -2.5$ [ ]. The muon spectrometer covers a total length of $\simeq$ 17 m and it is composed of the following components: absorbers to filter all particles except muons coming from the interaction point, a large dipole magnet, a high-resolution Muon Tracker, a 120 cm thick iron wall (Muon Filter), and a Muon Trigger (MTR).

The muon trigger is the former name given to the muon identifier prior the upgrades. Further technical details concerning the muon trigger will be described in details in the next sections as the work described in this thesis, is solely focused on this specific sub-detector.

1.1.4 Muon Trigger

The muon trigger system is intended to analyse high muons produced in heavy quarkonium and open heavy flavour meson decays. Equipped with a configurable threshold, the sub-detector is able to provide trigger signals for selecting events of interest and discarding events with only low muons. The muon trigger is based on 72 single gap Resistive Plate Chamber (RPC) detectors with x-y read-out, arranged in 2 stations of 2 chambers each at a distance of about 16 m and 17 m from the interaction point respectively. Each RPC consists of two planes, a positively-charged anode and a negatively-charged cathode, both made of very high resistivity plate plastic material and separated by 2 mm of gas. Once a charged particle such as a muon passes through the chamber, electrons are knocked out of the gas atoms. These electrons in turn hit other atoms causing a mass of electrons. The electrodes are transparent to the electrons, which are instead picked up by external metallic strips outside the chamber after a small but precise time delay. The pattern of hit strips gives a quick measure of the muon momentum, which is measured by the Front-End Electronics (FEE) known as A DUaL Threshold (ADULT) cards [ ]. The signals from the ADULT cards are then propagated to the readout electronics based on three programmable circuits (local, regional and global) working in pipeline mode at 40 MHz, to make immediate decisions about the validity of the data. The ADULT electronics were initially developed for streamer mode operation with a gas mixture of Ar, CH2F4, C4H10 and SF6 for the LHC Run 1 (2010-2012) [ ]. Few years later, a maxi-avalanche operation mode was introduced for the LHC Run 2 (2015-2018) [ ], where the signal amplitude is smaller than the streamer mode, but still compatible with the minimum threshold ($\approx$ 7 mV) set in the ALDULT cards.



Left: view of the two trigger stations behind the filter of the muon. Right-top: schematic view of the cross section of the RPC. Right-bottom: an independent RPC module with ADULT electronics [ ]

1.2 LHC Run 3

Based on data collected in Run 1 and 2 (~10 petabytes of raw data) [ ], ALICE is the leading heavy-ion experiment in the world and is quickly expanding the knowledge gathered in previous experiments all over the world. ALICE is currently going through three years planned second Long Shutdown called (LS2) that has started in 2018 to prepare for Run 3. At the centre of the ALICE upgrade strategy is a high-speed readout approach based on a Common Readout Unit (CRU). The CRU has been developed for detector data readout, concentration, reconstruction, multiplexing and data decoding onto the online-offline (O^2) computing system.

The LHC Run 3 was planned to start from 2021 onwards but has been postponed to 2022 due the global pandemic [ ]. It is predicted to have a peak luminosity of 6×1027 cm^2 per second. Many of the proposed observables require a shift in the data taking strategy, moving away from triggering a small subset of events to online processing and recording of all collisions delivered by the LHC. To achieve these goals, ALICE detector is being upgraded in such a way that all interactions will be inspected. The upgrade entails the replacement of some sub-detectors while most others including the muon trigger, are moving to new front-end electronics and readout system to allow all detectors to be read out at near the expected interaction rate up to 50 kHz lead-lead (Pb-Pb) collisions per second.

1.2.1 Muon Trigger to Muon Identifier

For the past 10 years since the LHC Run 1, the selection of single muon and di-muon events with a maximum trigger rate of 1 kHz has always been provided by the muon trigger [ ], however, to cope with the increased luminosity of the LHC during Run 3, this current trigger strategy is no longer sufficient. The upgrade trigger strategy does not require a muon trigger, since all event of interests will be read out upon the interaction trigger before online selections. As part of the upgrade, the existing muon trigger sub-detector has been renamed to the muon identifier (MID).

The transition from MTR to MID during the LS2 entails, the replacement of the RPC ADULT electronics by a new ASICS called the Front-End Electronics Rapid Integrated Circuit (FEERIC). Unlike ADULT, FEERIC performs amplification of the analogue signals from the RPCs. The RPCs will be operated in avalanche mode with a significant reduction of the charge produced in the gas, hence limiting ageing effects. Furthermore, in order to cope with the given readout rates, both the local and regional readout cards have been redesigned. Since the triggering functionalities are abandoned, a simplified design has been implemented. The hardware implementation of the regional and local card is identical, reducing the design and production effort by re-using the same hardware and adapting the FPGA firmware. The global crate has been replaced by a regional crate equipped with backplane bus card that serves as interface between the regional and local cards.

1.3 Problem statement

Several problems occurred during the transition of MTR to MID. These problems were observed throughout a preliminary series of tests conducted on the MID readout chain. The upgraded system revealed limitations when running without data pre-analysis performed in the CRU firmware level. Among these limitations are: large data rate, desynchronization of data, and failure to process the entire readout electronics.

1.3.1 Large data rate

A bandwidth of 3.2 Gbps is produced by each regional link of the readout chain [ ]. This large amount of data is a problem for the O² computing facility to conduct data processing concurrently without data compression at the CRU firmware level. Furthermore, the MID sub-detector is expected to read out data from collisions every 20 μs and the regional crate continuously transmits data to the CRU every 25 ns. This means only 4 Mbps out 3.2 Gbps are worth analysing and might turn out to be valuable data. The remaining data is meaningless and must be suppressed. Holding these data in the memory leads to poor efficiency and wasteful use of memory.

1.3.2 Desynchronization of data

The data obtained from all readout electronics occurs simultaneously, at fixed periods and is transmitted to the CRU over a wide spectrum of optical links. However, differing transmission delays result in the data from the various links to lose synchronization when transmitted to the O² computing system and causes more problems further along the chain at the synchronous reconstruction level [].

1.3.3 Failure to process the entire readout electronics

The O^2 computing system is capable of handling the data rate from a single regional crate at the expense of 2 core processors. Attempting to use 1 core to decode a single regional crate leads to irreversible data loss. Hence, it takes 2 core processors to decode a single regional crate. However, the computer used in the readout chain contains 20 core processors [ ]. In order to decode data from the entire readout chain, that computer would need 32 core processors, not to mention any additional cores required to perform further processing of the decoded data. This makes it impossible for a single computer to process data from the entire front-end system.

1.4 Research aim

The ALICE collaborators participating in the MID project are searching for new ways to process data. Many alternatives have been suggested, but most of them entail significant improvements in the existing readout chain and man power such as changing the algorithm implemented in the O^2 processing to cope with the large data rate, acquiring additional CRUs and core processor computers to process data from the entire readout electronics. A thorough analysis review revealed that, the most efficient and cost-effective solution is to take advantage of the existing high-speed FPGA incorporated in the CRU by designing a customized user logic firmware to meet the requirements of the readout chain.

The user logic is a specific sub-detector component, that can be implemented into the CRU firmware through a specific compilation [ ]. It is developed by the sub-detector teams and has the capability to perform low-level data processing and other additional features before forwarding it to the O^2 computing facility for further analysis. The aim of this research is to improve the way data are processed in the MID readout chain by means of a customized user logic firmware before the start of the LHC Run 3.

1.5 Objectives

The research aim stated above is achieved through the following objectives:

- Review and analyse different components of the readout chain
- Select the best user logic algorithm
- Identify and subsequently remove meaningless data
- Receive timing and trigger information
- Synchronize essential data before performing the correct analysis
- Reformat data transmitted from the readout electronics
- Transmit data in the order required by the O^2 computing facility
- Handle errors identified in the readout electronics data
- Successfully validate the user logic simulation tests
- Successfully validate the user logic hardware tests
- Make recommendations for future improvements

1.6 Hypothesis

There is a possibility of designing and developing a stable and reliable user logic firmware that can improve the way data is processed in the MID readout chain. This can be achieved by developing an algorithm based on systems requirements. However, the difference in protocol between various systems of the readout chain makes it complex and can be time consuming. The main question to be considered is whether a user logic prototype can be designed and tested to meet the requirements of the MID readout chain in a timely manner prior to the start of the commissioning phase of the MID sub-detector, and whether or not this prototype can be used to develop a realistic user logic capable of processing data from the entire readout chain, considering hardware and software restrictions of the approved FPGA.

1.7 Delineation

The thesis is limited to the design and development of the user logic firmware prototype capable of pre-analysing data from 2 regional links of the MID readout chain. This research analyses in detail different systems used in the readout chain and improves the way data are processed in the CRU. The proposed scheme is developed after intensive research and good understanding of the ALICE detector. Hence, the incorporation of the user logic component into the existing CRU firmware is done through conformance with established requirements and practice. Additionally, important technical decisions such as hardware, communication protocols, design tools, programming languages and most relevant the resource usage limit of the research in question were long established before the beginning of the research.

Comparison in performance between the final design of the user logic expected to be delivered at CERN prior the beginning of the LHC Run 3 and the proposed user logic prototype is done. The following features are not included in the research investigations of the thesis:

- Merging and reformatting data from 16 regional link into 2 PCIe Endpoints (Dwrappers)
- Optimization of the user logic to reduce the memory usage in the FPGA
- Trigger and timing monitoring via PCie using Avalon Memory Mapped
- GBT packet monitoring via PCie Avalon Memory Mapped
- Configuration of the user logic parameters via PCie using Avalon Memory Mapped
- Develop a python or C++ script to facilitate the debugging and configuration of the user logic

1.8 Collaboration and main contributions

The National Research Foundation (NRF) iThemba Laboratory for Accelerators Based-Science (LABS) is part of the ALICE collaboration, and contributes to the ALICE Muon Spectrometer upgrade, in particular the MID. In collaboration with the Cape Peninsula University of Technology (CPUT) and the University of Cape Town (UCT), NRF iThemba LABS is responsible for conducting research and developing the CRU user logic firmware for the MID readout chain, including setting up a testbench data acquisition readout chain and maintenance thereafter.

The user logic project started in early 2018, with early research conducted by Nathan Boyles, a master student from the Electrical Engineering department at UCT. In early 2019, He delivered an early proof of concept of the user logic, which was completly discarded and identified as outdated by MID experts due to the rapid development of the ALICE CRU software and firmware projects. In mid-2019, Nathan left the project and, I took over the responsibility of design, development and prototype of user logic. Together with Dr C.Renard (expert in the readout electronics at the university of Nantes, France), the requirements to process data from 2 regional links of the readout chain were established. To keep track of the rapid development of the CRU software and firmware, frequent meetings are scheduled with Dr F.Costa (CRU software expert at CERN) and Dr O.Bourrion (CRU firmware expert at the university of Grenoble, France). Furthermore, Dr D.Stocco (O^2 data analysist expert at the university of Nantes, France) whose the outcome of this research may affect the way data will be handled at the next phase of the data acquisition, has set some additional requirements and constraints to facilitate the readability of the user logic output data.

Overall, the design and development of the ALICE CRU user logic firmware prototype for the MID readout chain is provided by the Electrical Engineering department at CPUT with support from various collaborators using NRF iThemba LABS advanced technology.

1.9 Methodology

The research methods that are utilized for the development of this thesis are:

- **Literature review:** since there is no written literature on the readout chain, the information is gathered by reading technical specification papers, IEEE published journals, conferences, interviewing specialist engineers in the data acquisition chain, and through Internet

- **Prototyping**: Intel Quartus pro 18.1 is the main software environment recommended and used to design and develop the user logic. For the purpose of this thesis, two different prototyping methods are implemented. The rapid throwaway [ ], this method involves exploring ideas by quickly developing a prototype based on preliminary requirements that is then revised through simulation tests feedback. Once validated, the evolutionary [ ] approach is then introduced. This approach uses a continuous, working prototype that is refined after each iteration of hardware tests feedback.

- **Simulation tests:** ModelSim is the simulation software used to verify the functionality of the user logic algorithm by analysing each component of the model. A more advanced simulation is performed by merging the CRU firmware simulation files [ ] as well as the MID readout electronics firmware simulation files [ ] into a single testbench for more efficient and accurate results.

- **Hardware tests**: a testbench available in the laboratory at iThemba LABS is developed for practical work. Expected tests for conformance include testing of the user logic prototype using a fully functional testbench setup capable of emulating the same events generated by the MID sub-detector readout chain at CERN.

- **Data collection:** simulation and hardware tests are conducted in order to collect practical data coming in and out of the user logic firmware. Comparison between the input and output data is done to perform an effective assessment on the user logic algorithm

1.10 Thesis outline

This thesis begins with the provision of the background information and examines the problem being addressed. Rudimentary objectives of the project are identified and an overview of the methodology used to achieve these objectives is presented. The hypothesis is outlined and constraints are presented.

Chapter 2

presents in greater depth, the readout electronic chain and its most important components and protocols. Furthermore, it expands on the methodology used to fully ascertain scope, constraints, objectives and evaluation procedures to successfully complete the project. Furthermore, it builds on the methodology used to completely determine the project's scale, limitations, goals, and assessment procedures.

Chapter 3

presents a detailed conceptual design of an envisaged system that conforms to the requirements previously established.

Chapter 4

tests the performance of the prototype of the conceptual design previously presented in relevant fields of metric for a project of this nature.

Chapter 5

The results obtained, performance of the prototype, the key findings, and the thesis deliverables are summarized in this chapter. The recommendations for possible future work and the extension of the project is also discussed in this chapter.

Appendix A

concludes this thesis by performing a comparison between the established objectives of the project and the performance of the prototype, results are then presented. Finally, additional work that needs to be done is discussed. This includes architecture not developed in this work and enhancements to the user logic.

Appendix B

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1.11 References