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A Gigabit Transceiver for Data Transmission in Future High Energy Physics Experiments

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Abstract

The transmission of data from detectors in future high energy experiments will be driven by a number of requirements. In many cases, raw bandwidth is the strongest of these but other needs such as diverse functionality, compactness, low power and radiation resistance are equally important. The GigaBit-Transceiver project has been launched to provide a solution to these problems. The aim is to deliver a chip-set to build a bidirectional optical link transmitting and receiving serial data at 4.8 Gigabit/s. The project is based on three integrated circuits; a trans-impedance amplifier to receive signals from a photo-diode, a laser driver, and a transceiver containing a high-speed serialiser and de-serialiser. All of these have been successfully prototyped, and this paper will focus on the design and results from the serialiser/deserialiser prototype. This has been designed in commercial 130 nm CMOS with particular emphasis on enhancing its immunity to single-event-effects. The specific design features to achieve this will be described. The chip has been fully characterized in the lab, and jitter and bit-error-rate measurements are presented. The custom packaging of the chip will also be described together with the next steps foreseen in the project.

KEYWORDS: VLSI circuits; CMOS; radiation hard electronics; radiation hard optical link

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1. Introduction

Future particle physics experiments are being planned to exploit more and more the high luminosity available at particle accelerators such as the Large Hadron Collider at CERN. These will generate unprecedented volumes of data to be transmitted off the detectors. To do this efficiently in terms of cost and power consumption requires the development of new data links with greater bandwidth than those currently operating in experiments. This demand for bandwidth can be achieved through faster serial data rates and modern CMOS technologies. However, many systems require data transmission from areas inside the detector subject to intense levels of radiation so any components of such a link must survive this environment and operate efficiently within it. The GigaBit Transceiver (GBT) project has been proposed to satisfy these requirements. Its aim is to produce a compact radiation-tolerant transceiver chipset that operates with minimal power and is versatile enough to cover a number of different interfaces to detector systems.

The concept of the GBT project is shown in Figure 1. The GBT chipset operates together with radiation-tolerant optoelectronic components produced by its sister project, the Versatile Link [1], to form a bi-directional link with a serial rate of 4.8 Gbit/s. The components of the GBT chipset are a trans-impedance amplifier (GBTIA) to receive signals from a photo-diode (PD), a laser driver (GBLD) to modulate the current driving a laser, and a transceiver (GBTX) containing a high-speed serialiser and de-serialiser. This also acts as the interface to the front-end electronics of the detector system. Note that in standard operation, the clock of the GBTX is recovered from the received serial data stream and clocks provided to the front-end electronics are derived from this. The functionality of this chipset is mirrored at the opposite end of the link, but because this is a radiation-free environment the circuitry is implemented in a commercial field-programmable gate-array (FPGA). Note that the concept has been conceived to allow the transmission of three different classes of data, namely clocks and triggers, data from the detector (DAQ) and slow controls. An additional chip, known as the GBTSCA, is also under design and this will act as an interface to provide a number of standard slow-control protocols to the front-end electronics, such as I2C and JTAG. The GBTIA, GBLD and GBTX have all been prototyped, and the rest of this paper will concentrate on the design and testing of the GBTX prototype, known as the GBT-SERDES. Results from the GBTIA and GBLD prototypes can be found in references [2] and [3].

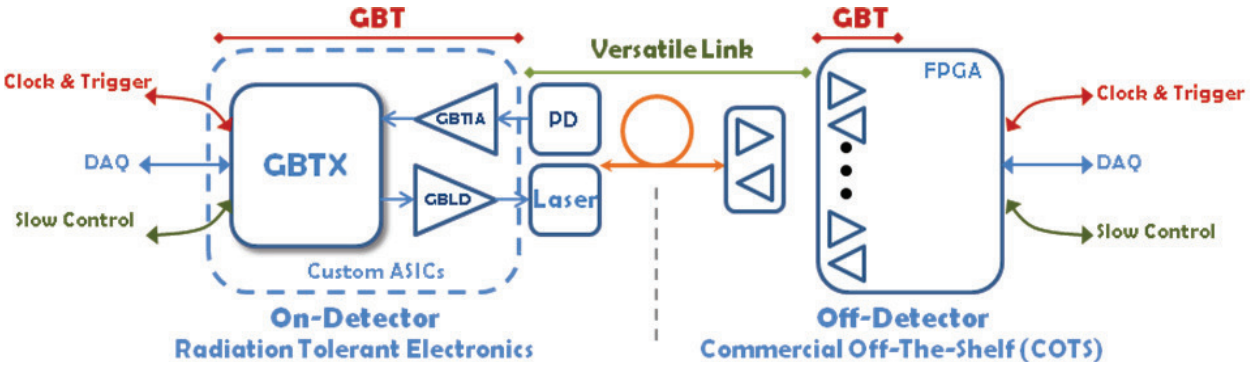

Figure 1: The components of the GBT project and the Versatile Link.

2. GBT-SERDES design

A number of constraints had to be considered in the design of the GBT-SERDES that are unique to applications in high energy physics and do not apply to links designed for commercial applications. The most important is tolerance to radiation, in particular the cumulative damage from doses of ionizing radiation and transient link errors caused by single-event-effects (SEEs). SEEs can also in some cases lead to a data link malfunctioning for a period of time and hence significant losses of data. Immunity to cumulated ionizing dose is guaranteed by the use of 130nm CMOS technology that has been shown to withstand doses beyond 400 Mrad [4]. Transient effects have been mitigated by design. All logic in the GBT-SERDES is triplicated and final results are calculated using voting gates. This also includes the clocks driving the sequential logic and three independent balanced clock trees were used inside the chip. The use of triple redundancy and the extra gates it requires does however have a detrimental effect on the maximum operational frequency of the circuit, which had an impact on the architecture of the high speed serialiser and de-serialiser circuits described below. Immunity to transients was further enhanced by operating the phase-locked-loops (PLLs) with bias currents higher than those necessary for achieving low phase-noise operation at the operating frequency. This reduces the sensitivity to current transients that could directly translate into jitter, but does so at the expense of an increase in power consumption. A simulation study of the effectiveness of this technique is presented in [5].

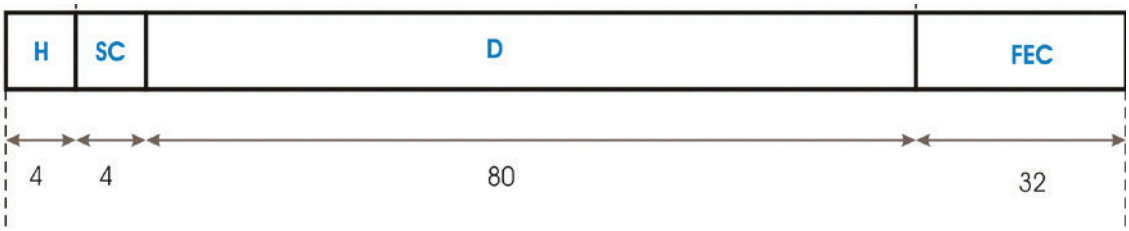

Figure 2: Frame format of the GBT protocol

Further immunity to transient errors is provided by the choice of protocol for the serial data transmission. Data frames of 120 bits are serialized every 25 ns at 4.8 Gbit/s, and the frame content is shown in Figure 2. A fixed 4-bit header (H) field is followed by 4 bits dedicated to slow-control data (SC). 80 bits are available for user data (D) and the rest of the frame consists of 32 bits of a forward-error-correction (FEC) field using a Reed-Solomon code derived from the data [6]. This can identify and correct up to 16 consecutive wrong bits in the data stream. Note that in the final GBTX chip, another mode will allow the use of 112 bits for data transfer by bypassing the FEC field, but hence with a greater risk of link errors. Figure 3 shows the implementation of the protocol in the GBT-SERDES transmitter. The header field is used for frame synchronization. The SC and D fields pass through a pseudo-random scrambler to ensure a DC-balanced frame and enough transitions in the serial data stream to allow recovery of a clock. Header, scrambled data and FEC are then serialized. The reverse procedure is carried out by the GBT-SERDES receiver.

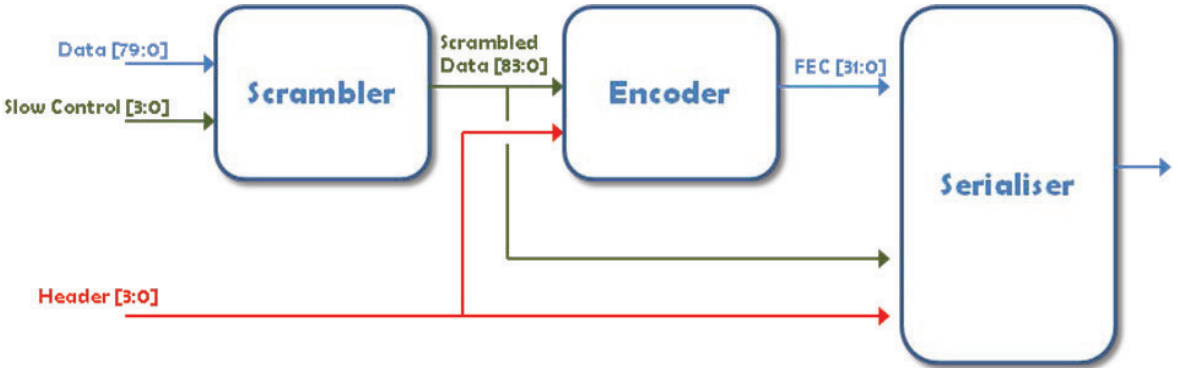

Figure 3: GBT transmission sequence

The serialiser uses three shift registers clocked at one third of the line rate (1.6 GHz). Each register is loaded with 40 bits of the 120-bit frame, and the 4.8 Gbit/s stream is formed using a fast multiplexer switching at 4.8 GHz at the output of the shift registers. In this way, the amount of circuitry operating at the serial rate is kept to a minimum. Complete details of the serialiser design can be found in [5]. A similar philosophy has been used for the deserialiser. The incoming 4.8 Gbit/s data stream is de-multiplexed into two half-rate streams each loading a shift register clocked at 2.4 GHz. The 120-bit frame is formed from the contents of these registers latched into parallel registers by a 40 MHz 'frame-clock'. This frame-clock is derived from the clock recovered from the data stream. Frame synchronization is maintained by a state-machine who looks for the presence of the 4 header bits in defined locations in the parallel registers. At power-up or if frame synchronization is lost, the state-machine will launch a search sequence for the header by shifting the phase of the frame-clock in steps of the 2.4 GHz clock period until the frame header appears in the correct location in the parallel registers. More details of the serialiser, PLL and clock recovery designs can be found in [7].

The high speed signals to and from the GBT-SERDES required a custom package for the chip to satisfy the bandwidth and signal integrity requirements. A flip-chip die-attach technique was chosen to provide high bandwidth interconnects. This brought other benefits such as the possibility of direct cooling on the backside of the die and reduced the difficulties of handling a high density of input/output (IO) signals. The flip-chip technique also allowed the placing of power supply connections close to or even within the circuit blocks. Figure 4 left shows the final chip layout. The full custom part (serialiser, deserialiser and clock generator) is on the right of the chip while the digital logic core is in the centre. The circular bump pads form a 13 x 13 matrix across the surface. Those directly above the circuitry are the power supply connections or the high speed signals. Around the top, bottom and left edges are the digital IOs where the rectangular structure beside each pad is the corresponding driver/receiver. Figure 4 right shows a photograph of the die with flip-chip bumps attached at a pitch of 250 μm. Some bumps are missing from this die due to a manufacturing error later corrected by the vendor. The dies were then flip-chip bonded to a ball-grid-array package for mounting on a test board. This technique proved successful and will be used for the final GBTX chip where the IO count will exceed 400.

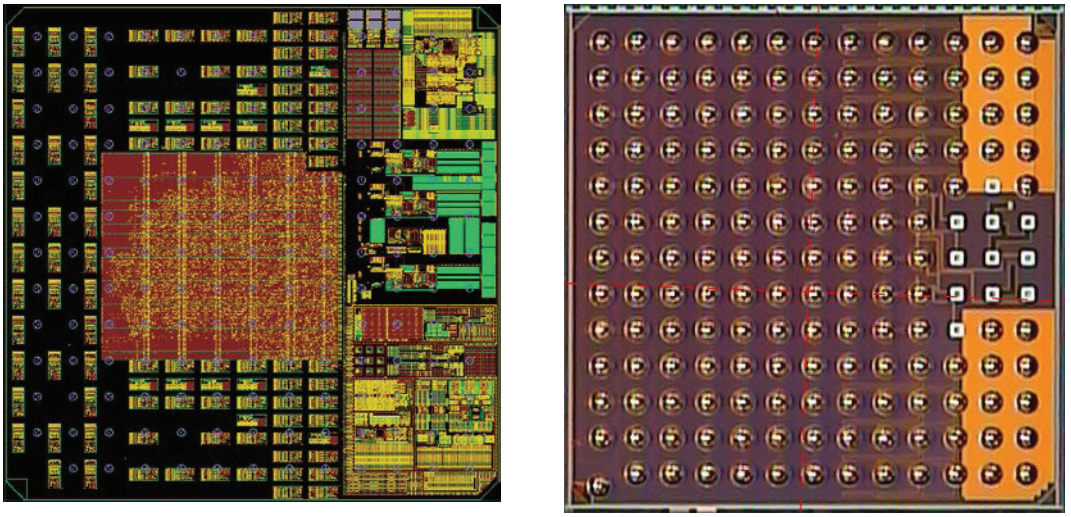

Figure 5: The layout of the GBT-SERDES (left) and the manufactured die (right) with flip-chip bonds attached.

3. Test results

A custom test system has been designed to characterize the chip in its different modes of operation. In this system, the GBT-SERDES is connected to a commercial optoelectronic transceiver. This in turn is coupled via optical fibre to a second transceiver connected to an FPGA in which the GBT protocol has been implemented. The FPGA thus acts as a data source and/or receiver to test the quality of the bidirectional link.

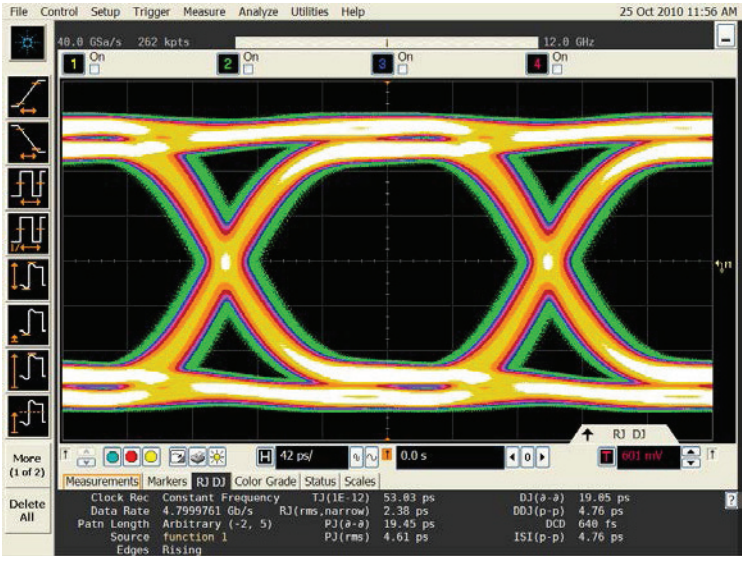

Figure 4: Eye diagram of the serial signal transmitted by the GBT-SERDES

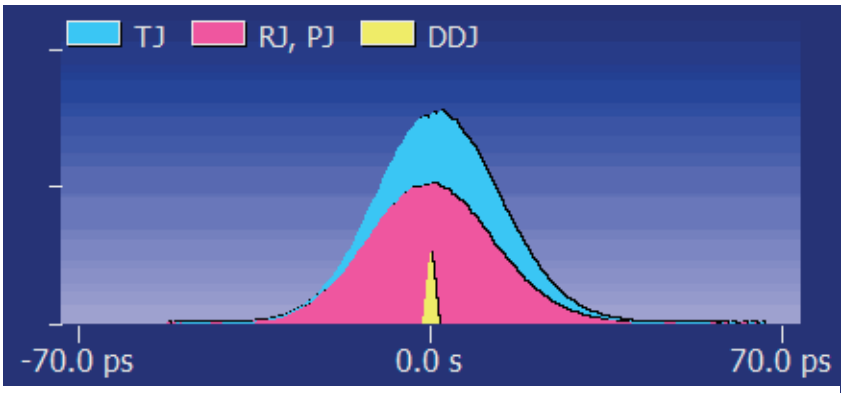

Figure 6: Jitter measured on a 40 MHz clock output of the GBT-SERDES, derived from the clock recovery from the received data

The signal quality from the serialiser has been measured by coupling the transmission fibre into a fast oscilloscope equipped with link diagnostic tools. Figure 5 shows the eye diagram of the data at full speed of 4.8 Gbit/s. The eye is clearly open and the total jitter measured is 53 ps. The transmitter was tested at higher frequencies, and was found to operate up to 6 Gbit/s. In the opposite direction, the clock recovery works well at 4.8 Gbit/s as shown by the jitter measured on one of the 40 MHz clock outputs of the GBT-SERDES in Figure 6. The jitter is about 70 ps peak-to-peak. However, the deserialisation was found to work error-free only up to 2.4 Gbit/s. Above this rate, errors appear frequently in the received data. The cause of this is a design error where a clock buffer was incorrectly placed and resulted in a hold violation of the data with respect to the 2.4 GHz clock driving the flip-flops of the shift registers in the deserialiser. This error will be corrected in the final version of the GBTX.

A bit-error-rate system was implemented in the FPGA to measure the quality of the GBT-SERDES transmitter link. Results of one particular test are shown in Figure 7, which shows the effectiveness of the FEC. Frame and bit error rates are measured as a function of both time and link attenuation, the latter increasing linearly with time. The attenuation was introduced using a programmable optical attenuator placed between transmitter and receiver. Two sets of results are shown, one using the FEC and one without. The results show that the error rate decreases with time (no errors detected) until the attenuation reaches about 15 dB when errors appear in the transmission without FEC. At this point, however, the FEC corrects wrong bits and provides error-free transmission beyond 16 dB of attenuation. The error rate then increases as the number of wrong bits is too high for the FEC to correct. A further measurement was made of the bit-error-rate of the transmitted data when the GBT-SERDES operates with the clock recovered from the received data. This will be the default operational scenario of the bidirectional GBTX link and a bit-error-rate of less than 9×10^{-16} was measured, limited by the measurement time. This measurement was made with an optical attenuation corresponding to the estimate for a system using the Versatile Link components [1] and indicates that the GBT will provide robust data transmission.

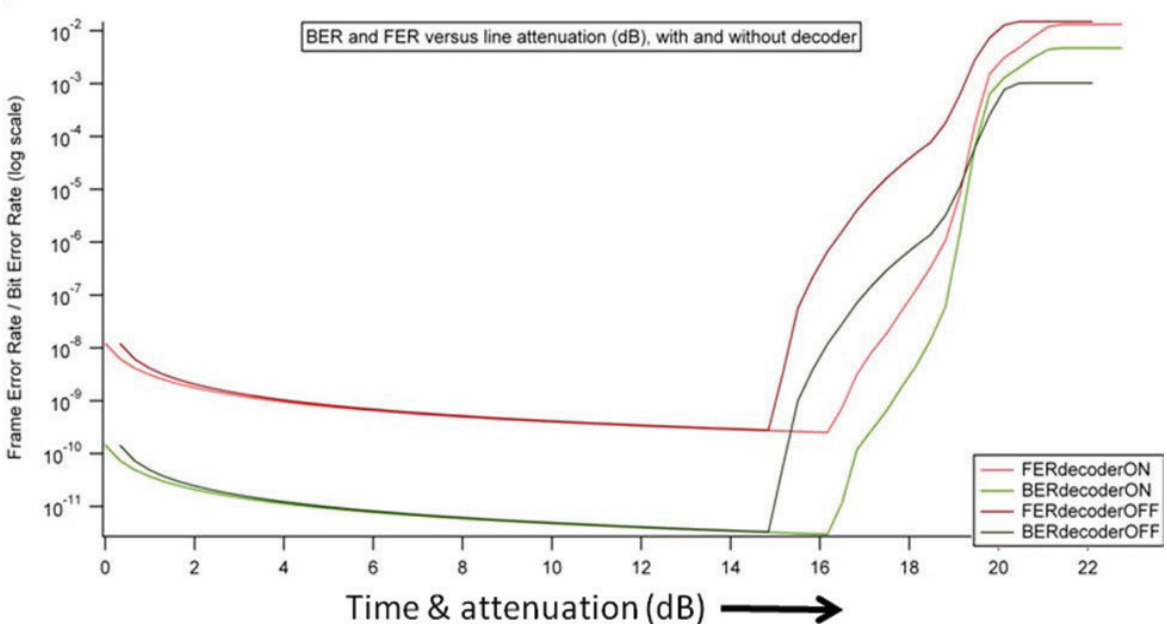

Figure 7: Frame (FER) and Bit (BER) error rates in the GBT-SERDES transmission as a function of optical attenuation between transmitter and receiver.

4. Conclusions and future work

The components of the GBT system have all been successfully prototyped. The GBT-SERDES has been designed to test the most important blocks for the final GBTX chip. Special attention has been paid to making the chip robust against radiation effects, both in the circuit design and in the data protocol. The chip has proven to be functional and works beyond the specifications for transmitting data. The recovery of the clock from the received data also functions well, but a design bug introduces errors in the received data. The GBT-SERDES is currently being tested for its resistance to single-event effects and the design of the full GBTX chip is underway incorporating the core blocks already tested in the GBT-SERDES.

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