Abstract

A Large Ion Collider Experiment (ALICE) at the Large Hadron Collider (LHC) at CERN is undergoing a major upgrade during which some of its sub-detectors are replaced with new ones and while others are equipped with new electronics to handle the expected higher lead-lead, proton-lead as well as proton-proton collision rates in the next running period (Run 3) foreseen to start in 2022. The upgrade requires, in part, new sub-detectors for the central system while other existing sub-detectors including those belonging to the Muon Spectrometer such as the Muon Trigger (MTR) which have been renamed to Muon Identifier (MID), will operate in continuous, trigger-less readout modes. At the center of the upgrade is a new approach based on the Common Readout Unit (CRU) developed to meet ALICE requirements. In particular, to share common interfaces, between 3 main sub-systems: the front-end electronics (FEE), the Online-Offline (O^2) computing system, and the timing and trigger system (TTS).

Due to the increase in data quantity, as well as the high collision and acquisition rates, typical methodologies are impossible to employ without massive efforts to expand processing capacity. Since the required scaling of the O^2 computing system can not keep up with the MID increased data flow, a new acquisition and processing paradigm has to be established. The CRU is a PCI Express 3rd generation FPGA processor board with a specific sub-detector feature called user logic. This user logic is a customizable component that can be used to extend the capabilities of the CRU firmware by providing additional features such as zero suppression, synchronization, and so on to meet the needs of any sub-detector in the ALICE experiment.

This research project provides a new approach to process the MID data based on a user logic prototype. The key aims of this thesis are to plan, build, evaluate and validate the user logic component. Innovative methods have been used to reduce the bandwidth produced by the sub-detector readout electronics, as well as adaptations to facilitate data handling later in the processing chain. Research procedures, simulations, evaluation methods, and applied methods are used to build a consistent prototype design. A laboratory testbench at NRF iThemba LABs equipped with the MID readout chain is used to test and validate the user logic prototype. The research findings and deliverables of this thesis will be used for postgraduate studies of other students, research, as well as a preliminary solution for a more complex user logic firmware.

Acronyms

ACORDE	-	A Cosmic Ray Detector
ADC	-	Analog-Digital Converter
ADULT	-	A DUaL Threshold
ALICE	-	A Large Ion Collider Experiment
ATLAS	-	A Toroidal LHC ApparatuS
CRU	-	Common Readout Unit
EMCal	-	Electromagnetic Calorimeters
FMD	-	Forward Multiplicity Detector
HMPID	-	High Momentum Particle Identification Detector
ITS	-	Inner Tracking System
LHC	-	Large Hadron Collider
LHCb	-	Large Hadron Collider beauty
LS2	-	Long Shutdown 2
MCH	-	Muon Chamber
MID	-	Muon Identifier
MTR	-	Muon Trigger
NRF	-	National Research Foundation
LABS	-	Laboratory for Accelerator-Based Science
FPGA	-	Field Programmable Gate Array
O^2	-	Online Offline
PHOS	-	Photon Spectrometer
PMD	-	Photon Multiplicity Detector
QGP	-	Quark-Gluon Plasma
SDD	-	Silicon Drift Detector
SPD	-	Silicon Pixel Detector
SSD	-	Silicon Strip Detector
TOF	-	Time Of Flight
TRD	-	Transition Radiation Detector
VHDL	-	VHSIC Hardware Description Language
ZDC	-	Zero Degree Calorimeter

Chapter 1

Introduction

Since the early days of its first employment in the 1960s, the distinctive qualities of Field Programmable Gate Arrays (FPGAs) [1] such as integration, flexibility, low power, and high bandwidth communication have allowed various new and critical approaches. FPGAs are the result of multiple generations of sophisticated technology, and they are often recognized as one of the major components utilized in the data acquisition of the detectors in high-energy physics experiments.

The ALICE detector at the Large Hadron Collider (LHC) at the European Organization for Nuclear Research (CERN) is undergoing a major upgrade during which some of its sub-detectors are replaced with new ones and while others are equipped with new electronics to cope with higher collision rates planned for the following years. The Muon Identifier (MID), one of the new sub-detector in ALICE is taking full advantage of today's FPGAs by changing the way data are processed in its readout chain using a customized user logic firmware. This user logic is written in the VHDL programming language and can implement multiple features tailored to the specific of the sub-detector.

This chapter begins with background information on the experiment and then introduces the ALICE detector. The project's goals are established, and an overview of the strategy used to achieve these goals is provided. The hypothesis, as well as the constraints and key contributions, are listed.

1.1 Background

1.1.1 ALICE experiment

CERN [2] is the world's leading laboratory for nuclear and particle physics research located on the border of Switzerland and France. CERN houses the LHC [3] which is about 100 meters below the surface and 27 kilometers in circumference. The LHC produces particle beams i.e. proton-proton (p-p), proton-lead (p-Pb), and lead-lead (Pb-Pb) at ultra-relativistic energies to create and study the characteristics of a highly dense form of matter reminiscent of the early Universe a microsecond after the Big Bang [4]. Spread along the LHC ring are four individual experiments positioned around the four collision points where the beams collide. As shown in Figure 1.1, one of these experiments is ALICE.

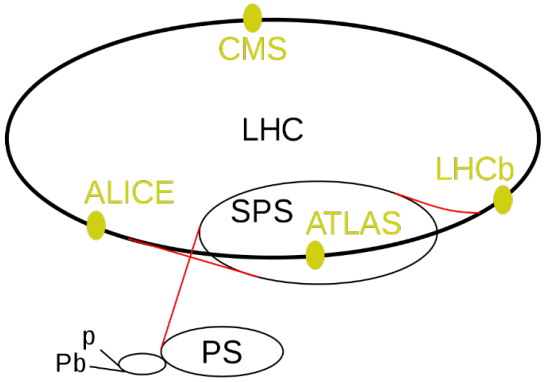

Figure 1.1: LHC ring with its four main experiments, ALICE, ATLAS, LHCb, and CMS as well as its super proton synchrotron (SPS), proton synchrotron (PS), and proton and lead accelerators [5].

For a few millionths a second after the Big Bang, the universe consisted of a hot plasma of deconfined elementary particles called quarks and gluons. A few microseconds later, this hot plasma known as the quark-gluon plasma (QGP) cooled further down to form hadrons, amongst others protons and neutrons, the fundamental building blocks of atomic matter. The conditions of the QGP can be created in high-energy heavy-ion collisions at the CERN LHC. ALICE is the detector at the CERN LHC dedicated to the study of this strongly interacting matter, the QGP, and its properties after recording data in pp and p-Pb collisions.

1.1.2 ALICE Detector

To reconstruct and identify a myriad of particles created in these collisions, the ALICE detector is shown in Figure 1.2, is using a set of 19 sub-detectors extended over a length of 26 m and 16 m in height and width, weighing over 10 000 tons. The sub-detectors encapsulated in a toroid magnet (L3) provide information about the mass, velocity, and electric charge of the particles. Each sub-detector is designed to study different aspects of the particles created in the collisions.

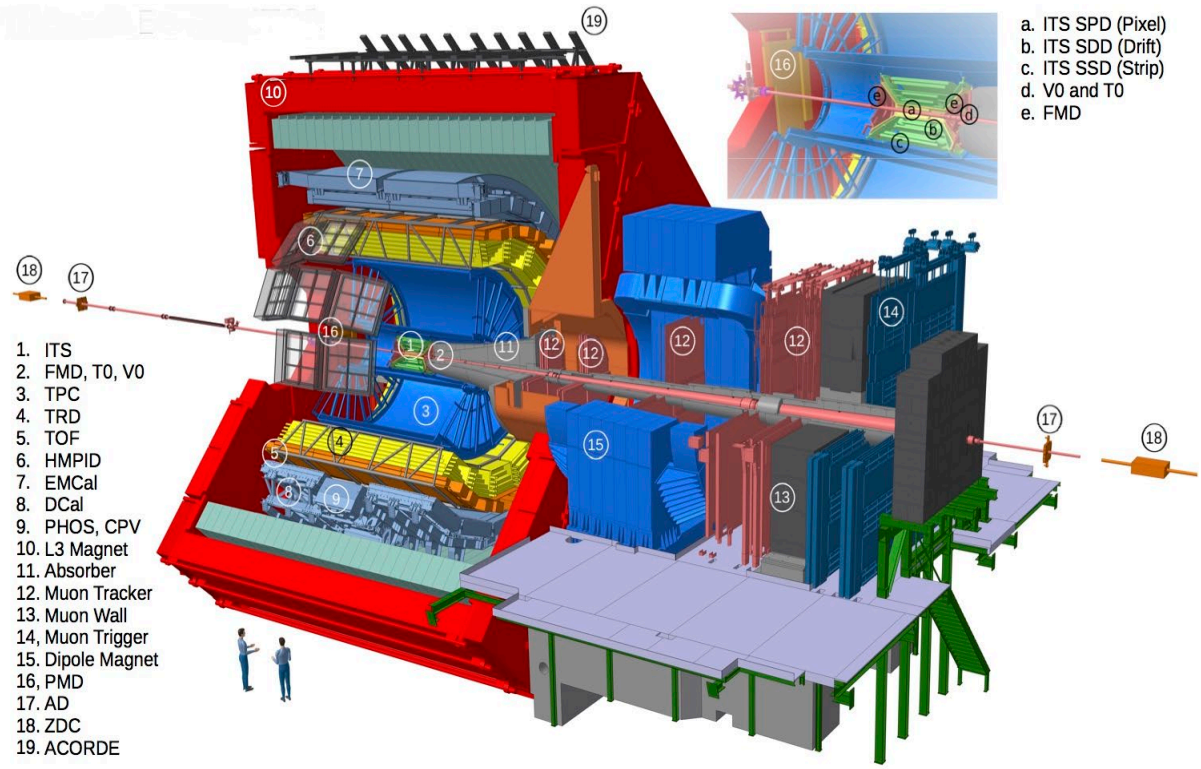

Figure 1.2: Schematic overview of the ALICE detector with its sub-detectors used during Run 2 [6].

The ALICE detector consists of two main regions: the central barrel region and the forward region known as the Muon Spectrometer.

The central barrel detectors are surrounded by a solenoid L3 magnet providing a field of 0.5 Tesla. At the center of the central barrel and closest to the beamline is the Inner Tracking System (ITS) composed of six layers of silicon detectors: Silicon Pixel Detector (SPD), Silicon Drift Detector (SDD), and Silicon Strip Detector (SSD). The ITS is encompassed by a cylindrical Time Projection Chamber (TPC), three-particle identification arrays of Time of Flight (TOF), a ring imaging of Cherenkov High Momentum Particle Identification Detector (HMPID), and a Transition Radiation Detector (TRD). The surface layer contains the Electromagnetic Calorimeters (EMCal), and the Photon Spectrometer (PHOS). Small-scale sub-detectors used for global event identification and triggering such as the Zero Degree Calorimeter (ZDC), Photon Multiplicity Detector (PMD), Forward Multiplicity Detector (FMD), T0, and V0 are located on either side of the interaction point. On the three upper outside faces of the solenoid L3 magnet is A Cosmic Ray Detector (ACORDE). It consists of an array of plastic scintillator counters and provides accurate information about cosmic ray events.

The Muon Spectrometer is designed to measure muon production from the decays of quarkonia, low mass vector mesons, heavy-flavor hadrons, and electroweak bosons [7]. The Muon Spectrometer has an angular acceptance of 171˚- 178˚, corresponding to the pseudorapidity region $-4.0 < \eta < -2.5$. The Muon Spectrometer covers a total length of $\simeq$ 17 m and it is composed of the following components: front-absorbers to filter all particles except muons coming from the interaction point, a large dipole magnet, high-resolution Muon Tracking Chambers (MCH), a 120 cm thick iron wall (Muon Filter), and a Muon Trigger (MTR).

1.1.4 Muon Trigger

The MTR system is equipped with a configurable threshold to provide trigger signals for selecting events of interest and discarding events with only low momentum muons (p<4 GeV/c). As illustrated in Figure 1.5, the muon trigger is based on 72 single-gaps Resistive Plate Chamber (RPC) detectors, arranged in 2 stations of 2 chambers, each at a distance of about 16 m and 17 m from the interaction point, respectively. Each RPC consists of two planes, a positively charged anode, and a negatively charged cathode, both made of very high resistivity plate plastic material and separated by 2 mm of a gas mixture of Ar, CH2F4, C4H10, and SF6. Once a charged particle such as a muon passes through the chamber, it knocks electrons out of the gas atoms. These electrons in turn hit other atoms causing an avalanche of electrons. Since the electrodes are transparent to the electrons, these are instead picked up by external metallic strips after a small but precise time delay. The combination of hit strips firing gives a quick measure of the muon momentum, which are read-out by the front-end electronics, known as A DUaL Threshold (ADULT) cards [8]. The signals from the ADULT cards are then propagated to the readout electronics based on three programmable circuits (local, regional and global) working in sequential mode at 40 MHz, to make immediate decisions about the validity of the data. The ADULT electronics were initially developed for streamer mode operation with a gas mixture for the LHC Run 1 (2010-2012). A few years later, a maxi-avalanche operation mode was introduced for the LHC Run 2 (2015-2018), where the signal amplitude was smaller than in the streamer mode, but still compatible with the minimum threshold of 7 mV set in the ADULT cards. The sub-detector planes are mounted on a mechanical frame on rail support that can be moved to allow access to the chambers for maintenance purposes.

The MTR will be called Muon Identifier (MID) after the upgrade for Run 3. Technical details concerning the new MID readout chain are described in chapter 2, as the work described in this thesis is focused on this specific sub-detector.

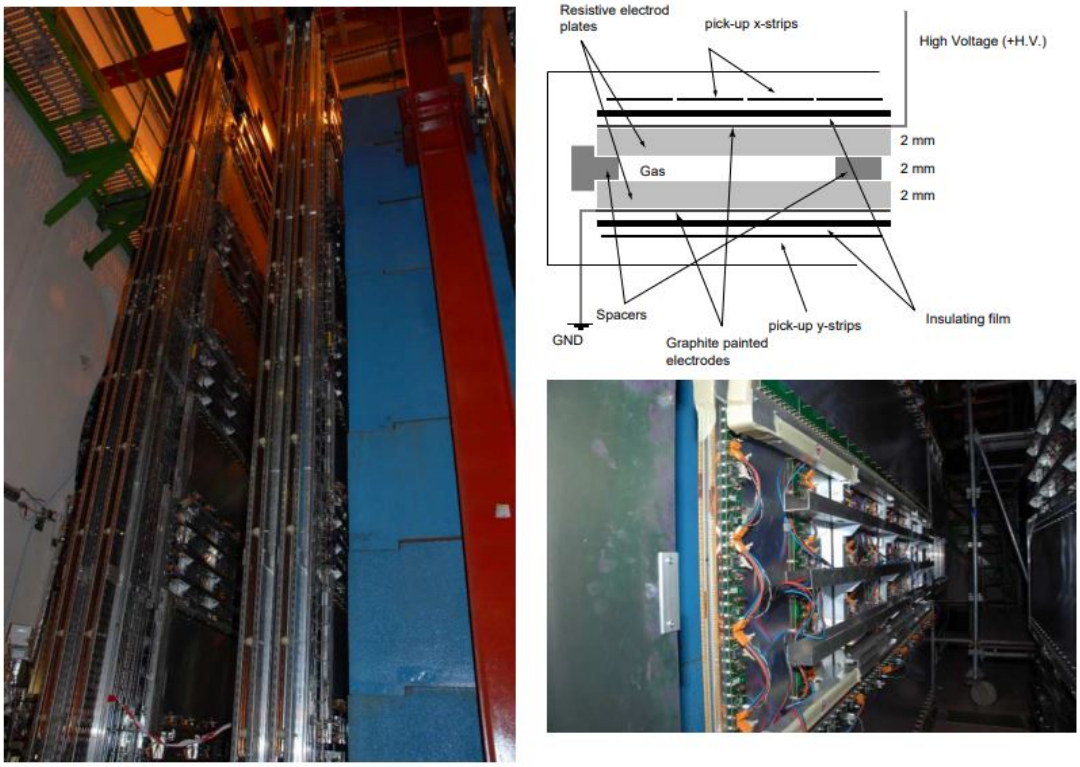

Figure 1.5: Left: View of the two trigger stations positioned behind the muon filter. Right-top: schematic view of the cross-section of the RPC. Right-bottom: an independent RPC module with ADULT electronics

1.2 LHC Run 3

Based on data collected in Run 1 and 2 (~10 petabytes of raw data), ALICE is the leading heavy-ion experiment in the world and is quickly expanding the knowledge gathered in previous experiments all over the world. The LHC is currently going through three years of a planned second Long Shutdown called (LS2) which started at the end of 2018 to prepare for Run 3. In line with the LHC upgrade, the ALICE detector is undergoing a major upgrade. This upgrade addresses the challenge of reading out lead-lead collisions at the rate of 50 kHz, proton-proton, and proton-lead at 200 kHz and higher. At the center of the ALICE's upgrade strategy is a high-speed readout approach based on a Common Readout Unit (CRU). The CRU has been developed for detector data readout, concentration, reconstruction, multiplexing, and data decoding onto the online-offline (O^2) computing system.

Many of the proposed physics observables require a change in the data-taking strategy, moving away from triggering a small subset of events to continuous online processing and recording of all events. To achieve these goals, the ALICE detector is being upgraded in such a way that all interactions will be scrutinized with precision. The upgrade entails the replacement of some sub-detectors with new ones, making use of new technologies while most others are equipping their detectors with new electronic systems.

The LHC Run 3 was planned to start in the middle of 2021 onwards but has been postponed to March 2022 due to the global pandemic [9].

1.2.1 The upgrade: Muon Trigger to Muon Identifier

For the past 10 years since the beginning of the LHC Run 1, the selection of single muon and di-muon events with a maximum trigger rate of 1 kHz was provided by the MTR. However, to cope with the increased luminosity of the LHC during Run 3, this current trigger strategy is no longer sufficient. The upgrade trigger strategy described in [10] does not require a muon trigger, since all events of interest will be read out upon the interaction trigger before online selections. For this reason, as part of the upgrade, the MID will play the role of providing the muon identification.

1.3 Problem statement

Several issues concerning the readout arose during the transition from MTR to MID. These issues [11] were observed throughout a preliminary series of tests conducted on the MID readout chain at Subatech, Nantes in France (where the readout electronics are developed). The upgraded system showed limitations when running without data pre-analysis performed at the CRU firmware level. Among these limitations are large data rate, desynchronization of data, lack of hardware resources and, many other minor issues related to the data format transmitted to the O^2 computing system. All these limitations had to be addressed urgently.

1.3.1 Large data rate

In the triggerless readout chain, all events are read out continuously. This results in a bandwidth of 3.2 Gbps generated by each data link of the chain. This large amount of data is a problem for the O^2 computing facility to conduct data processing concurrently without data compression already at the CRU firmware level. The readout electronics data links are based on an 80-bit frame transmitted continuously at 40 MHz (25 ns), which corresponds to the LHC bunch crossing interval. The bunch crossing interval is the period between bunches of particles crossing each other in the LHC. In other words, it is the amount of time between colliding bunches.

On the other hand, as previously mentioned, one of the primary goals of the ALICE detector upgrade is to read out lead-lead collisions at 50 kHz (20 μs), proton-proton, and proton-lead collisions at 200 kHz (5 μs). This indicates that out of 3.2 Gbps, just 4 Mbps during lead-lead collisions and 16 Mbps during proton-proton and proton-lead collisions are worth analyzing and might turn out to be valuable collision data. The remaining data are meaningless and must be suppressed. Retaining these data in the memory results in inefficiency and waste of memory.

1.3.2 Desynchronization of data

The data obtained from all readout electronics occur simultaneously, at fixed periods, and are transmitted to the CRU over a wide set of optical links. However, differing transmission delays result in the data from the various links losing synchronization when transmitted to the O^2 computing system. Therefore, cause more problems further along the chain at the synchronous and reconstruction levels.

1.3.3 Lack of hardware resources

The O² computing system is capable of handling the data rate from a single regional crate at the expense of 2 core processors. Attempting to use 1 core to decode a single regional crate leads to irreversible data loss. Hence, it takes 2 core processors to decode a single regional crate. However, the computer [12] used in the readout chain contains 20 core processors. To decode data from the entire readout chain, that the computer would need 32 core processors, not to mention any additional cores required to perform further processing of the decoded data. As a result, processing data from the complete front-end system is unfeasible on a single machine. The architecture of the MID readout chain is described in Chapter 2.

1.4 Research aim

The ALICE collaborators participating in the MID project are searching for new ways to process raw data. Many alternatives have been suggested, but most of them entail significant improvements in the existing readout chain. Some of the improvements require changing the algorithm implemented in the O² processing to cope with the large data rate, acquiring additional CRUs, and core processor computers to process data from the entire readout electronics. A thorough analysis review revealed that the most efficient and cost-effective solution is to take advantage of the existing high-speed FPGA incorporated in the CRU by designing a customized user logic firmware to meet the requirements of the readout chain.

The user logic is a specific sub-detector component, that can be implemented in the CRU firmware through a specific compilation. It is developed by the sub-detector teams and can perform low-level data processing and other additional features before forwarding data to the O² computing facility for further analysis. This research aims to improve the way data are processed in the MID readout chain using a customized user logic firmware before the start of the LHC Run 3.

1.5 Objectives

The research aim stated above is achieved through the following objectives:

- Review and analyze different components of the readout chain
- Select the best user logic algorithm
- Identify and subsequently remove meaningless data
- Receive timing and trigger information
- Synchronize essential data before performing the correct analysis
- Reformat data transmitted from the readout electronics
- Transmit data in the order required by the O² computing facility
- Handle errors identified in the readout electronics data
- Successfully validate the user logic simulation tests
- Successfully validate the user logic hardware tests
- Make recommendations for future improvements

1.6 Hypothesis

This study offers the possibility of designing and developing a stable and reliable user logic firmware that can improve the way data are processed in the MID readout chain. This can be achieved by developing an algorithm based on systems requirements. However, the difference in protocol between various systems of the readout chain makes it complex and can be time-consuming. The main questions to be considered are whether a user logic prototype can be designed and tested to meet the requirements of the MID readout chain on time before the start of the commissioning phase of the MID-sub-detector, and whether or not this prototype can be used to develop a realistic user logic capable of processing data from the entire readout chain, considering hardware and software restrictions of the approved FPGA.

1.7 Delineation

This thesis is limited to the design and development of the user logic firmware prototype capable of pre-analyzing data from 2 regional links of the MID readout chain. This research analyses in detail different systems used in the readout chain and improves the way data are processed in the CRU. The proposed scheme is developed after intensive research and a good understanding of the ALICE detector. Hence, the incorporation of the user logic component into the existing CRU firmware is done through conformance with established requirements and practice. Additionally, important technical decisions such as hardware, communication protocols, design tools, programming languages, and most relevant resource usage limit of the research in question have been established before the beginning of the research.

1.8 Collaboration and main contributions

In South Africa, the National Research Foundation (NRF) iThemba Laboratory for Accelerators Based-Science (LABS) is part of the ALICE Collaboration and contributes to the ALICE Muon Spectrometer upgrade, in particular the MID. In collaboration with the Cape Peninsula University of Technology (CPUT) and the University of Cape Town (UCT), NRF iThemba LABS is responsible for conducting research and developing the CRU user logic firmware for the MID readout chain, including setting up a testbench data acquisition readout chain and the maintenance thereof.

The user logic project started in early 2018, with early research described in this paper [13]. Due to the rapid evolution of the ALICE CRU software and firmware projects, a complete modification to the initial project was necessary. In 2020, a new design and development of the user logic based on realistic data acquisition requirements and availability of relevant readout components led to this study. Together with Dr. C.Renard (expert in the readout electronics at Subatech in Nantes, France), the requirements to process data from 2 data links of the readout chain were established. To keep track of the rapid evolution of the CRU software and firmware, rigorous consultations and discussions took place with Dr. F.Costa (ALICE CRU software expert at CERN) and Dr. O.Bourrion (ALICE CRU firmware developer at the University of Grenoble, France). For what concerns the MID O^2 requirements, Dr. D.Stocco (MID O^2 expert at Subatech, France) was the main contact and source of information. His input was required since the outcome of this research may affect the way data will be handled at the next phase of the data acquisition chain. As such, he was instrumental in setting up some additional requirements and constraints to facilitate the readability of the user logic output data.

Overall, the design and development of the ALICE CRU user logic firmware prototype for the MID readout chain are provided by the Electrical Engineering department at CPUT with support from various collaborators using facilities provided by the NRF iThemba LABS and advanced technology.

1.9 Methodology

The research methods that are utilized for the development of this thesis are:

- **Literature review:** since in many cases the written literature is not available on the readout chain. The information was gathered by reading technical specification papers, IEEE published journals, conferences, interviewing specialist engineers in the data acquisition chain, and through the World Wide Web.

- **Prototyping**: Intel Quartus Pro 18.1 [14] is the main software environment recommended and used to design and develop the user logic. For this thesis, two different prototyping approaches are implemented. The rapid throwaway method involves exploring ideas by quickly developing a prototype based on preliminary requirements which are then revised through simulation test feedback. Once validated, the evolutionary approach is then introduced. This method uses a continuous, working prototype that is refined after each iteration of hardware test feedback.

- **Simulation tests:** ModelSim [15] is the simulation software used to verify the functionality of the user logic algorithm by analyzing each component of the model. A more advanced simulation is performed by merging the CRU firmware simulation files as well as the MID readout electronics firmware simulation files into a single testbench for more efficient and accurate results.

- **Hardware tests**: a readout testbench facility available at iThemba LABS is developed for practical work. Expected tests for conformance include testing of the user logic prototype using a fully-functional MID readout testbench set-up capable of emulating the same events generated by the main ALICE MID readout chain at CERN.

- **Data collection:** simulation and hardware tests are conducted to collect real data coming in and out of the user logic firmware. A comparison between the input and output data is done to achieve an effective assessment of the user logic algorithm.

1.10 Thesis outline

Chapter 2

This chapter looks deeper into the MID readout chain and its most important components and protocols, particularly the CRU, which will serve as the interface between the on-detector electronics and the O^2 computing system.

Chapter 3

This chapter explains in detailed the CRU firmware.

Chapter 4

tests the performance of the prototype of the conceptual design previously presented in relevant fields of metric for a project of this nature.

Chapter 5

The results obtained, the performance of the prototype, the key findings, and the thesis deliverables are summarized in this chapter. The recommendations for possible future work and the extension of the project are also discussed in this chapter.

Chapter 6

This thesis is concluded by a comparison of the project's defined goals and the results of the user logic prototype. Additionally, it addresses, the remaining work that needs to be completed. This includes features that are yet to be developed as well as potential recommendations.

Appendix A

This appendix describes the software tool package used for IED configuration and all ABB 670 series function blocks that were used to build the reverse blocking protection scheme. These blocks are described in different categories which are based on their functions.

Appendix B

This appendix describes the software tool package used for IED configuration and all ABB 670 series function blocks that were used to build the reverse blocking protection scheme. These blocks are described in different categories which are based on their functions.

Appendix C

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References

[1] "Intel® FPGAs Resource Center," Intel, https://www.intel.com/content/www/us/en/products/details/fpga/resources/overview.html.

[2] O. S. B. e. al., "CERN," LHC design report v.1: The LHC main ring. CERN-2004-003-V1, 2004.

[3] L. E. a. P. B., " LHC machine," *JINST,* 2008.

[4] P.Giubellino, "The big bang in the Lab," in *TechFest*, 2015.

[5] "LHC ring," Available: https://en.wikipedia.org/wiki/Large_Hadron_Collider. [Accessed 09 05 2021].

[6] "CERN Document Server", https://cds.cern.ch/record/2628419/plots. [Accessed 09 05 2015].

[7] Zaida CONESA DEL VALLE, "Performance of the ALICE muon spectrometer. Weak boson production and measurement in heavy-ion collisions at LHC," Zaida CONESA, Nantes, 2007.

[8] P. Dupieux(Clermont-Ferrand U.), "A new front-end for better performances of RPC in streamer mode," in *ALICE Collaboration*, 2003.

[9] A. Schaeffer, "CERN Accelerating science," 27 November 2020, Available: https://home.cern/news/news/accelerators/new-schedule-cerns-accelerators-and-experiments.

[10] ALICE Collaboration, "Upgrade of the Readout & Trigger System," CERN-LHCC-2013-019, 2014.

[11] D. Stocco, Interviewee, *Personal communication.* [Interview]. 16 August 2019.

[12] F. Costa, "Assessment of the ALICE O2 readout servers," *ALICE Collaboration,* p. https://indico.cern.ch/event/773049/contributions/3474356/attachments/1933568/3212521/Assessment_of_the_ALICE_O2_readout_servers_final.pdf.

[13] Nathan Boyles, "User Logic Development for the Muon Identifier Common Readout Unit for the ALICE Experiment at the Large Hadron Collider," *Instrumentation and Detectors,* no. arXiv:2104.05476, 2021.

[14] Intel, *Intel® Quartus® Prime Pro Edition,* https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug-qpp-programmer.pdf, 2020.

[15] Intel, *ModelSim® - Intel® FPGA Edition Simulation,* https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug-qpp-programmer.pdf.

[16] "ALICE Collaboration," https://home.cern/science/experiments/alice. [Accessed 09 05 2021].

[17] Arnaldi, "Design and performance of the ALICE muon trigger system," in *Nucl.Phys. B Proc.Suppl. 158 (2006) 21-24*, Korea University, Seoul, 2005.

[18] A. Collaboration, "Pion, Kaon, and Proton Production in Central Pb-Pb Collisions," *PHYSICAL REVIEW LETTERS,* pp. 1-2, 2012.

Chapter 2

Muon identifier readout chain

As discussed in the previous chapter, the approach taken by ALICE is to read out all pb-pb events at an interaction rate of 50 kHz. The objective behind the upgrades is to significantly improve vertexing and tracking capabilities at low transverse momentum. In line with the ALICE upgrades, the MID readout chain is also being upgraded to support continuous readout operation after the LS2. This upgrade entails:

- New RPCs;
- New front-end electronics;
- New readout electronics

This chapter deals with the description of the MID readout chain and is organized as follows. Section 2.1 gives a brief overview of the readout chain. The RPCs upgrade is described in section 2.2, while the front-end and readout electronics upgrades are discussed in sections 2.3 and 2.4. The CRU is the heart of the readout chain, and its hardware architecture is discussed in section 2.5. The timing and trigger, online-offline computing, and detector control systems are discussed accordingly in the following sections.

2.1 Overview

The readout chain block diagram is shown in Figure 2.1. The readout chain consists of 21 000 strips connected to 72 RPC detectors spread over multiple Front-End Electronics Rapid Integrated Circuit (FEERIC) cards equipped with one or two ASICs [1]. The strip pattern signals from the FEERICs are propagated to the readout electronics, acting as the readout interface and in charge of the first stage of the trigger decision. The readout electronics are mounted on the upper gangways a little further away from the stations, where the radiation is low. The beam collisions will produce a lot of radiation in the area around ALICE in the cavern, therefore the readout electronics regional cards are equipped with Gigabit Transceiver (GBT) radiation hardening to operate properly. The CRUs are the key components of the chain, they combine and multiplex data from multiple readout electronics cards as well as timing and trigger information generated from the Central Trigger Processor (CTP) via the Local Trigger Unit (LTU) before transmission to the O² computing facility for processing and storage. The CRUs are mounted in computers housed in the intermediary computer room, called the counting room, away from the ALICE cavern and thus do not require radiation hardening, as is the case for the readout electronics. These computers can be reached over the network from the main Detector Control System (DCS). The DCS manages the readout chain by sending commands and monitoring the system. Experimental data are moved from the FLP node to the O² computing system for processing and storage.

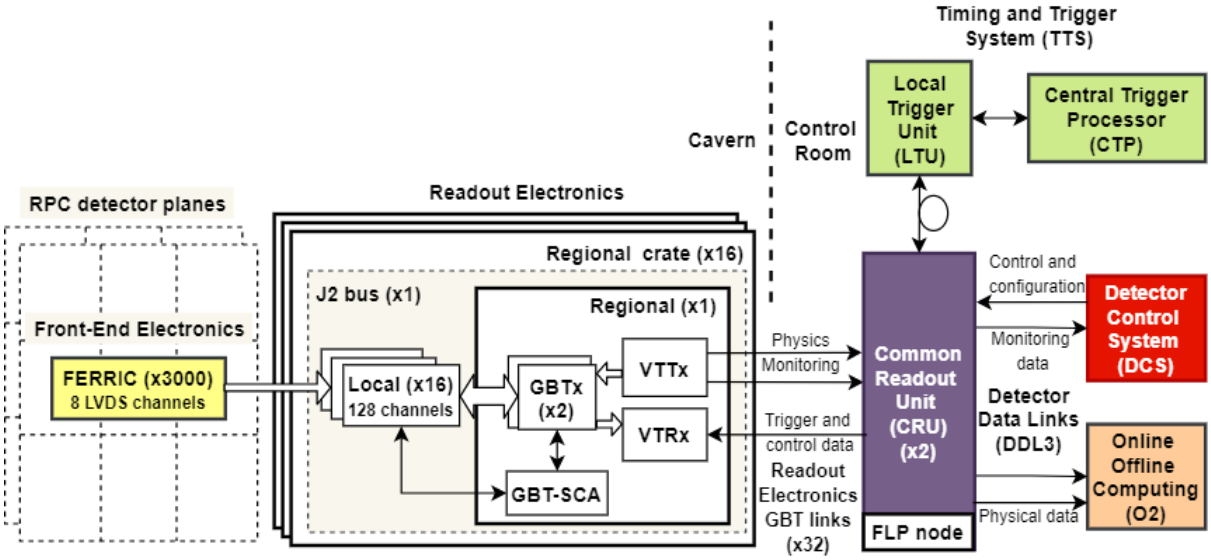

Figure 2.1: MID readout chain architecture

2.2 RPC detectors

In the ALICE cavern, three distinct forms of RPC are installed. They refer to long, short, and cut forms, respectively (Fig.2.3). The beam pipe is accommodated by the short-cut forms. The current RPCs are constructed with 2 mm wide gas gaps, 2 mm thick High-Pressure Laminate (HPL or bakelite) resistive electrodes, and polyamide insulation layers. The readout strips are made of copper and have three different pitch options: 1, 2, or 4 cm. Both RPCs have one collection of readout strips on each hand. The strips on either side of the RPCs are orthogonal to one another. In comparison to the dipole motion

on charged-particle tracks, the vertical strips that have (y) hits are referred to as non-bending and the horizontal strips that have (x) hits are referred to as bending.

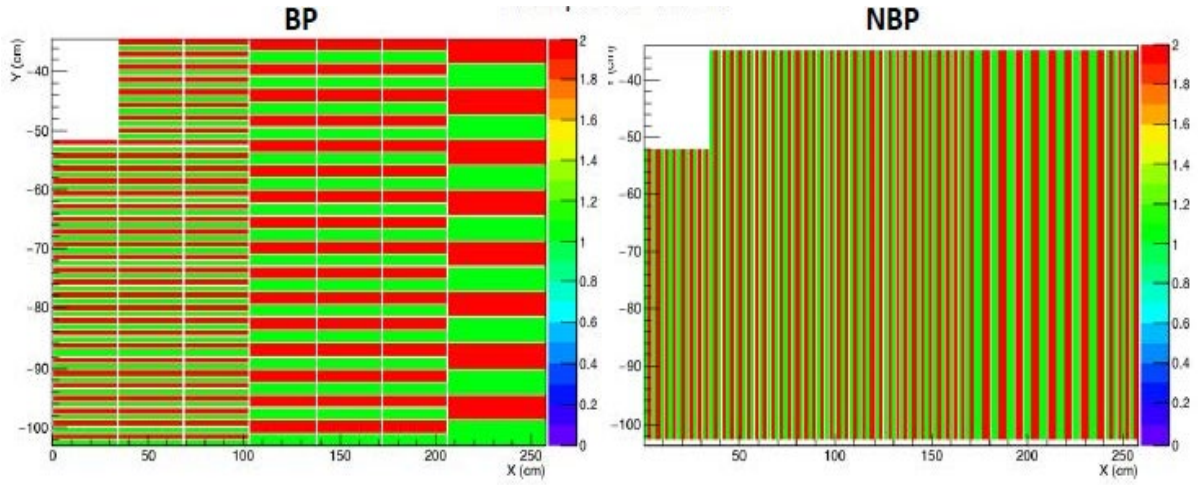

Figure 2.2: RPC strip patterns

As described in [2], the amount of RPC hits in pb-pb collisions is expected to exceed the highest counting rate of about 10 Hz/cm² up to 90 Hz/ cm². This is marginally similar to the maximum rated capacity of the detector in the maxi-avalanche mode during the LHC Run 2. This rise would also hasten the aging of the gas gaps, which will hit the end of their projected lifespan long before the end of Run 3, necessitating the replacement of certain gas gaps and other affected components.

These upgrades are distributed among three institutions. The Puricelli factory in Costa Masnaga (Italy) is responsible for redesigning the bakelite resistive electrodes, which feature a smoother surface for the bakelite used on the presently installed RPCs, the General Tecnica in Colli (Italy) is responsible for manufacturing the gas gaps for the new RPCs and, the National Institute for Nuclear Physics (INFN) in Torino (Italy) is responsible for checking and testing the performance of the new RPCs with cosmic rays. The installation of the new RPCs in the cavern is expected to start from July 2021, with the intent of installing 2 RPCs per day. In case of failure to meet this deadline, the MID will operate with the existing RPCs during Run 3 until the new RPCs are ready.

2.3 Front-End electronics

The RPC ADULT electronics have been replaced by the new FEERIC and unlike the ADULT, it performs amplification of analog signals from the RPCs. The FEERIC is an 8-channel ASIC, which uses low-cost AMS 0:35mm CMOS technology developed by the Laboratory of Physics Clermont-Ferrand. It is made up of a trans-impedance amplifier stage, a zero-crossing discriminator to limit time walk effects, and a one-shot to prevent retriggering during 100 ns and LVDS drivers. Table 2.1 summarizes the main specifications, and requirements of the FEERIC ASIC. In contrast to the ADULT card thresholds, which were set using an analog voltage distribution of just one threshold value per RPC, the FEERIC card thresholds would be set wirelessly during the LHC Run 3. Their values will be assigned to fine-tune the threshold based on the local RPC efficiency while minimizing operating high voltage.

The technology selected to accomplish this task is the ZIGBEE protocol [3]. It is a wireless technology established as an open universal norm to meet the special requirements of ultra-low-cost, low-power wireless IoT networks based on the IEEE 802.15.4 physical radio and works in unlicensed bands such as 2.4 GHz. The ZEGBEE is incorporated on the Atmel SAMD21 microcontroller [4] and the program is based on Arduino libraries (I2C, SD cards, and Xbee module). This is then put onto a printed circuit board called the Xbee cards. The master cards are connected to the DCS PC using ethernet, and the ZIGBEE (wireless) protocol is used to communicate from master to nodes.

Table 2.1: Requirements of the FEERIC ASIC [1]

Feature	Value or type
pulse polarity	positive or negative
# of channels	8
power consumption per channel	< 100 mW
input impedance	< 50 W
dynamic range	20 fC < q < 3 pC
time resolution	< 1 ns
time walk	< 2 ns
one-shot	100 ns
output format	LVDS
signal shape	square pulse 23±3 ns

As previously mentioned, the charge delivered within the gas gaps must be lowered to minimize aging and improve rate capabilities. This is achieved by operating RPCs with the same gas mixture but at a lower gain, in conjunction with the FEERICs, which perform amplification of the analog signal before discrimination. Hitherto 2384 + 336 spares FEERIC cards and 26 Xbee cards have been manufactured and installed in the ALICE cavern. The installation and commissioning of all FEERIC and Xbee cards concluded in July 2019.

2.4 Readout electronics

To cope with the new readout rates, the local and regional readout cards have been redesigned. Since the triggering functionalities are abandoned, a more streamlined approach has been introduced. The hardware implementation of the regional and local card is almost identical, minimizing the design and development effort by re-using the same hardware and altering the FPGA firmware. The global crate has been replaced by a new regional crate.

As shown in Figure 2.3, the readout electronics are divided into 16 vertical regions (8 on the left and 8 on the right side of the plane). Each vertical region is read out by a single regional crate. Each contains a backplane bus card called the J2 card, which connects to a single regional card and up to 16 local cards.

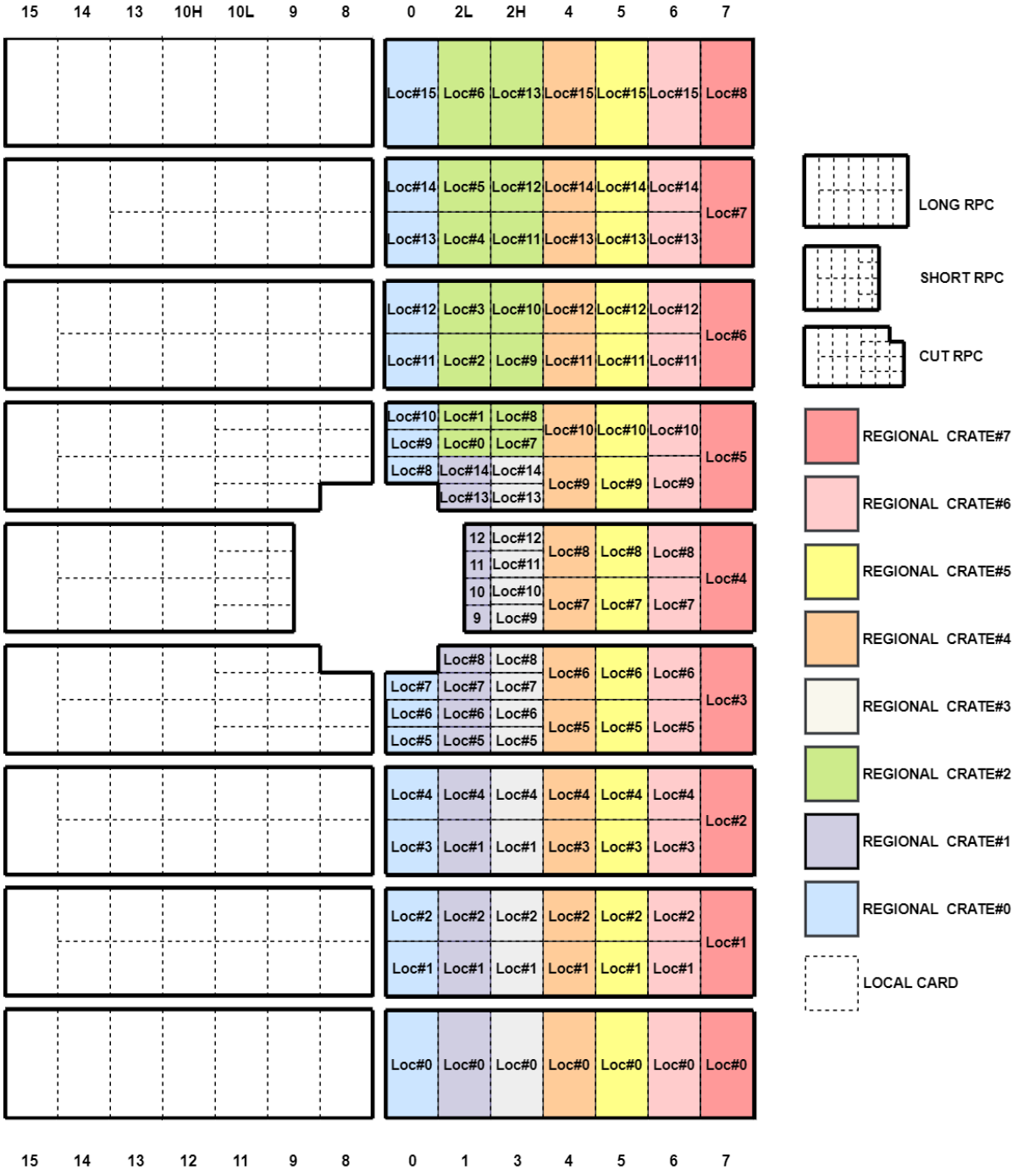

Figure 2.3: Geometry of the readout electronic

2.4.1 Local card

For every bunch crossing, the local card receives binary data from LVDS channels, which indicates whether the corresponding channel has been struck or not. The local card is equipped with 16 LVDS input connectors (32 pins, for both the BP and NBP). It is embedded with the Intel MAX 10 FPGA (10M50DCF484C7G) [5] its firmware is described here [6].

2.4.2 J2 bus card

The J2 bus card serves as an interface between the regional crate and the local/regional cards in terms of power, and it also serves as an interface between the local and regional cards in terms of data transfer. The J2 bus card has a 4-bit dip switch for assigning a specific identification to the regional crate, as well as three LEDs for monitoring the voltages (2.5V, 3.3V, and 5V) supplied to the regional and local cards.

2.4.3 Regional card

The regional card collects data from up to 16 local cards using the GBT protocol, which is discussed in the next section. Similar to the local card, the regional card is incorporated with the same Intel MAX 10 FPGA. However, unlike the local card, it is equipped with two bi-directional GBT optical links allowing transmission and reception of data to/from the CRU. The implementation of 2 GBT optical links per regional card enables complete regional crate data transfer. The firmware implemented in the regional card FPGA is a slightly modified version of the local card firmware, which is also described in [6].

2.4.4 Event data formats

Events are stored in the local and regional card multi-buffers for each trigger. The multi-event buffer in the local card carries strip patterns, therefore it is larger than the regional card. The event data formats of the local card and regional card are shown in Tab.2.2 and Tab.2.3 accordingly.

Table 2.2: Local event format [6]

Coding of SOx, EOx, RESET, CALIBRATE Event in LOCAL	*Bits*	*Coding of PHY, ORB Event in LOCAL*	*Bits*	*Coding of self-triggered DATA Event in LOCAL*	*Bits*
START BIT (always '1')	1	START BIT (always '1')	1	START BIT (always '1')	1
CARD TYPE (always '1'=LOCAL)	1	CARD TYPE (always '1'=LOCAL)	1	CARD TYPE (always '1'=LOCAL)	1
LOCAL BUSY ('0'=OK; '1'=FIFO full)	1	LOCAL BUSY ('0'=OK; '1'=FIFO	1	LOCAL BUSY ('0'=OK; '1'=FIFO full)	1
LOCAL DECISION (tracklet)	1	full)	1	LOCAL DECISION (tracklet)	1
ACTIVE ('0'=OFF; '1'=ON)	1	LOCAL DECISION (tracklet)	1	ACTIVE (always '1'=ON)	1
REJECTING ('0'=OFF; '1'=ON)	1	ACTIVE ('0'=OFF; '1'=ON)	1	REJECTING (always '0'=OFF;)	1
MASKED ('0'=OFF; '1'=ON)	1	REJECTING ('0'=OFF; '1'=ON)	1	MASKED ('0'=OFF; '1'=ON)	1
OVERWRITED ('0'=OFF; '1'=ON)	1	MASKED ('0'=OFF; '1'=ON)	1	OVERWRITED ('0'=OFF; '1'=ON)	1
	1	OVERWRITED ('0'=OFF; '1'=ON)	1		1
SOx	1	SOx (always '0')	1	Always '0'	8
EOx	1	EOx (always '0')	1		
PAUSE (always '0')	1	PAUSE (always '0')	1		
RESUME (always '0')	1	RESUME (always '0')	1		
CALIBRATE	1	CALIBRATE (always '0')	1		
PHY (ignored)	1	PHY	1		
RESET	1	RESET (always '0')	1		
ORB	1	ORB	1		
LOCAL bunch counter	16	LOCAL bunch counter	16	LOCAL bunch counter	16
LOCAL board position in Crate (0-15)	4	LOCAL board position in Crate (0-15)		LOCAL board position in Crate (0-15)	
Status: "0xF"	4	Always '0'		Data: detector plane(s) (1 bit / plane)	
Status: Mask registers (SOx='1'|EOx='1') Data: all strip patterns (not masked) [(X4, Y4), (X3, Y3), (X2, Y2), (X1, Y1)]	32*4	N/A	0	Data: Only masked strip pattern(s) [(X4, Y4), (X3, Y3), (X2, Y2), (X1, Y1)]	32*i
Total number of bits		Total number of bits	40	Total number of bits	8*bc
Bunches needed to send		Bunches needed to send	5	Bunches needed to send	9 - 21

Table 2.3: Regional event format [6]

Coding of SOx, EOx, RESET, CALIBRATE Event in REGIONAL	*Bits*	*Coding of PHY, ORB Event in REGIONAL*	*Bits*	*Coding of self-triggered DATA Event in REGIONAL*	*Bits*
START BIT (always '1') CARD TYPE (always '1'=LOCAL) LOCAL BUSY ('0'=OK; '1'=FIFO full) LOCAL DECISION (tracklet) ACTIVE ('0'=OFF; '1'=ON) REJECTING ('0'=OFF; '1'=ON) MASKED ('0'=OFF; '1'=ON) OVERWRITED ('0'=OFF; '1'=ON)	1 1 1 1 1 1 1 1 1	START BIT (always '1') CARD TYPE (always '1'=LOCAL) LOCAL BUSY ('0'=OK; '1'=FIFO full) LOCAL DECISION (tracklet) ACTIVE ('0'=OFF; '1'=ON) REJECTING ('0'=OFF; '1'=ON) MASKED ('0'=OFF; '1'=ON) OVERWRITED ('0'=OFF; '1'=ON)	1 1 1 1 1 1 1 1 1	START BIT (always '1') CARD TYPE (always '1'=LOCAL) LOCAL BUSY ('0'=OK; '1'=FIFO full) LOCAL DECISION (tracklet) ACTIVE (always '1'=ON) REJECTING (always '0'=OFF;) MASKED ('0'=OFF; '1'=ON) OVERWRITED ('0'=OFF; '1'=ON)	1 1 1 1 1 1 1 1 1
SOx EOx PAUSE (always '0') RESUME (always '0') CALIBRATE PHY (ignored) RESET ORB	1 1 1 1 1 1 1 1	SOx (always '0') EOx (always '0') PAUSE (always '0') RESUME (always '0') CALIBRATE (always '0') PHY RESET (always '0') ORB	1 1 1 1 1 1 1 1	Always '0'	8
REGIONAL bunch counter	16	REGIONAL bunch counter	16	REGIONAL bunch counter	16
REGIONAL crate position (0-15)	4	REGIONAL position crate (0-15)	4	REGIONAL crate position (0-15)	4
Status: Mask registers (SOx='1'| EOx='1') Data: All tracklet inputs (not masked)	4	Always '0'	4	Data: detector plane(s) (1 bit / plane)	4
Total number of bits	40	Total number of bits	40	Total number of bits	40
Bunches needed to send	5	Bunches needed to send	5	Bunches needed to send	5

2.4.5 Gigabit Transceiver protocol

The GBT protocol architecture was created at CERN, for use in the LHC, which requires high bandwidth as well as radiation protection [7]. Embedded in the regional cards is a radiation-hardened ASIC known as GBTx (Fig.2.6). This ASIC contains a high-speed serializer and deserializer that takes data and then transmits them through a laser transmitter, as well as the reverse for the downlink. The laser transmitter utilized is a special component manufactured at CERN. The GBT optical link controller is implemented as a module in the CRU firmware. The GBT protocol operates in 3 different frame modes: standard GBT frame, wide frame, and 8B/10B frame. Figure 2.4 depicts the standard GBT frame mode used in the MID readout chain.

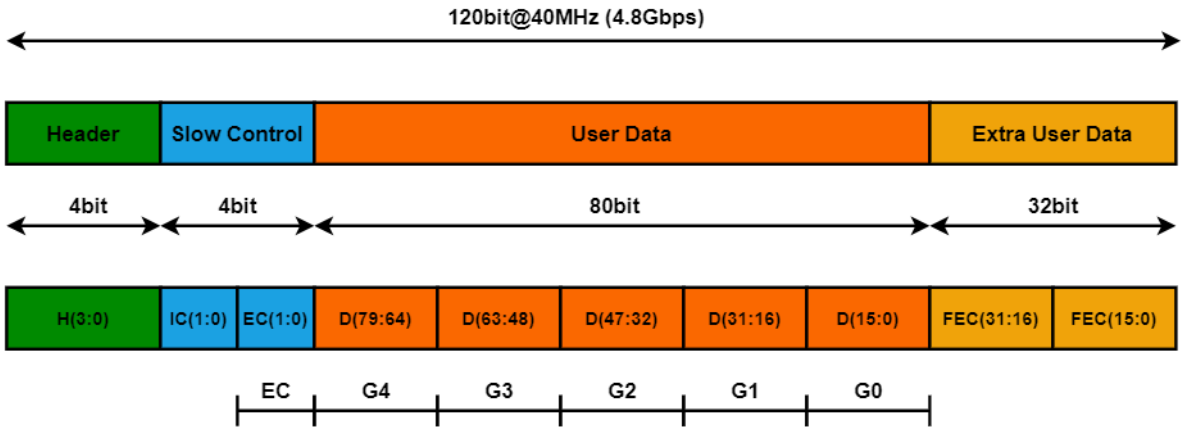

Figure 2.4: Block diagram of the standard GBT mode encoding and decoding. Adapted from [7]

The standard GBT frame is continuously transmitted during a single LHC bunch crossing. It starts with a 4-bit header field, which is necessary for frame-level synchronization of the data stream. Recognizing multiple valid headers implies a proper frame-locking. The opposite implies that the frame synchronization has failed and the frame synchronization cycle must be initialized. The header field can either provide a value "0x5" (data state), which indicates that the frame includes legitimate data, or "0x6" (idle state), which indicates that the frame does not include valid data. Next is, a 4-bit used for slow control, the first two of which are for Internal Control (IC), which is reserved for controlling the GBTx ASIC. The last two slow control bits are for External Control (EC). The payload data and EC fields are not pre-assigned and are utilized for a variety of functions, including Data Acquisition (DAQ), Timing and Trigger Control (TTC), and experiment control, depending on the needs of the MID. The last 32 bits are utilized for forwarding Error Correction (FEC). The remaining 84-bit, which includes the EC, having an associated bandwidth of 3.36 Gb/s, of which 3.2 Gb/s is allocated to the payload data.

Before serialization, the data, EC, and IC fields are put through a scrambling process that concatenates them. In addition to the header, a Reed-Solomon (RS) encoder creates the 32-bit FEC based on the scrambled data. The deserializer does the opposite. Both scenarios are represented in Figure 2.5.

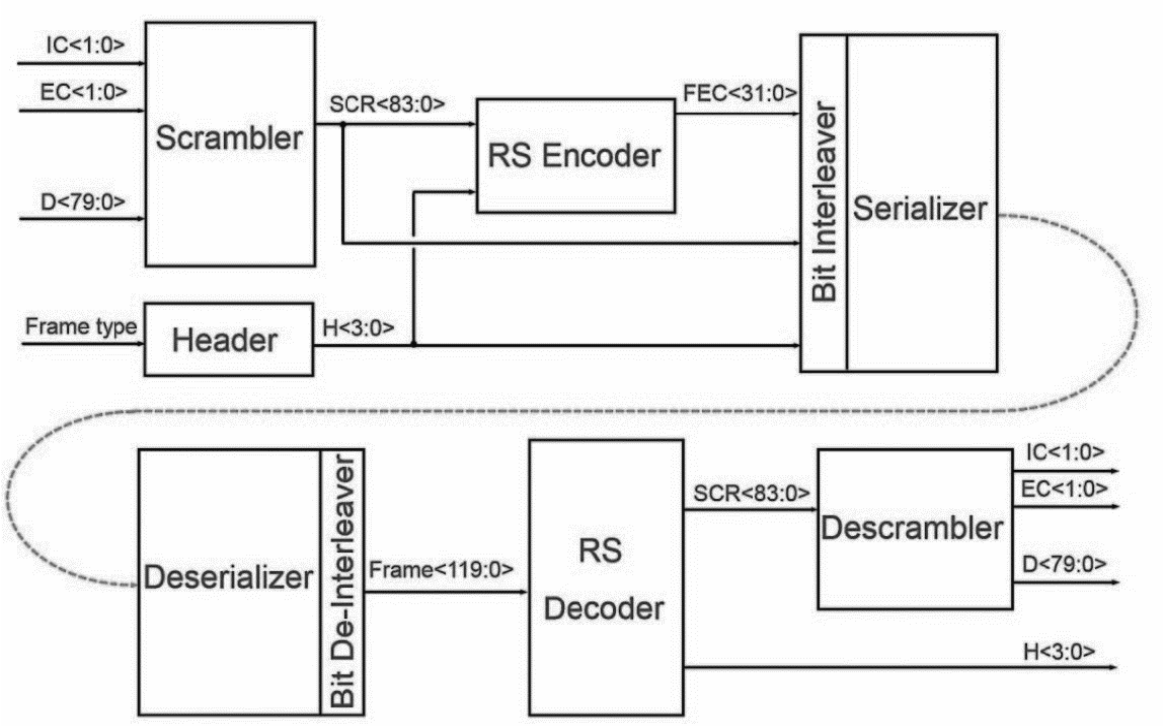

Figure 2.5: Block diagram of the standard Mode GBT encoding and decoding. Adapted from [7]

The header is used to track frames and synchronize the receiver with the sender. The header is not affected by the scrambling therefore, it is easily detectable. When a GBT receiver is powered up, it enters a frame-lock initialization mode in which it searches for valid headers. After detecting a configurable number of frames with valid headers, it considers that the connection has been established and enters the frame tracking mode, in which it receives data and runs normally while searching for invalid headers.

Once it is determined that a configurable number of consecutive frames is invalid, the synchronization is considered lost and the initialization mode is re-entered. This usually requires multiple invalid frames, so an accidental violation of a single random frame is not enough to cause channel synchronization. The data field (80 bits) of the GBT frame is used for data transmission. GBT frames are divided into control frames, data frames, and the header contains data valid only for the latter. The frame starts with a 4-bit identification header. Four headers are defined: IDLE, Start of Packet (SOP), End of Packet (EOP), and the Single Word Transaction (SWT). The IDLE frame does not contain any information. SOP and EOP, as the name suggests, mark the beginning and end of the detector data packet, which contains various packet-related metadata. The SWT frame contains any data used for a specific control or data transmission. On the GBT uplink, SWT frames are transmitted between data frames, that is, between EOP and SOP control frames. In the MID read chain, the SWT frame is used to access the register bus on the regional card.

The 2 bytes in the EC payload of the GBT frame are routed to a special slow control ASIC called GBT-SCA [8]. As mentioned above, the chip is part of the regional card. The communications between the CRU and SCA are implemented in the CRU firmware architecture described in Chapter 3. The GBT-SCA ASIC has a large number of communication modules, including various GPIO, ADC, and DAC pins, as well as I²C, SPI, and JTAG master control. The communication between the regional FPGA and GBT-SCA is carried out through the high-level serial link control (HDLC) protocol. The protocol is based on commands. In contrast to the direct reading and writing of registers, the transaction contains the command ID, transaction ID, and data required by the command. The command ID indicates what the GBT-SCA chip will do, such as read or write registers or perform operations. Each command transaction returns a batch with the same transaction ID. The return package contains status information and returned data. The slow control IC is used for GBTx register access, configuration, and monitoring. This field can also control the laser transceivers that use the main communication modules on the GBTx chip, which can be accessed through its registers.

Electrical-links

The GBTx chips on the regional cards communicate with up to 8 local card FPGAs using the standard GBT frame mode. It consists of connecting the GBTx and the regional FPGAs through duplex electrical serial lines (e-links). Each GBT bi-directional optical link of the readout chain is made up of 10 serial e-links (8 local e-links + 2 internal regional e-links).

Each of these e-links consists of three signal lines (differential pairs):

- Differential Clock line (dClk+/dClk-): Clock driven by GBTx to the local/regional FPGA
- Differential Downlink data output (dOut+/dOut-): Data from GBTx to the local/regional FPGA
- Differential Uplink data input (dIn+/dIn-): Data line from the local/regional FPGA to GBTx

The MID readout chain is configured to operate at the maximum e-links data rate of 320 Mb/s, with a maximum of 2 e-links per group. As mentioned earlier, each e-link is composed of one differential clock line (dClk+/dClk-), one differential downlink output (dOut+/dOut-), and one differential uplink input (dIn+/dIn-). Thus, the maximum number of differential e-link signals per group is 3 x 2 = 6, equivalent to 6 signal pins per group. Overall, a total of 6 x 5 = 30 configuration pins are dedicated to the e-links. To provide the greatest possible signal quality and transmission reliability, the physical e-link connections are assumed to be differential transmission lines with a differential impedance of 100 Ω and a suitable termination line at the receiver end.

Figure 2.6 represents the e-links configuration between the GBTx chip and the readout electronics.

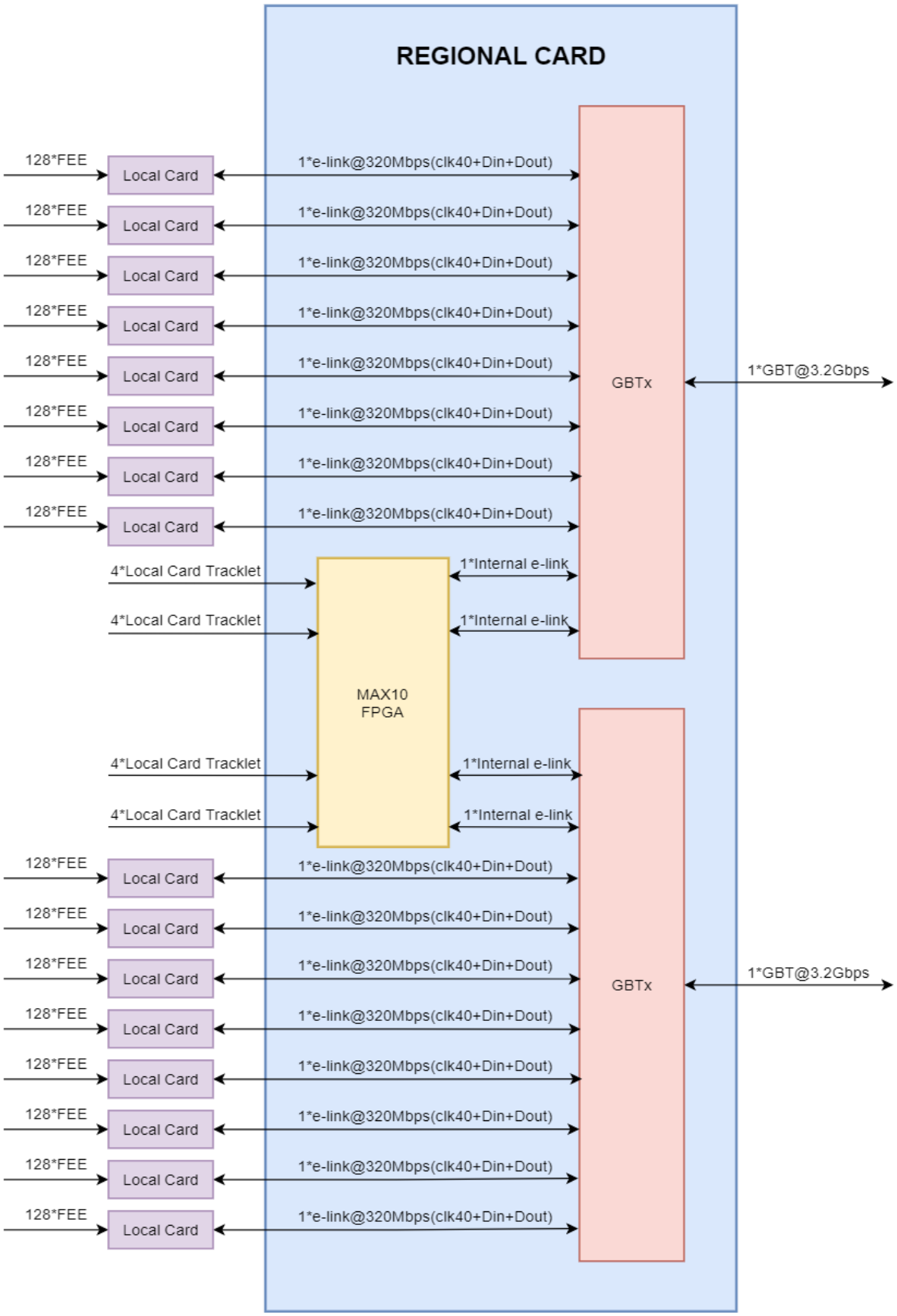

Figure 2.6: E-links configuration between the GBTx chip and the readout electronics.

2.5 Common readout unit

The ALICE CRU hardware architecture is shown in Figure 2.7. Besides the PCIe interface, which utilizes a built-in 100 MHz crystal oscillator, the clock tree is designed to utilize a single reference clock for all CRU communication links. The CRU card can either be used independently with a built-in 40MHz crystal oscillator or with a recovered clock retrieved from the TTS optical link. On the other hand, the TTS transceiver requires a constant 240 MHz reference frequency before initialization, which is generated locally with the help of a Phase-Locked Loop (PLL) SI5344. The clock recovered from the FPGA is transferred to a high-performance SI5345 PLL for jitter attenuation after it has successfully been locked to the incoming stream. The clocks extracted from the SI5345 PLL are then utilized to run the FPGA logic. The SI5345 PLL uses I²C communication to switch between local and recovered TTS clock modes. The clock generated from the built-in 100 MHz crystal oscillator is utilized to run many other features of the FPGA, including initialization and hardware monitoring.

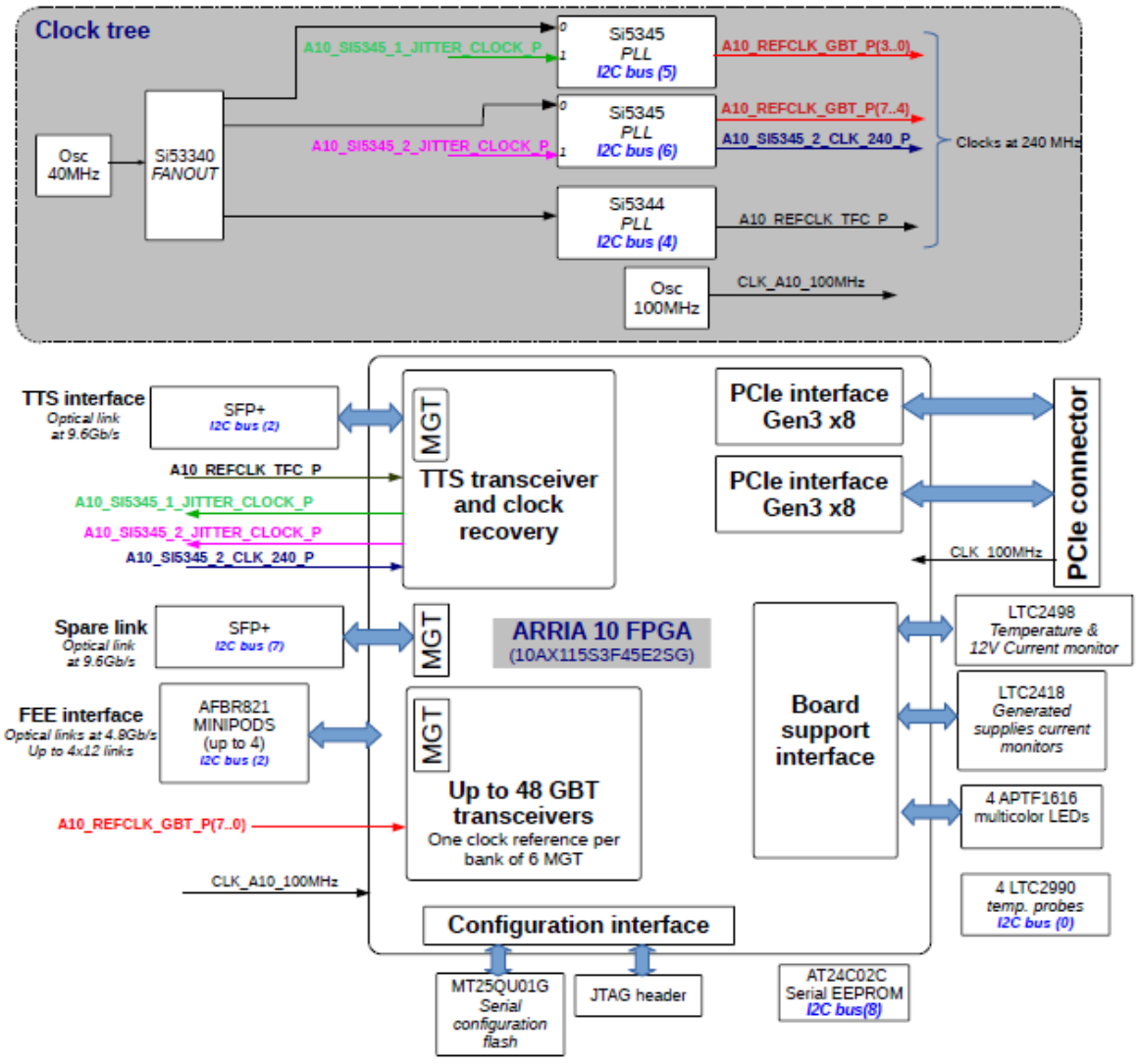

Figure 2.7: A functional overview of the hardware, highlighting the functions used in the CRU [9].

The CRU card is embedded with an Intel ARRIA10 FPGA (10AX115S3F45E2G) [10]. It is equipped with two Small Form-factor Pluggable (SFP+) connections. One is used for TTS connection, and the other is used as a backup. The connections from/to the readout electronics are ensured by up to 4x12-channel bi-directional 10.3125 Gb/s optical transceivers (mini-pods) [11]. These two mini-pods can connect to up to 24 GBT links. However, for what concerns the MID, 32 GBT links are necessary to transfer data from the complete readout electronics. Hence, 2 CRU cards are utilized, each connected to 16 GBT links.

The CRU is equipped with a PCIe edge connector on the rear end, that provides a dual gen3 x8 PCIe interface. This interface is synchronized with a 250MHz reference frequency provided through the connector. The FPGA is also linked to board support functions such as temperature and current sensors, as well as an EEPROM with a unique identifier assigned by the manufacturer during board construction. I²C and SPI are used to communicate with various peripheral devices. There is also the option to control tri-color LEDs, which is essential for easily locating a single machine in a server farm for maintenance purposes. Finally, the FPGA can be programmed using either a JTAG connector, which is useful for software debugging in the laboratory or a Quad SPI flash. The latter can be remotely modified over the PCIe interface, allowing for on-site updates.

2.6 Trigger architecture

The ALICE trigger architecture is an amalgamation of multi-link technologies based on several protocol standards. It has been optimized to function in coherence with the surrounding blocks of the detectors, allowing the complete readout chain to operate synchronously and efficiently. The ALICE trigger architecture relies on the Trigger and Timing distribution System (TTS) ability to efficiently distribute the critical Timing and Trigger Control (TTC) information from the CTP to the readout electronics via the LTU and CRUs with constant latency over bi-directional TTC 10G-Passive Optical Network (PON) links. This allows the MID to be read out in continuous and triggered readout mode operations.

2.6.1 Central Trigger Processing

The CTP in the trigger architecture controls global trigger decisions and supervises the generation of trigger requests by integrating inputs from a set of trigger contributing detectors [12]. It is critical to recognize unusual occurrences and record them for later analysis. The CTP also generates periodic heartbeat (HB) triggers and customized software triggers for both continuous and triggered operations. It interacts with up to 24 LTUs, one of which is dedicated to MID.

2.6.2 Local Trigger Unit

The LTU serves as an interface between the CTP and CRUs. It provides a clock, orbit, and external trigger inputs as well as allows monitoring and control using ethernet bus protocols. The LTU is a 6U VME-type board equipped with a Xilinx Kintect FPGA with 2 GB of DDR4 memory [13]. It has two modes of running, global and stand-alone. In global mode, the LTU acts as a transparent interface between the CTP and the CRU. It converts signal levels and provides some online monitoring. However, in the stand-alone mode, the LTU emulates the CTP protocol, allowing the MID team to perform tests, and calibration activities independently of the CTP, at remote sites, or when the CTP is either unavailable or not necessary.

2.6.3 Heartbeat

The heartbeat trigger is scheduled by the CTP to run with the highest possible priority and with a fixed period (89.4us). The heartbeat trigger is used by the readout electronics and CRU to verify whether its bunch crossing, orbit, and trigger counters are still synchronized. The amount of data collected between two HB triggers is called HeartBeat Frame (HBF). This HBF is generated by the CRU and used by O^2 systems for data segmentation, fault finding, and recovery procedures. The readout electronics cards in the MID readout chain are modified to handle this combination of physics and heartbeat triggers. Each regional/local card autonomously tags the data using the copy of the LHC Orbit and the bunch crossing id (BCID). For continuous mode, the payload data are sent as a continuous flow of successive frames each preceded with a header containing the time-based tagging. The triggered mode operates in the same way as the continuous mode with a few variations, it only sends a payload data block preceded with a header upon reception of physics triggers. Figure 2.8 shows how the physics and heartbeat triggers are used for the continuous and triggered readout modes.

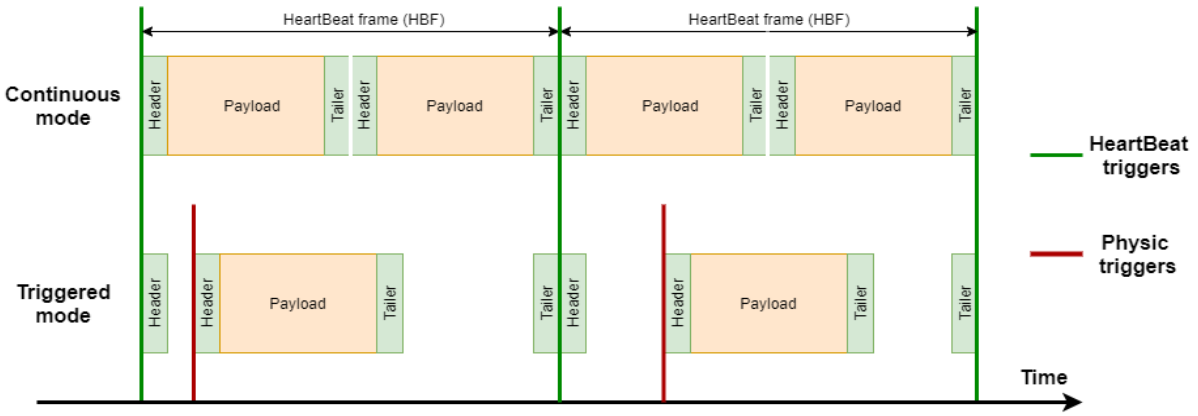

Figure 2.8: Continuous and triggered mode trigger configuration

2.6.4 TTC 10G-PON

The TTC 10G-PON is a point-to-multipoint network architecture that uses optical splitters to enable an Optical Line Terminal (OLT) to interact with several Optical Network Units (ONUs). The TTC 10G-PON technology, as illustrated in Figure 2.9, allows the TTC message to be split among multiple CRUs of the readout chain using a single link. The TTC-PON downstream (CTP to CRU) and upstream (CRU-CTP) messages are described below.

- The TTC-PON downstream message is based on a 240-bit word transmitted synchronously with the LHC clock from CTP to the CRUs. The PON internally uses 40-bit, leaving 200-bits available for the sub-detectors use. The complete message is summarised in Table 2.4. The trigger type information is described in Table 2.5.

- Upon reception of an HB trigger, each CRU of the readout chain transmits the TTC-PON upstream message of 56 bits to the CTP, alternatively called HB acknowledge message (HBam). The HBam carries information about the CRU status illustrated in Table 2.6. The CTP collects the HBam from all CRUs acknowledging that data have been successfully collected.

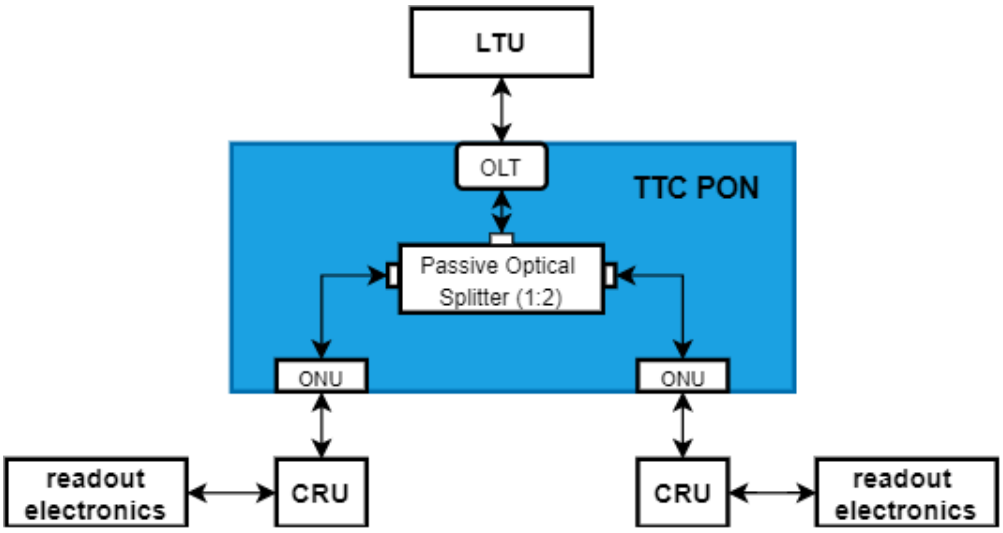

Figure 2.8: TTC-PON architecture

Table 2.4: PON downstream message

No. of Bit	Name	Description
<31:0>	TType	Trigger Types data
<11:0>	BCID	Bunch crossing identification
<31:0>	Orbit	Orbit counter
<0:0>	TTValid	Trigger Type data valid
<7:0>	HBM header	Heartbeat message header
<31:0>	1st ORBIT of TF/HBMTF	Heartbeat message time frame
<0:0>	HBMValid	Heartbeat meassage valid

Table 2.5: Trigger Types

Bit	Name	Description
0	Orbit	Orbit flag
1	HB	HeartBeat flag
2	HBr	HeartBeat reject flag
3	HC	Health Check
4	PhT	Physics Trigger
5	PP	Pre Pulse Calibration
6	Cal	Calibration trigger
7	SOT	Start of Continuous
8	EOT	End of Continuous
9	SOC	Start of Triggered Data
10	EOC	End of Triggered Data
11	TF	Time Frame
…	…	Spare
29	TPCSync	TPC synchronization
30	TPCReset	TPC reset
31	TOF	TOF special trigger

Table 2.4: PON upstream message

No. of Bit	Name	Description
<31:0>	HB id	Heartbeat identification
<9:0>	CRU id	CRU identification
<0:0>	CRU ack	CRU acknowledge bit
<1:0>	CRU status	CRU buffer status
<11:0>	Spare	Spare bits

2.6.5 MID trigger types

The TTC-PON trigger types information are compressed to be of HB triggers are envisaged, HB-accept (HBa) and HB-reject (HBr) depending on the status of CRUs. The HBa and HBr triggers will contain the HBid and a bit to signify whether it is an HBa or HBr. After receiving an HB trigger, each CRU will transmit an HB acknowledge message to the CTP, via their LTU. The payload of the message is defined in [8], table 7. The CTP will collect the HB acknowledge of all CRUs, within a time-frame of 8 Orbits and form an HB map**. (Please ignore for now)**

Table 2.4: MID custom trigger format

MID trigger type	CTP trigger type	CRU message to Readout electronics	FEE trigger code
SOx (Start Of Run)	9: SOC 7: SOT	Update internal ORBIT, BCID, bunch counter Transmit command to all e-links Reset event buffers Start assembling events Start sending events	0x80
EOx (End Of Run)	10: EOC 8: EOT	update internal Orbit, BCID & bunch counters Transmit command to all e-links Assemble last events Send last events	0x40
TF (TimeFrame)	11: TF	Transmit command to all e-links	0x20
RUNNING (Run status)	14: RS	Transmit command to all e-links	0x10
CALIBRATE	6: CAL	Update internal Orbit, BCID & bunch counters Transmit command to all e-links	0x08
PHY	4: PhT	Update internal Orbit, BCID & bunch counters Transmit command to all e-links	0x04
RESET	12: FEErst	Update internal Orbit, BCID & bunch counters Transmit command to all e-links Stop assembling events Stop sending events	0x02
ORBIT	0: ORBIT	Update internal Orbit, BCID & bunch counters Reset internal MID's bunch counter Transmit command to all e-links	0x01

2.7 Online-Offline computing farm

The O² computer farm is composed of the First Level Processors (FLP) and Event Processing Nodes (EPN).

The ALICE reconstruction strategy consists of 2 phases: a first synchronous online reconstruction stage during data-taking enabling detector calibration, and a posterior calibrated asynchronous reconstruction stage.

The global architecture of the online system as presented in the upgrade LoI

2.7.1 First Level Processor

The FLP (DELL POWEREDGE R740) exchanges information with the FEE via the CRU, it can host a maximum of two CRUs. The FLP communicates with the EPN through a 100 Gb InfiniBand network.

2.7.2 Event Processing Node

2.8 Detector control system

The readout electronics are monitored and controlled by the ALICE DCS. The DCS system accesses the readout electronics via the FLP and CRUs through a network connection. The main protocol considered for communication between the CRU and DCS is called Alice Low-Level Front-end (ALF) on the CRU side and Front-End Device (FRED) on the DCS side. In the current readout chain implementation, the ALF can read/write registers implemented on the readout electronics cards modules and publish the data using a Distributed Information Management System (DIM) service.

The DIM is a communication system for distributed/mixed environments, originally developed for one of the experiments of the Large Electron-Positron Collider, an earlier particle accelerator at CERN. It provides a network transparent inter-process communication layer. The FLP host computer runs a DIM server, which acts as a bridge between the DIM network and the CRU driver, allowing DCS to communicate with the CRU from the control center without physical access to the CRU host computer.

2.9 References