Chapter 2

Muon identifier readout chain

The transition from MTR to MID during the LS2 entails,

2.1 Overview

In total, the readout chain consists of 21 000 strips attached to 72 RPC detectors spread over multiple front-end electronics cards equipped with one or two FEERIC ASICs. The strip pattern signals from the FEERICs are propagated to the readout electronics, acting as the readout interface and in charge of the first stage of the trigger decision. The readout electronics are mounted on the upper gangways a little further away from the stations, where the radiation is low. The beam collisions will produce a lot of radiation in the area around ALICE, therefore the readout electronics regional cards are equipped with Gigabit Transceiver (GBT) radiation hardening to operate properly. The CRUs combine and multiplex data from multiple readout electronics cards as well as timing and trigger information from the Timing and Trigger system (TTS) before transmission to the O² computing facility for processing and storage in the next layer of the readout chain. The CRUs are mounted in computers housed in the intermediary computer room, called the counting room, away from the ALICE cavern and thus do not require radiation hardening, as is the case for the readout electronics. These computers can be reached over the network from the main Detector Control System (DCS). The DCS manages the readout chain by sending commands and monitoring the system. Experiment data are moved from the FLP node to the O² computing system for processing and storage. A block diagram of the readout chain is shown in Figure 2.2.

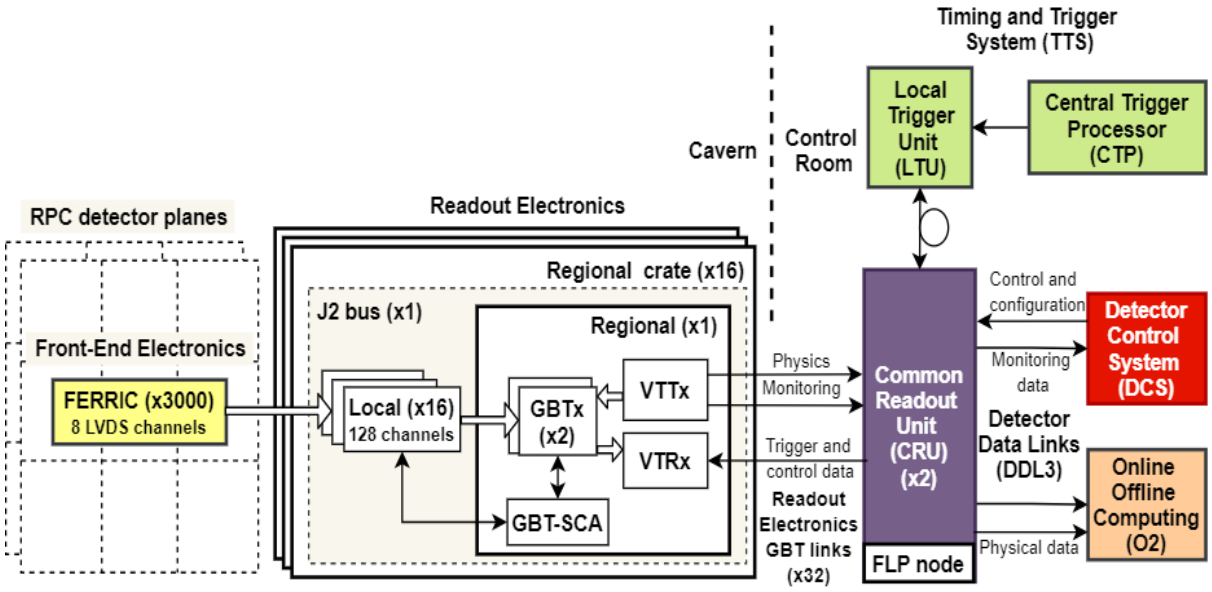

Figure 2.2: MID readout chain architecture

2.2 RPC detectors

In the ALICE cavern, three distinct forms of RPC are installed. They refer to long, short, and cut forms, respectively (Fig.2.3). The beam pipe is accommodated by the short-cut forms. The current RPCs are constructed with 2 mm wide gas gaps, 2 mm thick High-Pressure Laminate (HPL or bakelite) resistive electrodes, and polyamide insulation layers. The readout strips are made of copper and have three different pitch options: 1, 2, or 4 cm. Both RPCs have one collection of readout strips on each hand. The strips on either side of the RPCs are orthogonal to one another. In comparison to the dipole motion

on charged-particle tracks, the vertical strips that have (y) hits are referred to as non-bending and the horizontal strips that have (x) hits are referred to as bending.

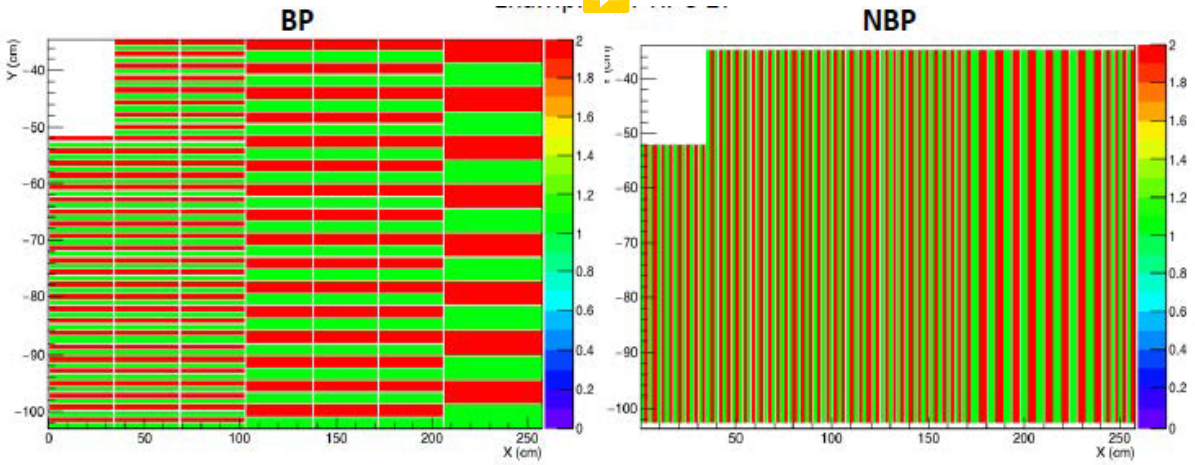

Figure 2.1: RPC strip patterns

Scientists predict an improvement in RPC hits in lead-lead collisions to exceed the highest counting rate of about 10 Hz/cm2 up to 90 Hz/cm2, which is marginally similar to the maximum rated capacity of the sub-detector in the maxi-avalanche mode described in [ ]. This rise would also hasten the aging of the gas gaps, which will hit the end of their projected lifespan long before the end of Run 3, necessitating the replacement of certain gas gaps and other affected components.

These upgrades are distributed among three institutions. The Puricelli factory in Costa Masnaga (Italy) is responsible for redesigning the bakelite resistive electrodes, which feature a smoother surface for the bakelite used on the presently installed RPCs, the General Tecnica in Colli (Italy) is responsible for manufacturing the gas gaps for the new RPCs and, the National Institute for Nuclear Physics (INFN) in Torino (Italy) is responsible for checking and testing the performance of the new RPCs with cosmic rays. The installation of the new RPCs in the cavern is expected to start from July 2021, with the intent of installing 2 RPCs per day. In case of failure to meet this deadline, the MID will operate with the existing RPCs during Run 3 until the new RPCs are ready.

2.3 Front-End electronics

The RPC ADULT electronics have been replaced by a new ASICS named the Front-End Electronics Rapid Integrated Circuit (FEERIC) [ ] and unlike the ADULT, it amplifies the analog signals from the RPCs. The FEERIC is an 8-channel ASIC that uses low-cost AMS 0:35mm CMOS technology developed by the Laboratory of Physics Clermont-Ferrand. It is made up of a trans-impedance amplifier stage, a zero-crossing discriminator to limit time walk effects, and a one-shot to prevent retriggering during 100 ns and LVDS drivers. Table 2.1 summarizes the main specifications, and requirements of the FEERIC ASIC. In contrast to the ADULT card thresholds, which were formerly set using an analog voltage distributed of just one threshold value per RPC, the FEERIC card thresholds would be set wirelessly during Run 3. Their values will be assigned to each card, allowing one to fine-tune the threshold based on the local RPC efficiency while minimizing operating high voltage. The technology selected to accomplish this task is the ZIGBEE protocol. It is a wireless technology established as an

open universal norm to meet the special requirements of low-cost, low-power wireless IoT networks based on the IEEE 802.15.4 physical radio interface and works in unlicensed bands such as 2.4 GHz. The ZEGBEE is incorporated on the Atmel SAMD21 microcontroller and the program is based on Arduino libraries (I2C, SD cards, and Xbee module). This is then put onto a printed circuit board called the Xbee cards. The master cards are linked to the DCS PC using ethernet, and the ZIGBEE (wireless) protocol is used to communicate from master to nodes.

Table 2.1: Requirements of the FEERIC ASIC

feature	**value or type**
pulse polarity	positive or negative
# of channels	8
power consumption per channel	< 100 mW
input impedance	< 50 W
dynamic range	20 fC < q < 3 pC
time resolution	< 1 ns
time walk	< 2 ns
one-shot	100 ns
output format	LVDS
signal shape	square pulse 23±3 ns

As previously mentioned, the charge delivered within the gas gaps must be lowered to minimize aging and improve rate capabilities. This is achieved by operating RPCs with the same gas mixture but at a lower gain, in conjunction with new FEERIC ASICs which perform amplification of the analog signal before discrimination. So far, ~~(~~2384 + 336 spares~~)~~ FEERIC cards and 26 Xbee cards have been manufactured and installed in the ALICE cavern. The installation and commissioning of all FEERIC and Xbee cards concluded in July 2019 [ ].

2.4 Readout electronics

To cope with the new readout rates, the local and regional readout cards have been redesigned. Since the triggering functionalities are abandoned, a more streamlined approach has been introduced. The hardware implementation of the regional and local card is almost identical, minimizing the design and development effort by re-using the same hardware and altering the FPGA firmware. The global crate has been replaced by a new regional crate.

As shown in Fig 2.3, the readout electronics are divided into 16 vertical regions (8 on the left and 8 on the right side of the plane). Each vertical region is read out by a single regional crate. Each contains a backplane bus card called the J2 card, which connects to a single regional card and up to 16 local cards.

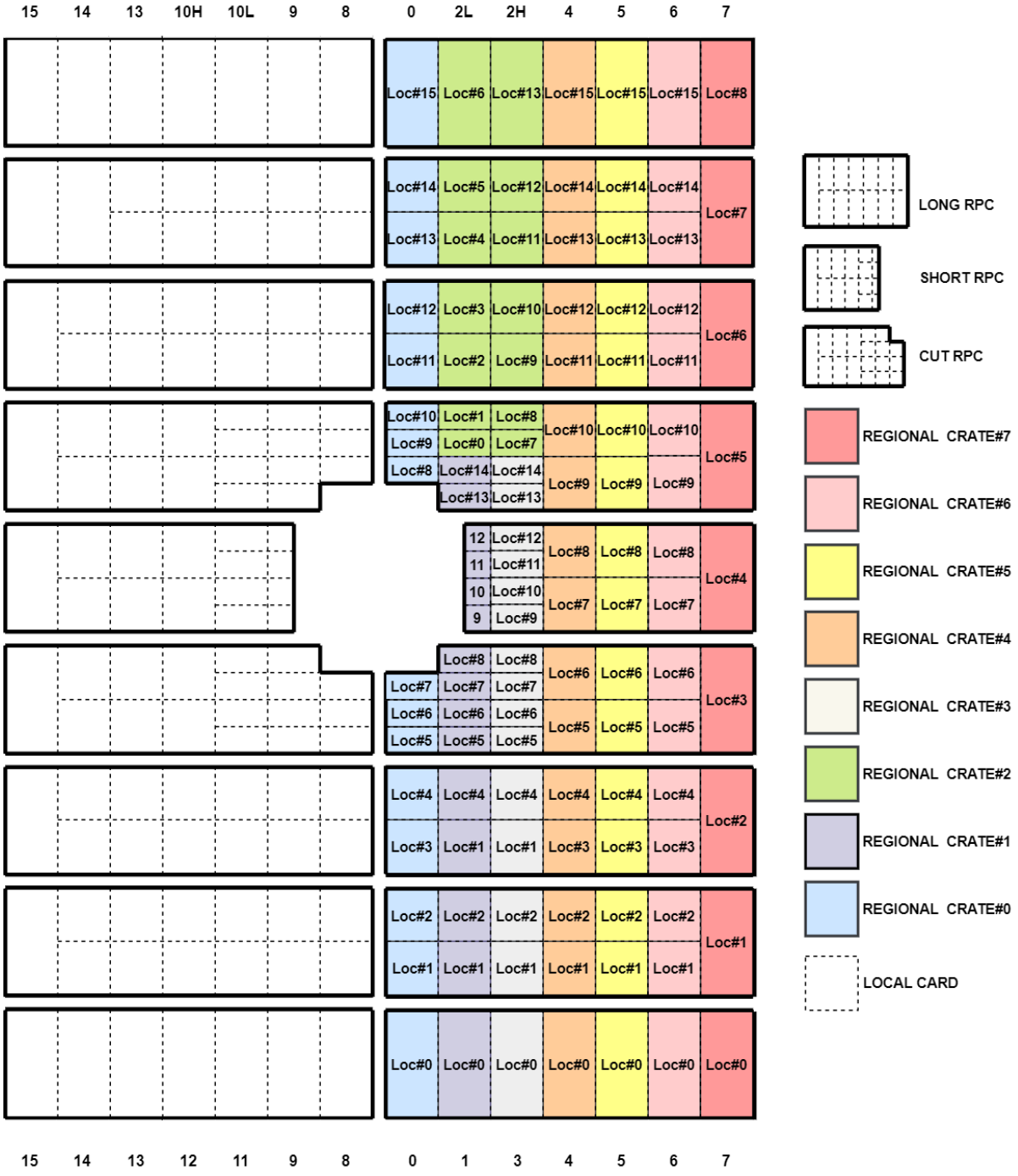

Figure 2.2: Geometry of the readout electronic

2.4.1 Local card

For every bunch crossing, the local card receives binary data from LVDS channels, which indicates whether the corresponding channel has been struck or not. The local card is equipped with 16 LVDS input connectors (32 pins, for both the BP and NBP). It is embedded with the Intel MAX 10 FPGA (10M50DCF484C7G). Its FPGA firmware is described here []

2.4.2 J2 bus card

The J2 bus card serves as an interface between the regional crate and the local/regional cards in terms of power, and it also serves as an interface between the local and regional cards in terms of data transfer. The J2 bus card has a 4-bit dip switch for assigning a specific identification to the regional crate, as well as three LEDs for monitoring the voltages (2.5V, 3.3V, and 5V) supplied to the regional and local cards.

2.4.3 Regional card

The regional card collects data from up to 16 local cards using the GBT protocol, which is discussed in the next section. Similar to the local card, the regional card is incorporated with the same Intel MAX 10 FPGA. However, unlike the local card, it is equipped with two bi-directional GBT optical links allowing transmission and reception of data to/from the CRU. The implementation of 2 GBT optical links per regional card enables complete regional crate data transfer. The firmware implemented in the regional card FPGA is a slightly modified version of the local card firmware, which is also described in [].

2.4.4 Event data formats

Events are stored in the local and regional card multi-buffers ~~at~~ each trigger. The multi-event buffer in the local card carries strip patterns, therefore it is larger than the regional card. The event data formats of the local card and regional card are shown in Tab.2.2 and Tab.2.3 accordingly.

Table 2.2: Local event format

Coding of SOx, EOx, RESET, CALIBRATE Event in LOCAL	*Bits*
START BIT (always '1') CARD TYPE (always '1'=LOCAL) LOCAL BUSY ('0'=OK; '1'=FIFO full) LOCAL DECISION (tracklet) ACTIVE ('0'=OFF; '1'=ON) REJECTING ('0'=OFF; '1'=ON) MASKED ('0'=OFF; '1'=ON) OVERWRITED ('0'=OFF; '1'=ON)	1 1 1 1 1 1 1 1 1
SOx EOx PAUSE (always '0') RESUME (always '0') CALIBRATE PHY (ignored) RESET ORB	1 1 1 1 1 1 1 1
LOCAL bunch counter	16
LOCAL board position in Crate (0-15)	4
Status: "0xF"	4
Status: Mask registers (SOx='1'|EOx='1') Data: all strip patterns (not masked) [(X4, Y4), (X3, Y3), (X2, Y2), (X1, Y1)]	32*4
Total number of bits	
Bunches needed to send	

Coding of PHY, ORB Event in LOCAL	*Bits*
START BIT (always '1') CARD TYPE (always '1'=LOCAL) LOCAL BUSY ('0'=OK; '1'=FIFO full) LOCAL DECISION (tracklet) ACTIVE ('0'=OFF; '1'=ON) REJECTING ('0'=OFF; '1'=ON) MASKED ('0'=OFF; '1'=ON) OVERWRITED ('0'=OFF; '1'=ON)	1 1 1 1 1 1 1 1 1
SOx (always '0') EOx (always '0') PAUSE (always '0') RESUME (always '0') CALIBRATE (always '0') PHY RESET (always '0') ORB	1 1 1 1 1 1 1 1
LOCAL bunch counter	16
LOCAL board position in Crate (0-15)	
Always '0'	
N/A	0
Total number of bits	40
Bunches needed to send	5

Coding of self-triggered DATA Event in LOCAL	*Bits*
START BIT (always '1') CARD TYPE (always '1'=LOCAL) LOCAL BUSY ('0'=OK; '1'=FIFO full) LOCAL DECISION (tracklet) ACTIVE (always '1'=ON) REJECTING (always '0'=OFF;) MASKED ('0'=OFF; '1'=ON) OVERWRITED ('0'=OFF; '1'=ON)	1 1 1 1 1 1 1 1 1
Always '0'	8
LOCAL bunch counter	16
LOCAL board position in Crate (0-15)	
Data: detector plane(s) (1 bit / plane)	
Data: Only masked strip pattern(s) [(X4, Y4), (X3, Y3), (X2, Y2), (X1, Y1)]	32*i
Total number of bits	8*bc
Bunches needed to send	9 - 21

Table 2.3: Regional event format

Coding of SOx, EOx, RESET, CALIBRATE Event in REGIONAL	*Bits*
START BIT (always '1') CARD TYPE (always '1'=LOCAL) LOCAL BUSY ('0'=OK; '1'=FIFO full) LOCAL DECISION (tracklet) ACTIVE ('0'=OFF; '1'=ON) REJECTING ('0'=OFF; '1'=ON) MASKED ('0'=OFF; '1'=ON) OVERWRITED ('0'=OFF; '1'=ON)	1 1 1 1 1 1 1 1 1
SOx EOx PAUSE (always '0') RESUME (always '0') CALIBRATE PHY (ignored) RESET ORB	1 1 1 1 1 1 1 1
REGIONAL bunch counter	16
REGIONAL crate position (0-15)	4
Status: Mask registers (SOx='1'| EOx='1') Data: All tracklet inputs (not masked)	4
Total number of bits	40
Bunches needed to send	5

Coding of PHY, ORB Event in REGIONAL	*Bits*
START BIT (always '1') CARD TYPE (always '1'=LOCAL) LOCAL BUSY ('0'=OK; '1'=FIFO full) LOCAL DECISION (tracklet) ACTIVE ('0'=OFF; '1'=ON) REJECTING ('0'=OFF; '1'=ON) MASKED ('0'=OFF; '1'=ON) OVERWRITED ('0'=OFF; '1'=ON)	1 1 1 1 1 1 1 1 1
SOx (always '0') EOx (always '0') PAUSE (always '0') RESUME (always '0') CALIBRATE (always '0') PHY RESET (always '0') ORB	1 1 1 1 1 1 1 1
REGIONAL bunch counter	16
REGIONAL position crate (0-15)	4
Always '0'	4
Total number of bits	40
Bunches needed to send	5

Coding of self-triggered DATA Event in REGIONAL	*Bits*
START BIT (always '1') CARD TYPE (always '1'=LOCAL) LOCAL BUSY ('0'=OK; '1'=FIFO full) LOCAL DECISION (tracklet) ACTIVE (always '1'=ON) REJECTING (always '0'=OFF;) MASKED ('0'=OFF; '1'=ON) OVERWRITED ('0'=OFF; '1'=ON)	1 1 1 1 1 1 1 1 1
Always '0'	8
REGIONAL bunch counter	16
REGIONAL crate position (0-15)	4
Data: detector plane(s) (1 bit / plane)	4
Total number of bits	40
Bunches needed to send	5

2.4.5 Gigabit Transceiver protocol

The GBT protocol architecture was created at CERN, for use in the LHC, which required high bandwidth as well as radiation protection [ ]. Embedded in the regional cards is a radiation-hardened ASIC known as GBTx (Fig.2.4). This ASIC contains a high-speed serializer and deserializer that takes data and then transmits them through a laser transmitter, as well as the reverse for the downlink. The laser transmitter utilized is a special component manufactured at CERN. The GBT optical link controller is implemented as a module in the CRU firmware as described later in Chapter 4. The GBT protocol operates in 3 different frame modes: standard GBT frame mode, wide frame mode, and 8B/10B frame mode. Fig.2.5 depicts the standard GBT frame mode used in the MID readout chain.

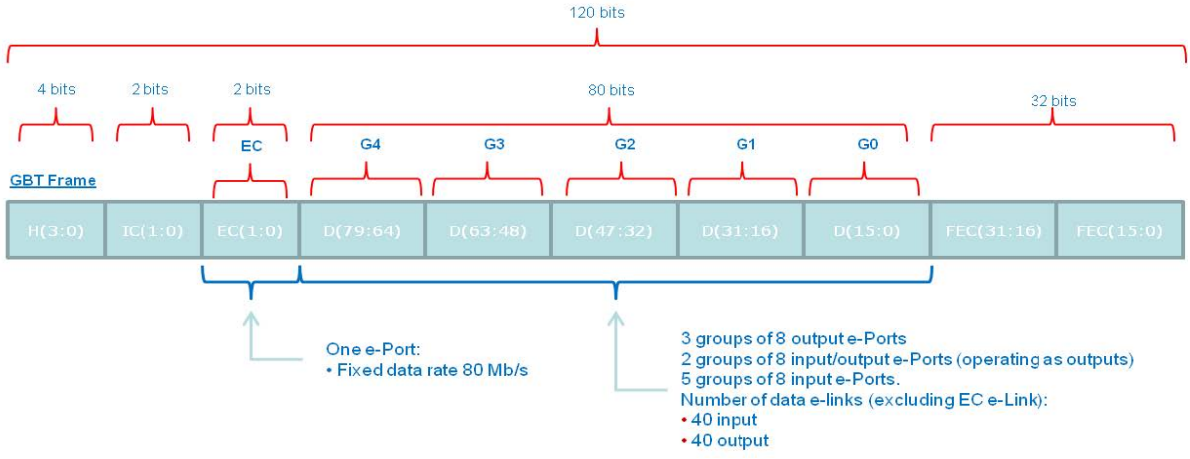

Figure 2.3: Block diagram of the standard mode GBT encoding and decoding. (to be changed later)

The GBT frame shown ~~above~~ is continuously transmitted during a single LHC bunch crossing. It starts with a 4-bit header field, which is necessary for frame-level synchronization of the data stream. Recognizing multiple valid headers implies a proper frame-locking. The opposite implies that the frame synchronization has failed and the frame synchronization cycle must be initialized. The header field can either provide a value "0b0101" (data state), which indicates that the frame includes legitimate data, or "0b0110" (idle state), which indicates that the frame does not include valid data. Next is a 4-bit used for slow control, the first two of which are for Internal Control (IC), which is reserved for controlling the GBTx ASIC. The last two slow control bits are for External Control (EC). The payload data and EC fields are not pre-assigned and are utilized for a variety of functions, including Data Acquisition (DAQ), Timing and Trigger Control (TTC), and experiment control, depending on the needs of the MID sub-detector. The last 32 bits are utilized for forwarding Error Correction (FEC). The remaining 84-bit, which includes the EC, having an associated bandwidth of 3.36 Gb/s, of which 3.2 Gb/s is allocated to the payload data.

Before serialization, the data, EC, and IC fields are put through a scrambling process that DC balances them. In addition to the header, a Reed-Solomon (RS) encoder creates the 32-bit FEC based on the scrambled data. The deserializer does the opposite. Both scenarios are represented in Figure 2.6.

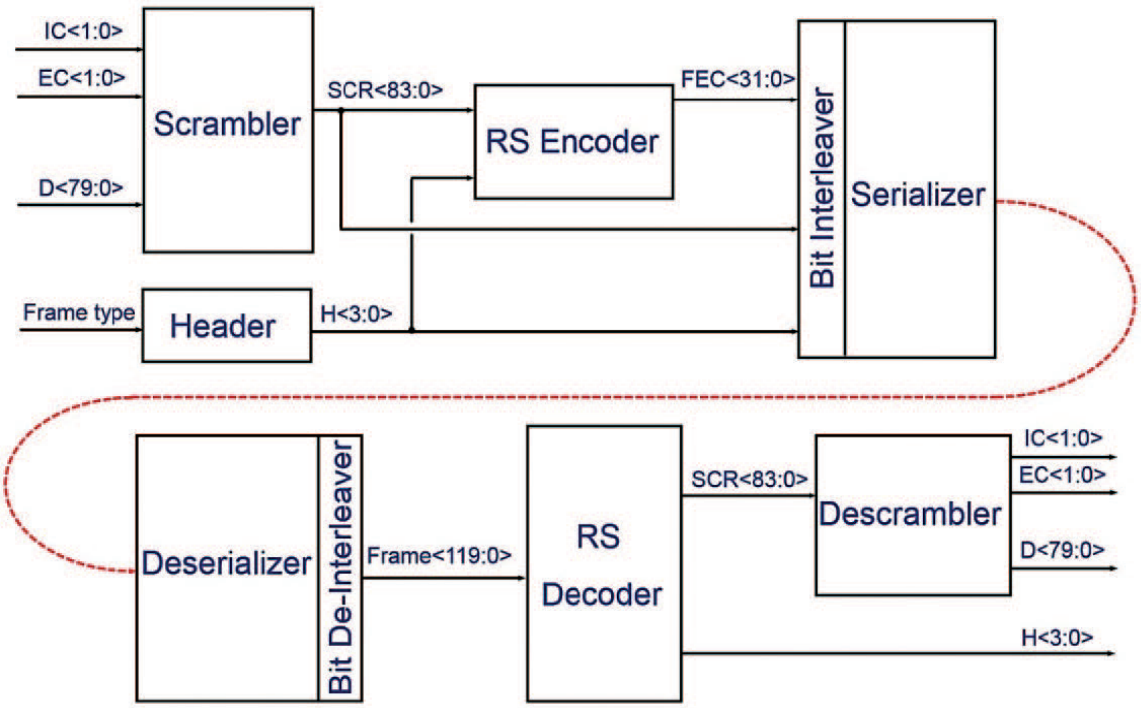

Figure 2.4: Block diagram of the standard Mode GBT encoding and decoding. Adapted from [36]

The header is used to track frames and synchronize the receiver to the transmitter. The header is not affected by the scrambling so that it can be easily detected. When a GBT receiver is powered up, it enters a frame-lock acquisition mode in which it searches for valid headers. Once a configurable amount of frames with valid headers have been detected in succession, it considers the link established and enters frame-tracking mode. In this mode, it receives data and operates normally, while keeping track of invalid headers.

Once a configurable amount of frames in succession is found to be invalid, it considers the synchronization lost and re-enters the acquisition mode. Typically multiple invalid frames are needed to trigger this, so that occasional random single event upsets aren't enough to cause the link to fall out of synchronization. The data field (80-bit) of the GBT frame is used to transmit the data. GBT frames are differentiated into control frames and data frames, with the header specifying data valid for the latter only. Control frames start with a 4-bit identifying header. Four headers are defined: IDLE, SOP (Start Of Packet), EOP (End Of Packet), and SWT. IDLE frames contain no information. SOP and EOP, as the names suggest, mark the start and end of packets of data from the detectors. They contain various metadata relating to the packets such as length and tags.

Single Word Transactions frames can contain arbitrary data used for special control or data transfers. In the GBT downlink, this will normally be the only type of GBT frame. In the uplink, SWT frames may only be sent in between data frames, in other words between EOP and SOP control frames. ~~In the ITS readout electronics, SWT frames are for example used to access the register bus on the readout unit main FPGA.~~

Slow Control

Part of the GBT connection is the slow control system. The 2 bytes in the EC field of the GBT frame payload are routed to a special ASIC for slow control called GBT-SCA. This chip is part of the readout unit board as described. On the CRU main FPGA, the SCA communication is implemented as part of the GBT VHDL module. The GBT-SCA ASIC features many communication modules, including a variety of GPIO, ADC, and DAC pins, as well as I²C, SPI, and JTAG masters[13]. These modules are linked to different components of the regional card. Communication between the regional FPGA and the GBT-SCA is done utilizing the High-Level Data Link Control (HDLC) serial protocol. This protocol is command-based. Rather than reading and writing straight to registers, transactions include a command ID, a transaction ID, and data if the command demands it. Command IDs specify what the GBT-SCA chip will perform, for example writing or reading registers or performing operations. Every command transaction returns a package with the same transaction ID. The return packet comprises status info and returned data if there is any. The IC slow control field is used for accessing the GBTx registers, for setup and monitoring. This field may also control the laser transceivers using a master communication module on the GBTx chip, accessible via its registers.

E-links

The GBTX chips on the regional cards communicate with the local cards using the standard GBT frame mode architecture. It consists of connecting the GBTX and the regional and regional FPGAs through duplex electrical serial lines (e-links). Each GBT bi-directional optical link of the readout chain is made up of 10 serial e-links (8 local e-links + 2 internal regional e-links).

Each of these e-links consists of three signal lines (differential pairs):

- Differential Clock line (dClk+/dClk-): Clock driven by GBTX to the local/regional FPGA
- Differential Downlink data output (dOut+/dOut-): Data from GBTX to the local/regional FPGA
- Differential Uplink data input (dIn+/dIn-): Data line from the local/regional FPGA to GBTX

Figure 10 represents the standard GBT frame mode topology between the GBTX chip and the readout electronics using e-links.

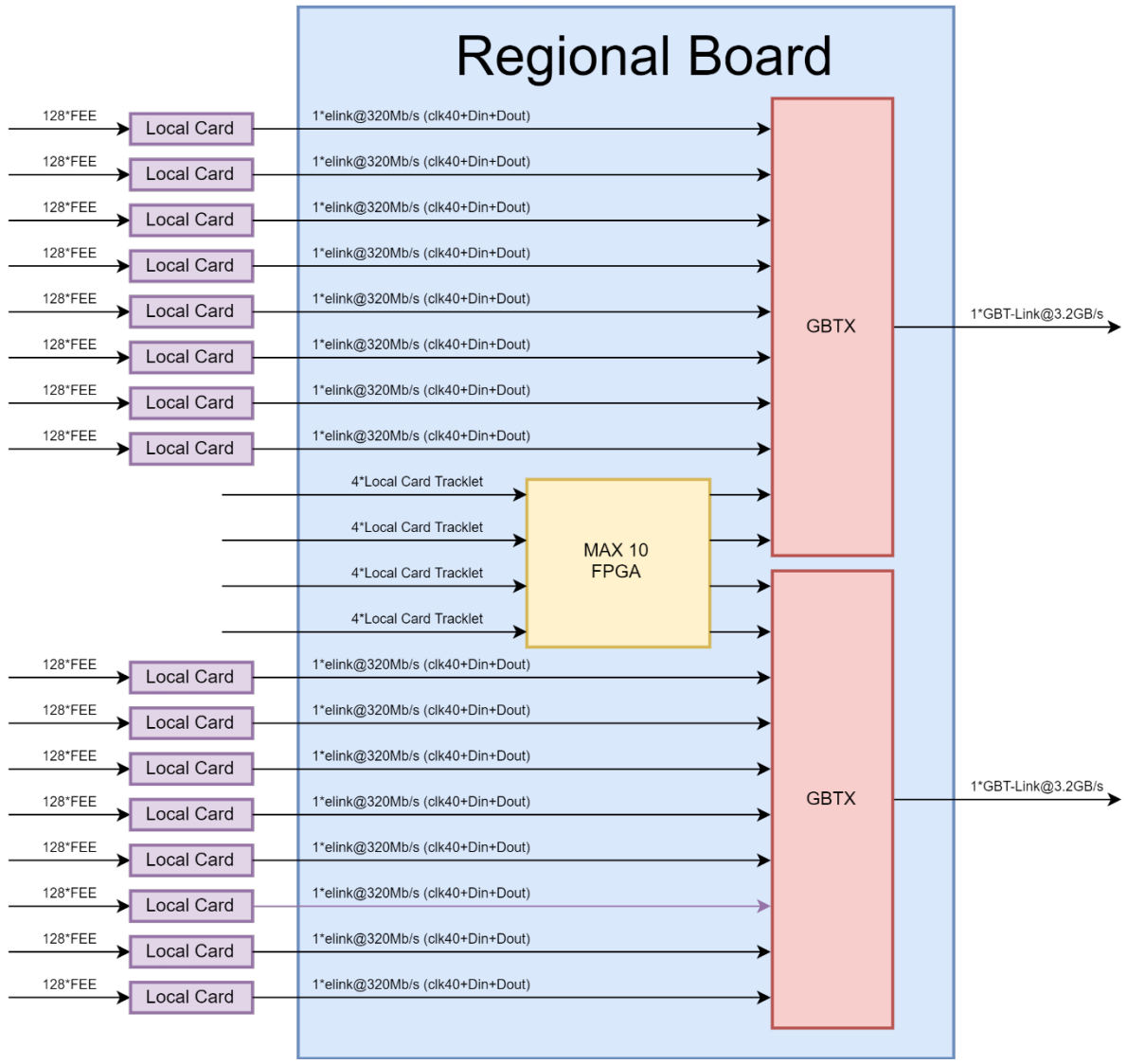

Figure 2.5: Geometry of the readout electronics (to be changed later)

The maximum data rate in the e-links is 320 Mb/s, with a maximum of 2 e-links per group. As already mentioned earlier, each e-link is composed of one differential clock line (dClk+/dClk-), one differential downlink output (dOut+/dOut-), and one differential uplink input (dIn+/dIn-). Thus, the maximum number of differential e-link signals per group is 3 x 2 = 6, equivalent to 6 signal pins per group. Overall, a total of 6 x 5 = 30 configuration pins are dedicated to the e-links.

To provide the greatest possible signal quality and transmission reliability, the physical e-link connections are assumed to be differential transmission lines with a differential impedance of 100 Ω and a suitable termination line at the receiver end. The e-link receivers have built-in 100 Ω terminations that can be disabled if necessary. The e-link signal drivers and receivers that are not being utilized in the readout chain are shut off to minimize the power consumption (I/O power is a significant part of the total GBTx power consumption).

2.5 Common readout unit

Besides the PCIe, which utilizes a 100 MHz onboard crystal oscillator, the main clock tree is intended to utilize a single reference clock for all communication lines of the CRU. The CRU board can either be used in independent mode with a 40MHz onboard crystal oscillator or with a recovered clock retrieved from the TTS optical link. The TTS transceiver, on the other hand, requires a steady 240MHz reference clock before initialization, this is produced locally by a SI5344 Phase Locked Loop (PLL). The clock recovered from the FPGA is transferred to a high-performance SI5345 PLL for jitter attenuation after it has successfully been locked to the incoming stream. The cleaned clocks are then utilized to operate the FPGA logic and the GBT. The SI5345 PLL uses I2C communication to switch between local and recovered clock modes. The clock generated by the 100 MHz onboard crystal oscillator is utilized to operate many features of the FPGA, which includes initialization and hardware monitoring.

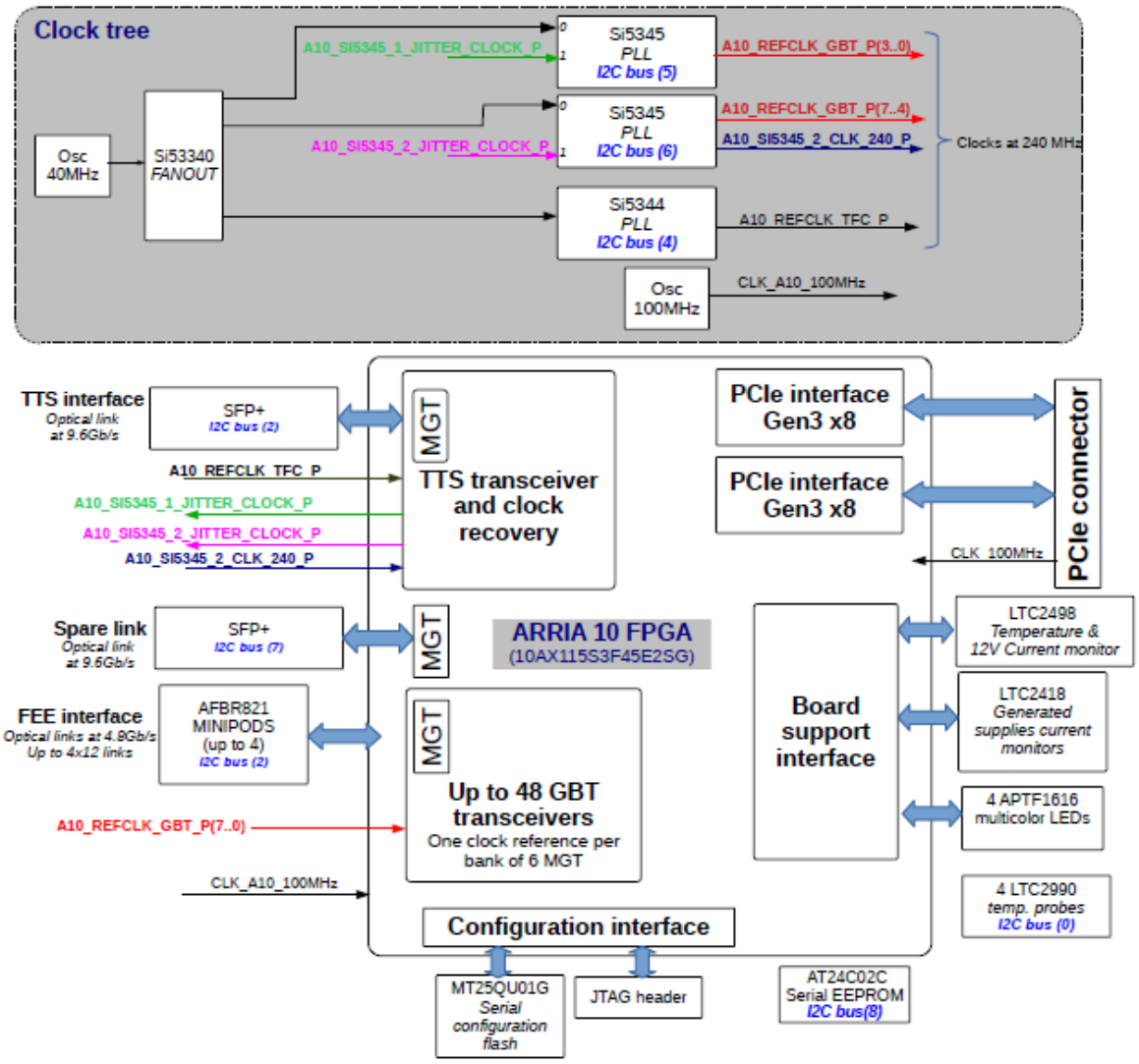

Figure 2.6: CRU hardware overview. The clock tree as well as the FPGA and its interfaces with the different components of interest are shown [36].

Intel's ARRIA10 FPGA is used (10AX115S3F45E2G). It has two Small Form Pluggable (SFP+) connections. Only one of the two SFPs is utilized for the TTS connection; the other serves as a backup. The connections to the front-end electronics are ensured by up to 4x12-channel bi-directional 10.3125 Gb/s optical transceivers (mini-pods [5]). ALICE only has two mini-pods to connect to 24 front-end connections, except for the TRD detector, which does not utilize the GBT protocol and requires 36 connections and three mini-pods.

The CRU is attached to the PCIe edge connector on the rear end and provides a twin gen3 x8 PCIe interface. This interface is timed by a 250MHz reference clock supplied through the connection. The FPGA is also linked to board support functions such as temperature and current sensors, as well as an EEPROM with a unique identifier assigned by the manufacturer during board construction. I2C, or Serial Peripheral Interface, is used to communicate with various peripherals (SPI). There is also the option to control multi-color LEDs, which is essential for easily locating a single machine in a server farm for maintenance purposes. Finally, the FPGA may be programmed using either a JTAG probe, which is useful for debugging software in the lab, or a Quad SPI flash. The latter may be remotely modified over the PCIe interface, allowing for on-site updates. Figure 2 depicts a functional overview of the hardware emphasizing the characteristics utilized in ALICE CRU. The clock tree, as well as the FPGA and its connections with the different components of importance, are shown.

2.6 Timing and trigger system

2.6.1 Central Trigger Processing

2.6.2 Local Trigger Unit

The Local Trigger Unit combines the functions of transmission of trigger signals and emulation of the CTP for use in detector development, in a way similar to that implemented in the current LTU [23]. The LTU (Fig. 4.2) will have the possibility to send trigger signals to detectors via the GBT or the TTC protocol. For the GBT there will be ten separate bi-directional GBT links that can also be used for upstream BUSY collection. In the TTC case, the LTU optical links will provide the optical signal according to TTC protocol, and BUSY is propagated by dedicated LVDS cables. In addition, there will be provision for a clock, orbit, and external trigger inputs. Monitoring and control will be provided by a 1Gb/s optical Ethernet link using the bus protocol.

Each bi-directional GBT optical link of the readout chain is made up of 10 serial electrical links (8 locals + 2 regionals), with both regional serial electrical links data primarily used to identify which of the local events belong to the same bunch crossing and carry strip patterns data

2.7 Detector control system

The MID readout process is monitored and controlled by the ALICE Detector Control System (DCS). The DCS system accesses the readout electronics via the FLP and CRUs through a network connection.

One of the protocols considered for the communication between the CRU and DCS is called ALF (On the CRU side) and FRED (On the DCS side). This protocol is based on Distributed Information Management System (DIM). DIM is a communication system for distributed/mixed environments, originally developed for one of the experiments of the Large Electron-Positron Collider, an earlier particle accelerator at CERN[14]. It provides a network transparent inter-process communication layer. The FLP host computer runs a DIM server, which acts as a bridge between the DIM network and the CRU driver, allowing DCS to communicate with the CRU from the control center without physical access to the CRU host computer.

The DCS data is extracted from the data stream and sent to the ALF (Alice Low-Level Front-end) interface, which publishes the data to the upper layers of the software. ALF can also receive commands and converts them to data words to be sent to the front-end electronics. To keep the ALF detector neutral, its functionality is restricted to the basic I/O operations. In the current implementation, the ALF can read/write registers implemented on the front-end modules and publish the data using a DIM service. The data published by ALF could be single values or blocks of data prepared by the electronics modules.

2.8 Online Offline computing system

2.8.1 First Level Processor

2.8.2 Event Processing Node

The 80bit data field is used for generic transmission of data, having an associated bandwidth of 3.2 Gb/s. The data field is fully available to the user via the flexible E-links and is fully protected by the FEC. Data transmitted has fixed latency in both directions enabling its efficient use for trigger information and timing control.

2.9 References