ALICE Upgrade

(CERN LHC)

Birmingham, Liverpool,

STFC-Daresbury

Nuclear Physics Community Meeting.
University of Warwick, January 2016

UNIVERSITY OF BIRMINGHAM

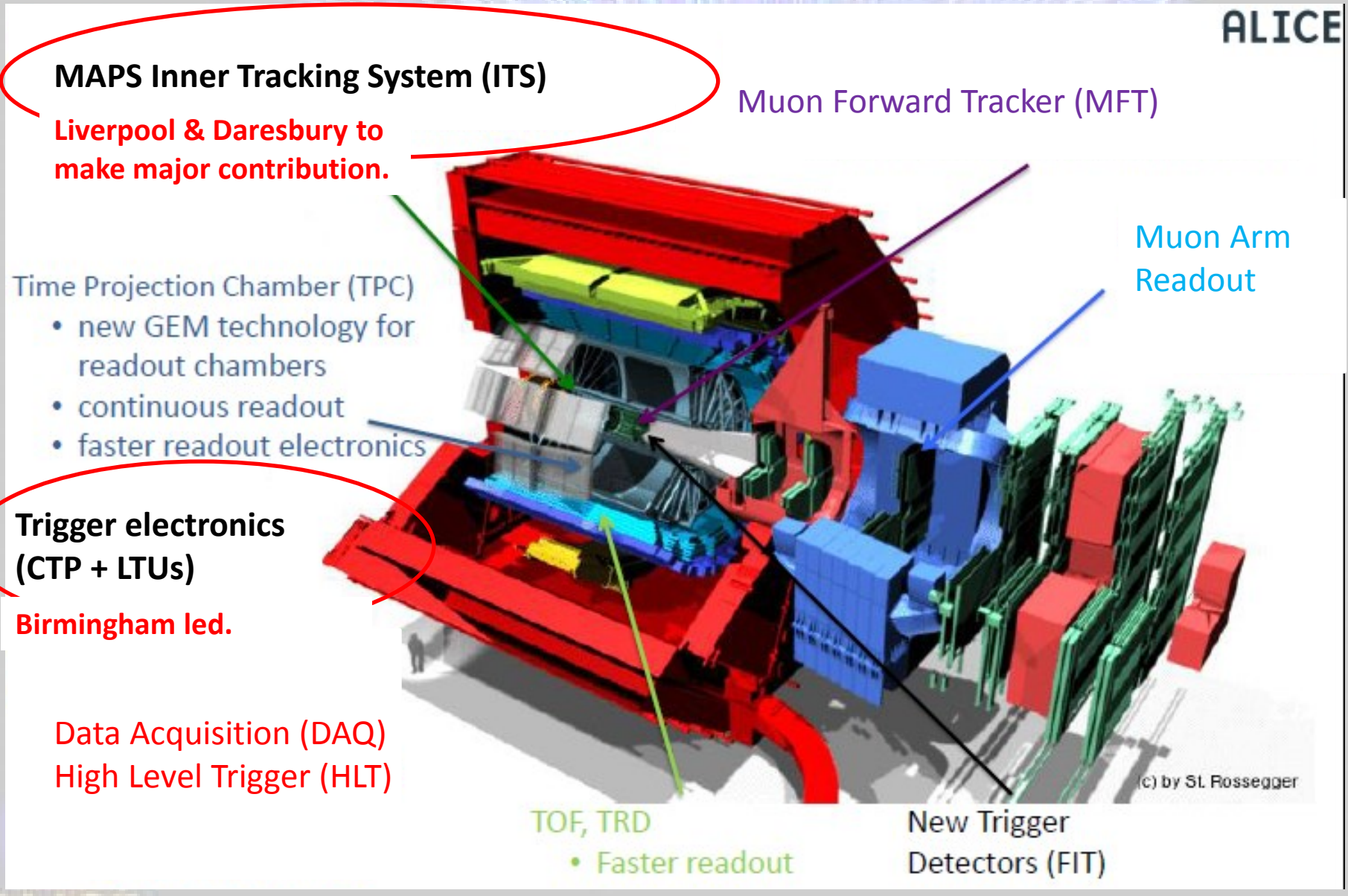
UNIVERSITY OF LIVERPOOL

Science & Technology Facilities Council
Daresbury Laboratory

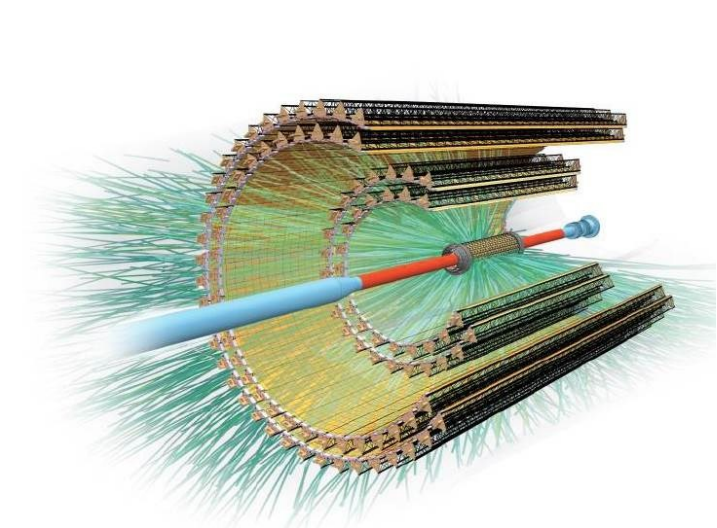
ALICE Status and Plans

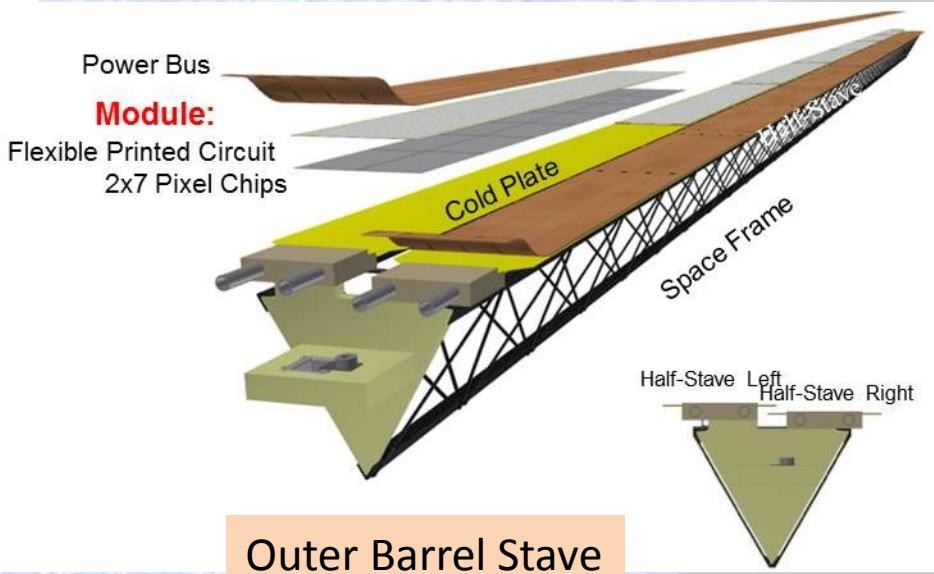
- LHC RUN1 (2010-2013) – **probe QGP with u, d, s quarks**
  - Lot's of exciting results
  - 139 papers so far
  - High impact (average of 75 citations per paper)
  - After the 4 Higgs discovery papers, 3 of the next 4 highest cited physics papers from the LHC are from ALICE.
- RUN2 (2015-2018) – nearly double the energy
  - Plan to take 10x stats of RUN1 **– probe QGP with c quarks**
  - Already off to a great start with successful lead run in November
- **Long Shutdown 2 (2019-2020) – install upgraded detector and systems**
- RUNs 3&4 (2021-2029?) – 10x intensity
  - Plan to increase stats by another 10x (i.e. 100x RUN1)
  - New inner detector **– probe QGP with b quarks**

Summary of Upgrades



ITS Upgrade Status





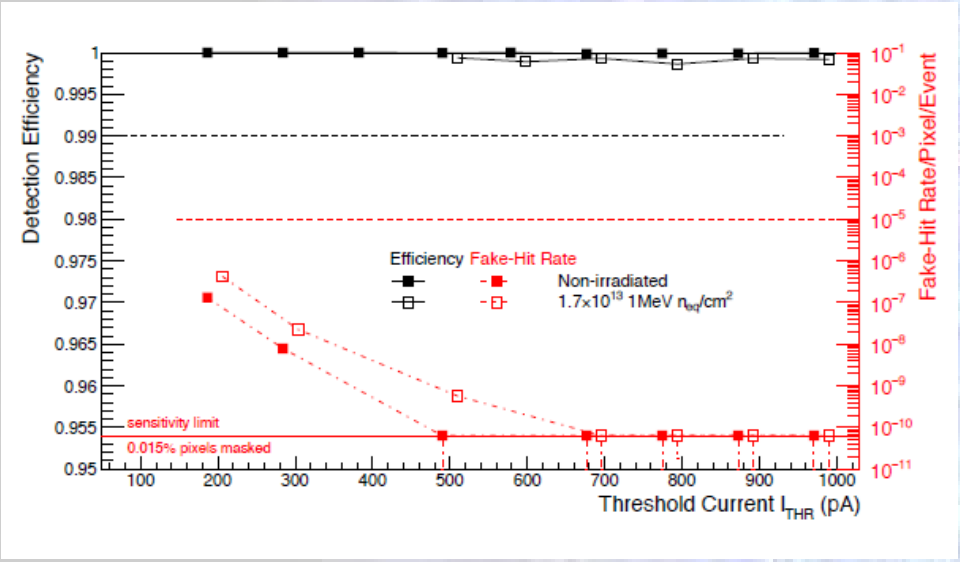
Outer Barrel Stave

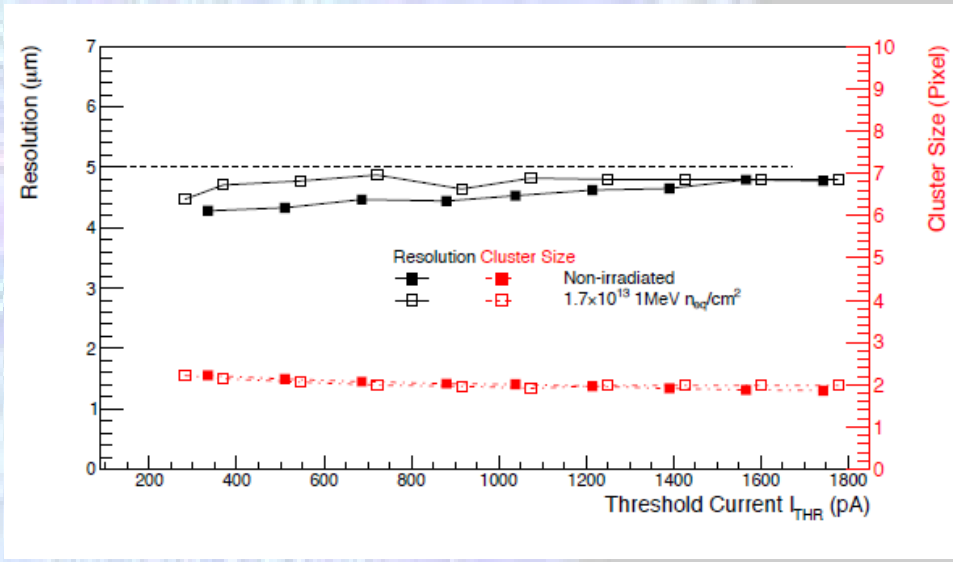
- 7-layer barrel based on CMOS sensors
- Radial coverage 22 – 400 mm
- Total active area ~10m^2
- ~ 24,000 pixel chips (12.5 G pixels in total)
- Radiation ~ 2.7 Mrad (~ 1.7x10^{13} 1 MeV n_{eq} /cm^2)

Lots of work and testing being carried out, overall project on schedule.
No time to give break-down of progress so just take one example → New CMOS pixel chip

Test beam results from proto-type chip version 2 (June 2015)

Efficiency, fake hit rate, resolution, and cluster size measurements at CERN PS (5-7 GeV pions)





ε_{det} > 99% at λ_{fake} << 10^{-5} / event / pixel

$\sigma_{det} \approx 5$ μm is achieved before and after radiation

Main parameters:

Dimension: 30 mm x 15 mm, Pixel Matrix: 1024 cols x 512 rows, Pixel pitch: 28 μm x 28 μm

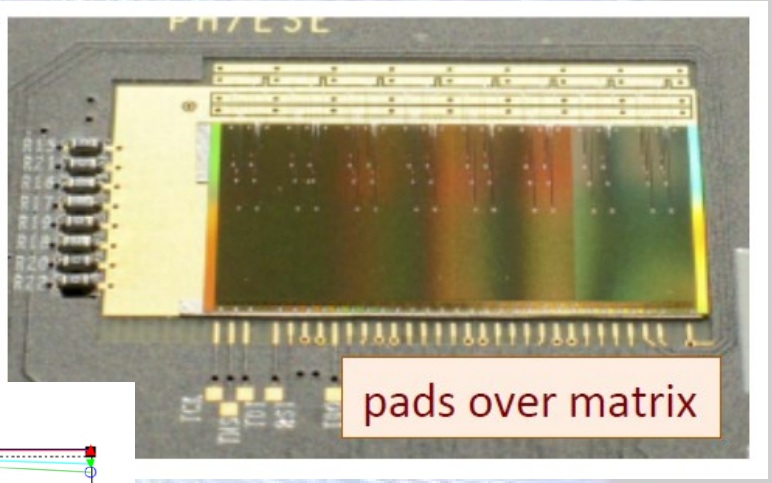
Main difference to final chip:

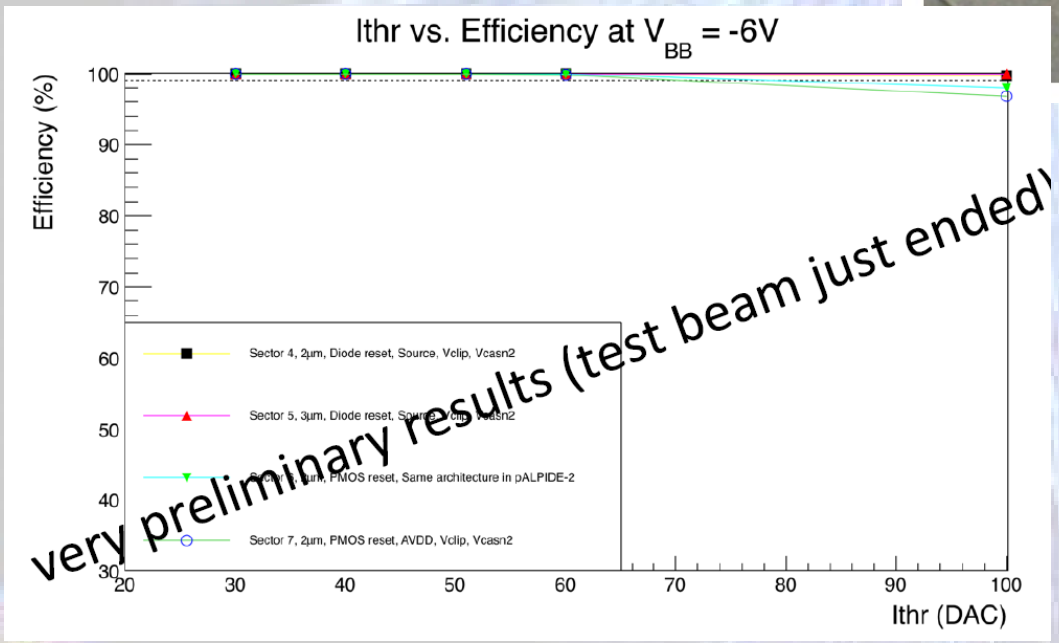
No in-pixel input buffer, No high-speed data output

Results from full-scale proto-type chip pALPIDE-3 (Nov 2015)

Main parameters

- Dimensions: 30 mm x 15 mm
- Pixel matrix: 1024 cols x 512 rows
- Pixel pitch: 28 μm x 28 μm
- Includes all final functionalities
- 8 sectors with different pixels



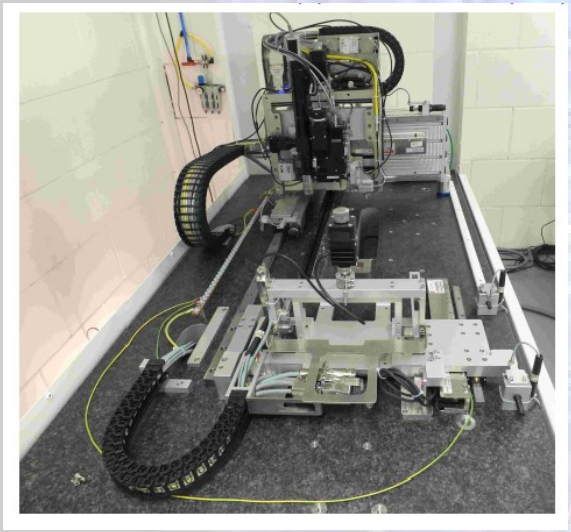


Test beam at BTF (Frascati), 1 GeV/c electrons

- **Final proto-type chip exceeds ALICE requirements**.
- Design of final ALPIDE chip will be finished at the end of January 2016
- Pre-series production starts this February.
- **ITS on schedule**.

UK ITS Status – Liverpool/Daresbury

ITS module assembly machines: custom made machine for semi-automatic procedure.
Tender completed and first proto-type to be delivered to CERN in February 2016



6 machines ordered
Inner Barrel: CERN,
Outer Barrel:
Liverpool, INFN (Bari), Strasbourg, Pusan, Wuhan

Machine expected to be delivered to Liverpool in July/Sept this year.

Major issue for UK: Project awarded on the assumption of vital effort from cross-community personnel, which didn't materialise (project has a short-fall of about 5 FTE).

Working with STFC and key stakeholders to try to resolve this problem asap (manpower shortage now becoming urgent).

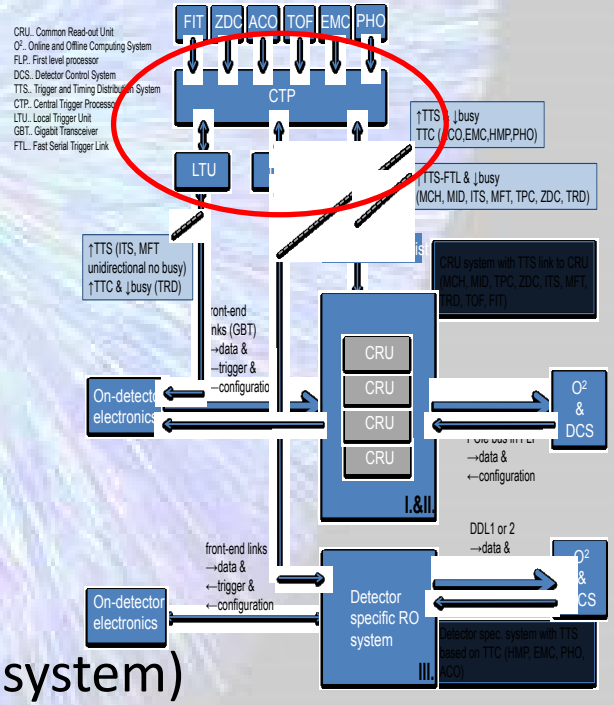
Summary of ITS Status

- ITS project as a whole going well and on schedule.
- Final chip proto-type exceeds ALICE requirements
- Construction centres (inc. Liverpool and Daresbury) need to start preparing clean rooms and production techniques.
- UK Manpower issue needs to be resolved urgently (work with STFC and key stakeholders).

Trigger Upgrade

Key requirements:

- Interaction Rates: 50 kHz for Pb-Pb, and up to 200 kHz for p-p and p-Pb
- 2 modes of running for detectors: triggered and continuous
- 3 different trigger latencies (LM, L0, L1)
- **No Trigger Dead-time**
- 3 types of trigger distribution
  - Directly on detector (ITS detector)
  - Via Common Readout Unit (CRU)
  - Via detector specific readout system
- 2 types of link layer (both optical)
  - GBT (PON) for upgraded detectors
  - TTC system for old detectors
- 14 detectors (10 with GBT system, 4 with TTC system)
- 6 Triggering detectors (FIT, ACO, EMC, PHO, TOF, ZDC; 22 inputs)
- Trigger system latencies as short as possible (< 200 ns)

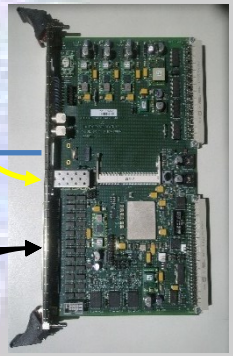


Design Proposal for Trigger System

A Central Trigger Processor (CTP) board → A CTP Fan-out board → 14 Local Trigger Units (LTUs) [1 per sub-detector] + duplicate setup in Birmingham Trigger Lab at CERN + spares (all boards are 6U VME-type boards but VME used for power only)

DAQ PC in UX25-CR4
(PCI40 board)
control and monitor

Fan-out board (6U VME format)



CTP board
(6U VME format)

Busy/Throttling

GBT/TTC optical links

Low Latency Interface

Metallic connection

L0 trigger
over copper cable

TTC TTC TTC TTC TTC

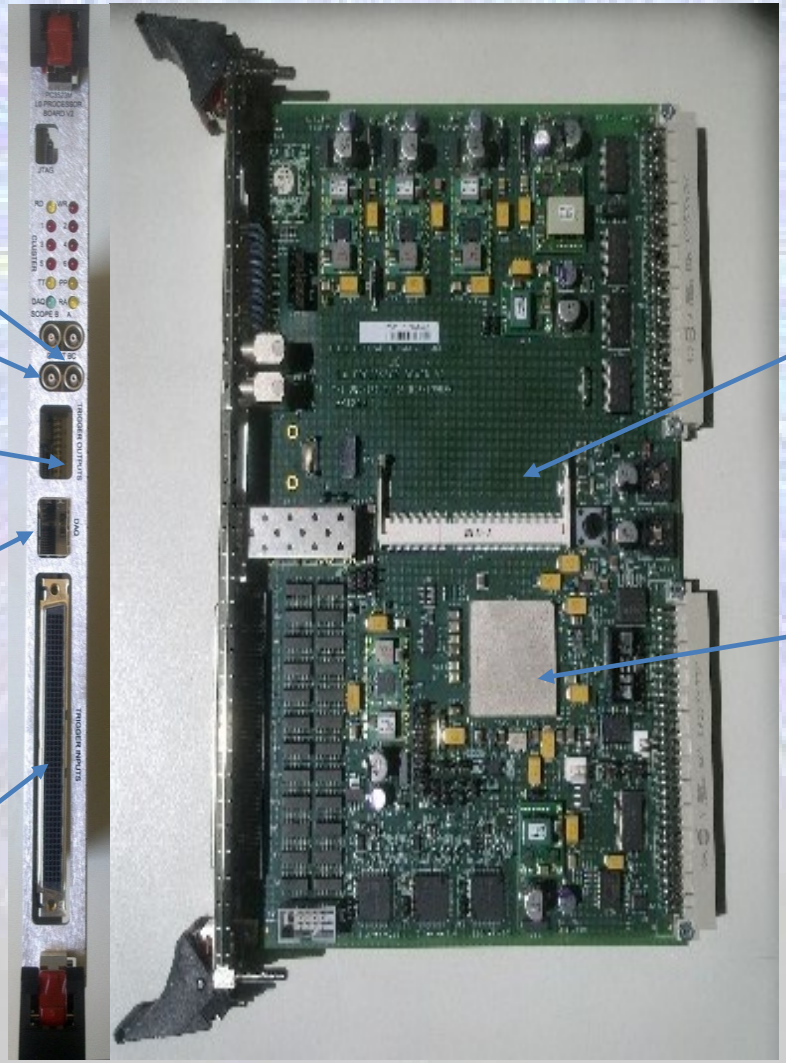
LTU + TTCex boards (TTC drivers)

LTU boards (GBT/PON drivers)

CTP prototype board

(also designed as LTU pre-prototype)

Successfully tested in ALICE cavern during 2015 p-p and Pb-Pb date-taking.



BC input (ECL)

ORBIT input (ECL)

SAMTEC FireFly cable
- 12 diff. links

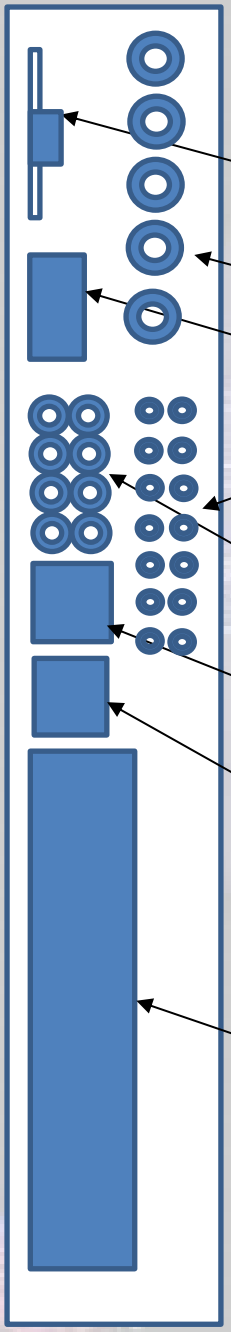
SFP+
- link to DAQ
- (optical link)

96 LVDS I/O
- Trigger inputs
- BUSY inputs
- LM output

2 GB DDR3 memory

Kintex-7 FPGA

LTU Board Design



USB-JTAG (programming of FPGA and SPI memory)

5 x LVDS LEMO (2x LM/L0 out, BUSY in, BUSY out, Fast LM in)

PM bus connector (voltage and temperature monitoring)

14 x LEDs

8 x Lemo 00 B (BC in, ORBIT in, Scope A out, Scope B out, TTC-A out, TTC-B out, Pulser in, Spare in/out)

SAMTEC FireFly (interface from CTP)

SFP+ for IP bus (it must be separate as SFP for RJ45 has wider end of SPF plug-in module -> see slide 12)

2x5 SPF+ (10 x GBT or 10GPON) optical connectors

LTU Front Panel

Single 6U VME type board but with double slot width front panel

Backwards compatible with old TTC system

Trigger Status

A huge amount of development and testing has taken place in 2015 but no time to talk about it.

- Prototype boards built and successfully tested
- Timing and error rates of CTP-fanout-LTU system successfully tested
- LTU and CTP designs (almost) finalised
- Trigger protocols and data format proposed and presented to collaboration

Next six months

- CTP & LTU Design Review to take place at the end of this month
- LTU schematic capture planned for February 2016
- LTU PCB layout (Rutherford Lab) planned for April 2016
- Pre-production planned for July 2016 (3 boards for testing)

Thank you