Trigger System

Design Review

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1. Contents

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2. Document History

Version	Date	Editor	Comments
1.0	15/1/16	D. Evans	First draft uploaded on to Trigger Design Review Indico page
1.0	21/1/16	D. Evans, M. Krivda, R. Lietava, O. Villalobos Baillie	Document modified to give more information and a general introduction to the Trigger system used in Runs 1 and 2 (following suggestions from Alex Kluge).
2.0	23/02/16	RL	Implementing review
2.1	06/04/16	RL	Marian's comments implemented
2.2	08/04/16	RL	Anton's comments implemented
2.3	11/04/16	RL	Orlando's comments implemented
2.4	12/04/16	DE	David's comments in docx
2.5	13/04/16	RL	Combining David with 2.3
2.6	20/04/16	RL	Detector's chapter
2.7	25/05/16	DE	Additional info on TRD, Gantt chart added plus improved format.
2.8	03/05/16	DE	Additional chapter on Busy, new fig 5.1, updated milestones and Gantt, format errors corrected. HB protocols updated.
2.9	09/05/16	DE/RL	Minor changes to throttling section and Tables 5.1 and 6.2
3.0	15/07/16	RL	Comments from EDR
3.11	15/07/16	RL	TRD chapter updated after discussion with TRD
3.12	15/08/16	DE	Milestones updated
3.13	21/08/16	RL	TRD section updated. Clock section added.
3.14	21/08/16	OVB	General comments
3.15	21/03/17	RL,MK	Latency correction, small modifications
3.16	07/04/17	RL,MK	CTP readout GBT link data specified
4.0	30/05/17	RL	Trigger Type size increased

3. Definitions and acronyms

ADC	Analogue to digital converter.
BC	Bunch Crossing (clock) - the 40.08 MHz clock, locked to the LHC machine cycle, used to synchronise the pipeline processing system.
BUSY	Signal generated by a detector to indicate that it cannot accept another trigger.
DM	Detector Mask (bitwise mask of detectors in trigger data).
CRC	Cyclic Redundancy Check on FPGAs
CRU	ALICE Common Readout Unit.
CTP	Central Trigger Processor - electronic board that receives inputs from ALICE trigger detectors and generates **LM**, **L0** and **L1** trigger decisions for all detectors.
DAQ	(ALICE) Data Acquisition system.(Run2).
DCS	(ALICE) Detector Control System.
ECL	emitter-coupled logic connector
ECS	(ALICE) Experiment Control System.
FLP	First Level Processor (PC in which CRUs are connected).
FMC	FPGA Mezzanine Card standard connector.
GBT	GigaBit Tranceiver.
HLT	(ALICE) High Level Trigger system.
LEMO	push-pull connectors made by LEMO.
LM	Level-minus trigger.
L0	Level-0 trigger.
L1	Level-1 trigger.
LED	Light Emitting Diode (indicator).
LTU	Local Trigger Unit (board).
LVCMOS	Low voltage CMOS

LVDS	*Low Voltage Differential Signalling* - a standard differential signal format.
NRZ	Non Return to Zero (signal format).
O2	Data acquisition system (Run3).
PLL	Phase locked loop.
PON	TTC 10G-PON.
TB	ALICE Technical Board.
TIM	Trigger Input Mark (bitwise mask of trigger inputs in trigger data).
TTC	Timing, Trigger and Control (system).
TTCex	TTC Encoder/Transmitter (board).
TType	Trigger Type (trigger data).
U	Unit of height in the standard 19" rack (1U = 4.36 cm).

4. Introduction and the current ALICE Trigger System

4.1 Introduction

The ALICE Upgrade will require a very different triggering strategy to the current one and hence a new Central Trigger Processor (CTP) will be required. The CTP will manage a system of detectors with markedly different properties. The majority of detectors, which will read out the nominal interaction rate, will be dead-time free. However, in order to provide backwards compatibility to detectors not being upgraded, the trigger system must also cope with detectors that will still have dead-time during the readout.

This document is prepared for the *ALICE CTP and LTU Design Review*. It sets out the proposal for the main design components and protocols of the upgraded ALICE trigger system and the schedule for design, construction, testing, and commissioning of the system. A brief description of the current trigger system, used in Runs 1 and 2, is outlined in this section, which we hope will be useful to the external reviewers. This document will then outline the requirements and our proposals for the upgraded trigger system. A section entitled "*The ALICE Trigger System – At a Glance*" is included at the back of the document (section 13) as a quick reference.

4.2 The current ALICE Trigger System

Details of the current ALICE trigger system are found in refs [1-4]. The trigger system consists of a Central Trigger Processor (CTP), plus a Local Trigger Unit (LTU) and TTC [5, 6] boards for each detector. The CTP consists of seven different types of 6U VME boards housed in a single VME crate and controlled, via a VME processor. The signals are distributed to the detectors using the Local Trigger Unit (LTU). Transmission of trigger signals to each detector is mediated by one of these boards. In addition, the boards can be decoupled from the CTP and used to emulate CTP signals for testing purposes (in *stand-alone* mode). Emulation of trigger sequences using the LTU was an important part of the testing and commissioning of detector electronics.

Some of the detectors require a strobe at 1.2 μs after an interaction. To achieve this, the 'fast' part of the trigger is split into two levels: a Level 0 (**L0**) signal, which reaches detectors at 1.2 μs, but which is too fast to receive all the trigger inputs, and a Level 1 (**L1**) signal arriving at 6.5 μs, which picks up all remaining fast inputs. Note that the CTP decisions are made in 100 ns, with the rest of the L0 latency coming from the generation time for the trigger input signals and from the cable delays. Another feature of the ALICE environment is that the high multiplicities of Pb-Pb collisions make events containing more than one central collision difficult to reconstruct. For this reason, 'past-future protection' is an important part of the ALICE trigger. A final level of the trigger (Level 2, **L2**) waits for the end of the past-future protection interval (a programmable interval, set to 100 μs in Run 2) to verify that the event can be taken.

The role of the ALICE trigger system is to combine information from the ALICE trigger detectors (trigger inputs) and the readout detectors (calibration requests, **BUSY**), and to form, in each bunch-crossing (BC) interval, yes/no trigger decisions for levels **L0**, **L1** and **L2**. The decisions are sent to the TTC system, which distributes them to the front-end electronics of the detectors, where they initiate data taking and control the readout. The TTC also receives from the CTP and broadcasts to the front-ends the information about the trigger type, the event identifier and the list of participating detectors.

The algorithms used to form different types of triggers are implemented through trigger-class definitions. *Trigger class* is a basic logic block of the CTP and the hardware provides for a number of classes that are processed in parallel. All trigger-class parameters are independently and fully programmable. The detectors are grouped into detector clusters, each with its own past-future protection period.

The trigger-class definition contains the detector cluster and the required patterns of the trigger inputs for levels **L0**, **L1** and **L2**. A bunch-crossing mask which reflects the bunch "quality" (full, empty, noisy, etc.), a programmable mask, internally generated random, periodical and software triggers could also be included in the **L0** pattern.

The **L0** class-trigger generation may be inhibited by a veto derived from **BUSY** logic, and by the status of the past-future protection logic; the **L0** class-trigger can also be pre-scaled. The **L1** and **L2** decisions, on the other hand, may be inhibited only by the past-future protection.

The **BUSY** logic synchronises the CTP operation with the detector front-end electronics and the DAQ readout chain. The asserted **BUSY** signal indicates that the corresponding detector is not ready to accept another event (e.g. buffers in the front-end are full) and inhibits further **L0** triggers. *The CTP can generate its own dead time after each L0 trigger that will last for up to 2μs.*

The past-future protection logic keeps track of the time since the last significant interaction and determines, for each detector cluster, whether sufficient time has elapsed to avoid pile-up in any of the cluster detectors (and its consequences on the pattern recognition).

In addition to generating the trigger signals, the CTP provides a DAQ with the list of participating detectors for all **L2**-selected events, and a complete record of bunch interactions. These data are archived and can be used for off-line checking of the trigger system, monitoring of experimental conditions such as beam quality, and for calculation of trigger efficiency; the interaction data should significantly simplify the event reconstruction process.

The CTP includes a number of scalers that are used to measure trigger rates and monitor dead time. The scalers are read in regular intervals, the data are processed in real time and the results are written to a permanent storage to be used by the off-line analysis. Any potential problem is reported to the run-control.

The CTP also contains diagnostic, “snap-shot” memories that sample, at full speed, trigger inputs and outputs as well as the data at various points in the processing chain. The data are used for on-line monitoring of the CTP performance and for the luminosity assessment of individual beam bunches.

The interfaces between the CTP and external systems are shown as a context diagram in Figure 4.1 below.

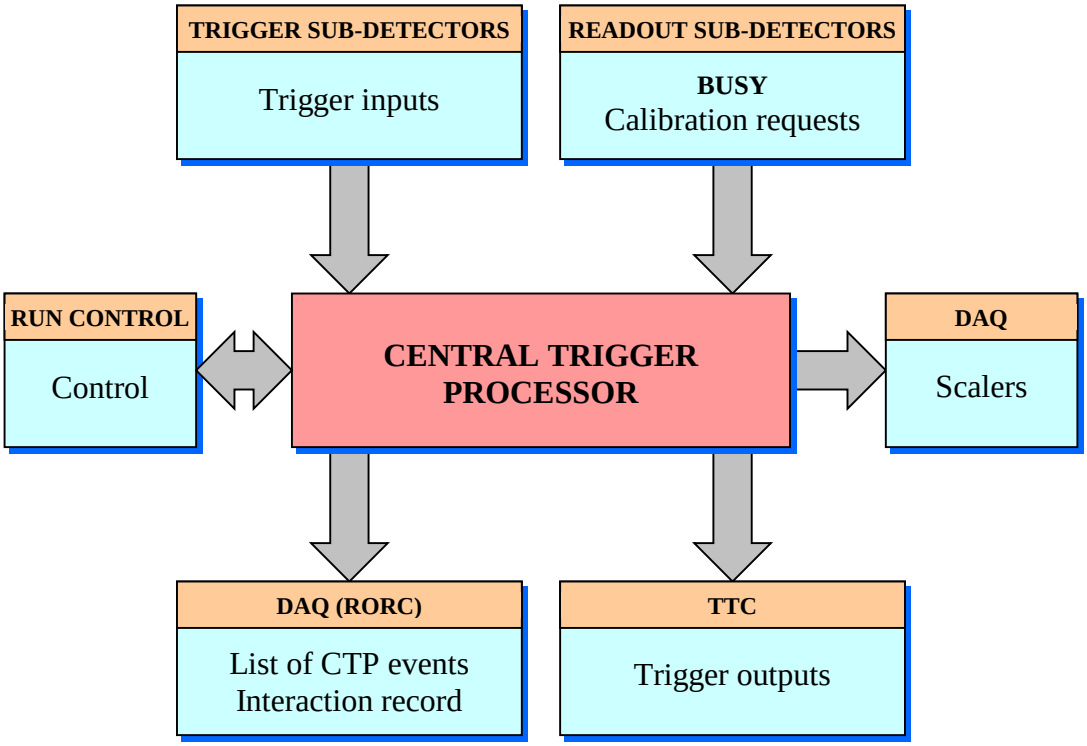


Figure 4.1 Context diagram of the CTP

Trigger inputs related to the same bunch crossing, but generated by different trigger detectors, in general arrive at the CTP at different times. The CTP therefore includes programmable elements that delay the signals that arrive early so they can be aligned in time with those that arrive last.

Calibration requests enable detectors to demand calibration triggers during the physics run (for stand-alone tests, the detectors can introduce their own triggers at the level of their local TTC system). The CTP also provides a *pre-pulse* facility used to generate calibration inputs prior to calibration triggers.

A link to the control system is used to configure the CTP and perform tests. It also carries error and warning massages which emerge from real time analysis of data coming from scalars and diagnostic memories.

Apart from information sent to the DAQ for all **L2**-selected events, the CTP also supplies, in regular intervals, the data via a DDL link.

The **L0** trigger is the only signal transmitted via a dedicated, low propagation delay cable; the TTC system is used to distribute all the other trigger outputs to the front-end electronics of the detectors. For detectors which are not time critical, the **L0** trigger may also be transmitted via the TTC system.

4.3 Modification to the trigger CTP for Run 2

The Transition Radiation Detector (TRD) requires a *wake-up* pre-trigger before it is ready to receive a L0 trigger. During Run 1, this was achieved by dedicated pre-trigger electronics developed by the TRD group that was independent of the CTP. Although a TRD pre-trigger was usually followed by a L0 trigger, it was possible for the TRD to receive a pre-trigger but not an L0. This situation reduced the data-taking efficiency of the TRD and was the main motivation for an upgrade to the CTP for Run 2. For Run 2, we replaced the existing Level-0 (L0) CTP board with a new Level-Minus-Zero (LM0) board. This new LM0 board incorporates a new pre-trigger (which is issued before the L0 trigger), increases the number of trigger physics classes from 50 to 100, and significantly increases the number of allowable trigger inputs. The design of the LM0 board was carried out with the trigger upgrade project in mind and hence the board was designed to have a dual role as both a LM0 board for RUN2 and as a prototype for the upgraded CTP. As such the LM0 board has a number of additional features not required for RUN2 but most of the features required by a CTP prototype.

5. The ALICE Trigger Upgrade Concept

The ALICE Upgrade will require a very different triggering strategy from the current one and hence a new Central Trigger Processor (CTP) is needed. The CTP will manage a system of detectors with markedly different properties. The majority of detectors, which will read out at the nominal interaction rate, are dead-time free. However, in order to provide backwards compatibility to detectors not being upgraded, the trigger system must cope with detectors which will have dead-time during the read-out.

The strategy for selecting events for readout will also be different from that employed in previous runs. Previously, despite the fact that ALICE events are highly complex, the trigger strategy was to combine a Minimum Bias sample with one selected according to thresholds in high E_T (calorimeter triggers), high p_T, or high multiplicity. The strategy for the ALICE upgrade system is to read out all interactions and apply an online filtering in the high level trigger (HLT).

In Run 3 the interaction rates will increase to ~ 50 kHz for Pb-Pb, and 200 kHz for p-p and p-A (and where feasible a safety margin of two is applied in the system design). The aim of the ALICE trigger system is to select essentially all of these interactions; the events are then read out and the event records are sent to the HLT farm for further filtering. To achieve this, the combination of continuous readout detectors and a minimum bias trigger based on the new forward FIT detectors is used, with a few additional inputs to allow for cosmic triggers and calorimeter based triggers to enhance rates for some types of events where the minimum bias trigger is inefficient.

5.1 Trigger Architecture

The overall trigger architecture is shown in Figure 5.1. For Run 3 we will keep the concept of a CTP and LTUs as detector interfaces but advances in FPGA technology mean it is now possible to have all the functionality of the CTP on a single 6-U board. Figure 5.1 shows the six detectors that will deliver trigger inputs to the CTP and the three ways the trigger data will be distributed to the detector FEE. Detectors not upgrading their FEE will have trigger data sent via the TTC system, directly to their FEE. Most of the detectors being upgraded will receive trigger data via a TTC 10G-PON (PON) optical link to their Common Readout Units (CRUs) but some will require a direct link via GBT. Trigger inputs are collected to satisfy three different latencies, giving hardware triggers at three different latencies known as LM, L0 and L1. The maximum latency for the trigger input signals to reach the CTP are summarised in Table 5.1.

Table 5.2 gives a summary for all detectors stating which trigger they require, their maximum readout rate, the trigger distribution method, whether they will use the CRUs and how they deliver their BUSY signal. The LM latency will be similar to that used in Run 2, and is suitable for generating a fast trigger signal for both the TRD and ITS/MFT electronics. An electrical LM signal will be also used by the CPV and HMPID detectors. The ITS will receive its LM trigger via a GBT link. However, it will not be possible to generate an Electro-Magnetic Calorimeter (EMC) signal early enough for the LM trigger, and for this reason the

L0 is retained. The FIT detector is not suitable for cosmic ray triggers. In this case the TOF and ACORDE detectors will be used.

Table 5.1 Summary of trigger inputs

Input Latency	Input to CTP [ns]	Contributing detectors
LM	425	FIT
L0	1200	ACO,EMC,PHS,TOF, ZDC
L1	6100	EMC,ZDC, PHS

Table 5.2 Summary of detector requirements

Detector	Trigerred by ()=optional	Pb-Pb RO Rate [kHz]	Trigger	CRU used	BUSY IN
TPC	(L0 or L1)	50	PON via CRU	yes	PON/CRU
MCH	(L0 or L1)	100	PON via CRU	yes	PON/CRU
MID	LM	100	PON via CRU	yes	PON/CRU
FIT	L0 or L1	100	PON via CRU	yes	PON/CRU
ACO	L0	100	PON via CRU	yes	PON/CRU
TOF	L0 or L1	>100	PON via CRU	yes	PON/CRU
ITS	LM	100	GBT	yes	PON/CRU
MFT	LM	100	GBT	yes	PON/CRU
TRD	LM	39	TTC	yes	PON/CRU
ZDC	L0	>100	PON via CRU	yes	PON/CRU
EMC	L0&L1	42	TTC	no	LVDS
PHS	L0&L1	42	TTC	no	LVDS
CPV	L0&L1	50	TTC	no	LVDS
HMP	L0&L1	7.5	TTC	no	LVDS

The ZDC is optionally available to clean the minimum bias trigger provided by the FIT. Downstream of the CTP, trigger decisions are transmitted to the individual detectors using an upgraded Local Trigger Unit (LTU), as at present. Trigger signals go to every detector, since it is a requirement for each detector, even those where continuous readout is foreseen as the norm, that it should also be capable of reading out in triggered mode. Owing to the reduced

number of trigger inputs with respect to Run 1 and Run 2, for the upgrade it will be possible to implement a lookup-table trigger. The optimal look-up table for Xilinx Kintex-Ultrascale is for eight inputs, however, it is possible to make a lookup-table with more inputs if internal FPGA timing allows it. Due to the continuous readout strategy, there will be relatively few physics conditions defined as combinations of trigger inputs (trigger class), with most events selected by a Minimum Bias trigger with subsequent filtering in the HLT. The selection of readout detectors will be different from previous runs. Whereas, previously, a trigger was successful only if every one of a list of readout detectors is available to read out the data (the list defining a trigger "cluster"), for the upgrade, if a trigger condition is

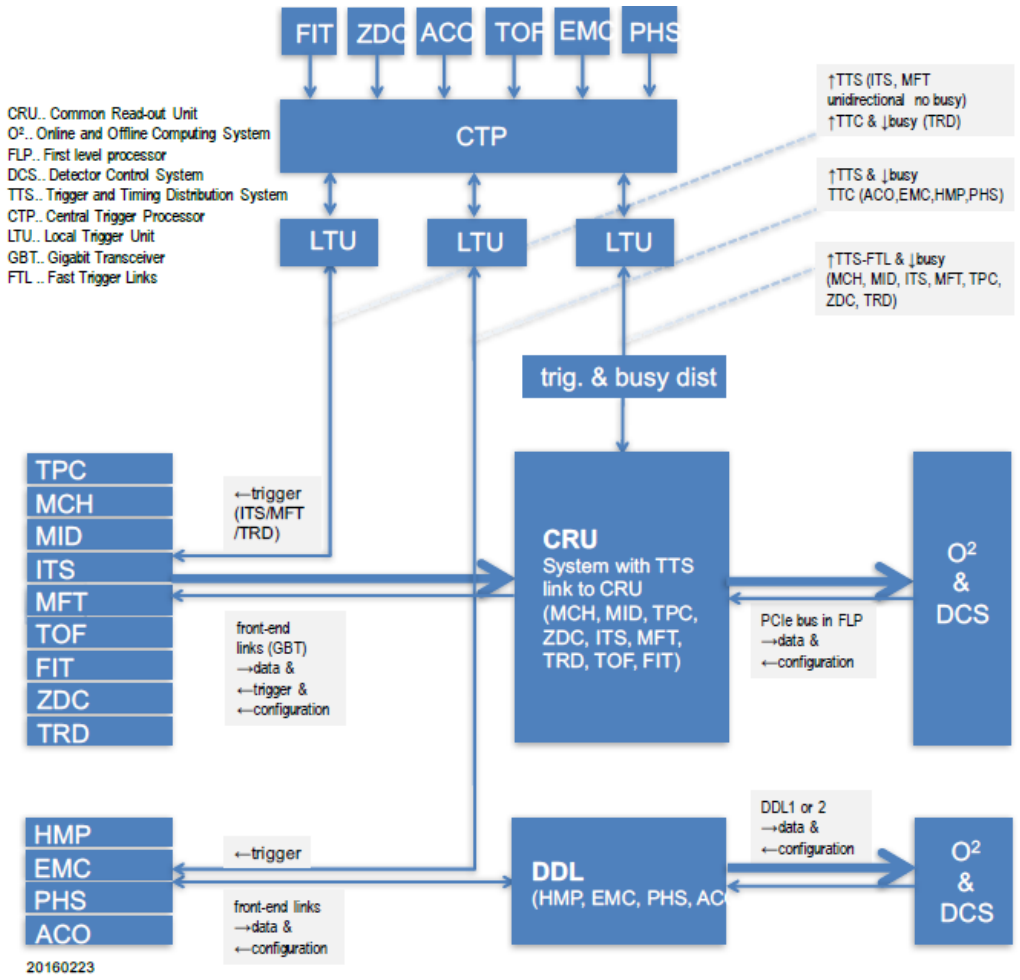


Figure 5.1 Summary of trigger distribution

satisfied, the event is read out with the full set of continuous readout detectors, plus all other available detectors. This strategy in effect treats each detector as a separate cluster, so any combination of detectors could be read out for a given event. In the same time the BUSY requirements of every detector (old readout detectors) can be treated independently of other detectors. It could turn out that this strategy would lead to insufficient numbers of events being read out with useful combinations of detectors, for example TRD, TOF and HMP, which are all used for particle identification. To allow for this possibility, the trigger logic can, in addition, define further clusters consisting of groups of detectors, as at present, and

balance the bandwidth between a free selection of all available detectors and a restricted choice requiring a given combination. A context diagram of the proposed trigger system is shown in Figure 5.2

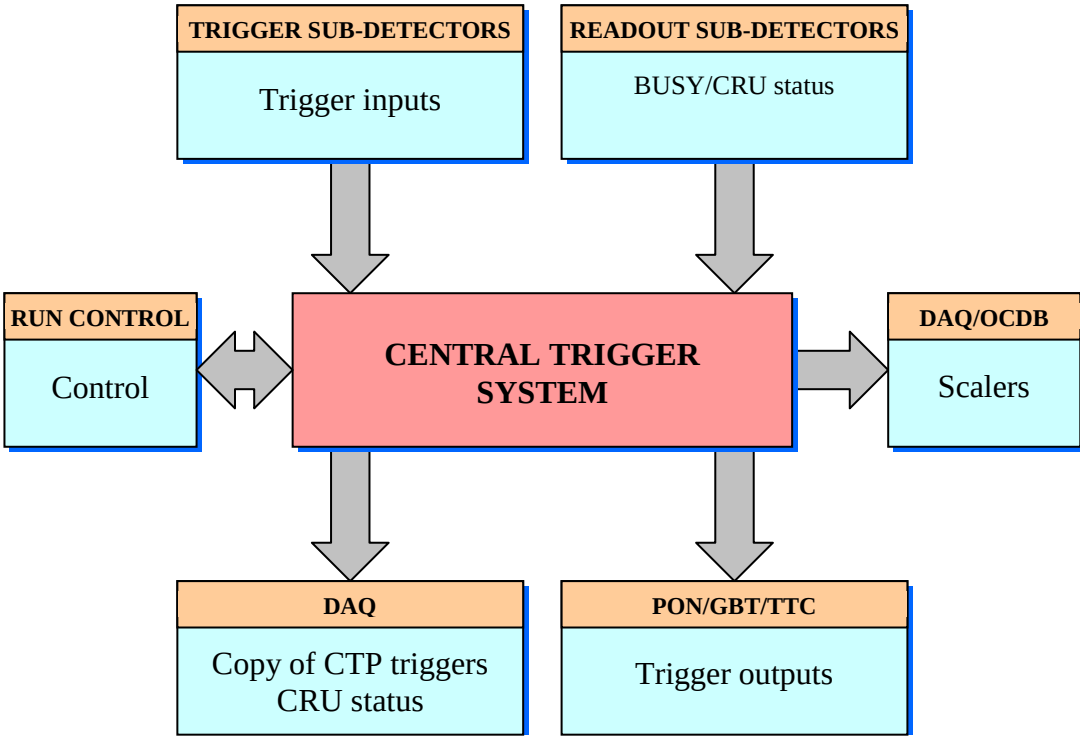


Figure 5.2 Context diagram of CTP

The trigger system itself will consist of a CTP board and a Local Trigger Unit (LTU) board for each detector. The interface between CTP and LTU boards is PON (GBT as a backup solution). All boards will be 6U VME type boards but the VME connectors will be used for power only due to the limited speed of the VME backplane.

A block diagram of the trigger system is shown in Figure 5.3 and a schematic layout is shown in Figure 5.4.

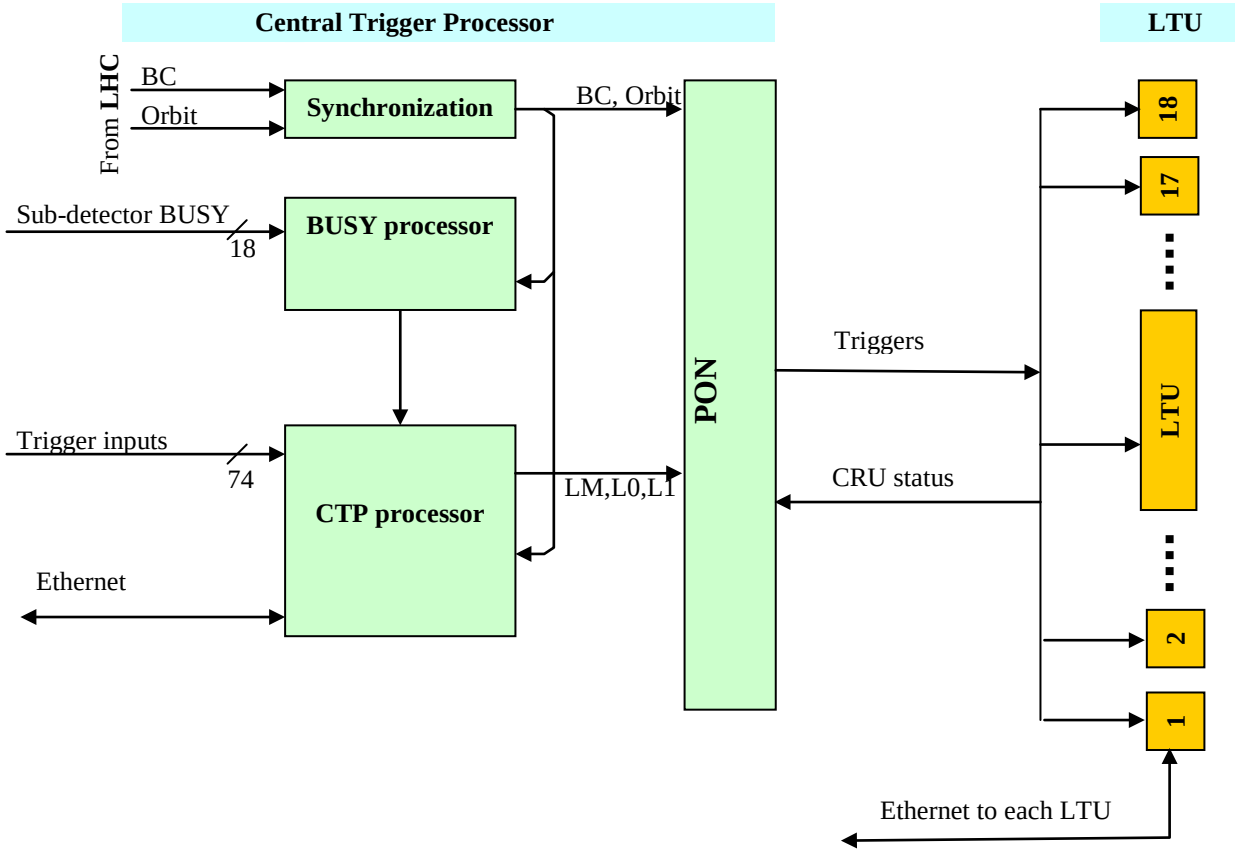


Figure 5.3 Block diagram of CTP and LTU system

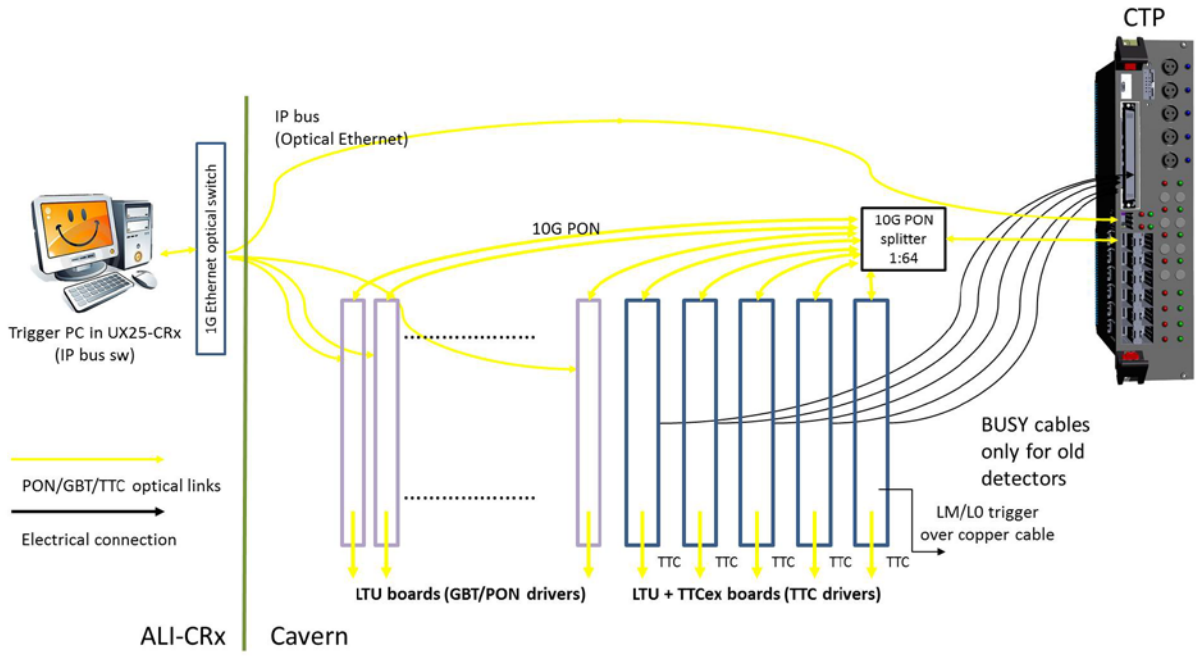


Figure 5.4 Schematic layout of the Trigger System

6. Trigger Protocol and Data Format

6.1 Continuous and triggered modes

The ALICE detectors will use two modes of operation after the upgrade: triggered and continuous readout. The continuous readout of some detectors is a substantial change from current practice. The data are not delimited by physics triggers but are composed of several constant data streams that will be transferred from the detectors to the computing system. The continuous and trigger modes are attributes of the detector and a particular run can contain a mixture of detectors with different modes.

Dedicated time marks are provided by *HeartBeat triggers* (HB), sent nominally every LHC Orbit, containing the BC and Orbit numbers (HBid). The HB period will, however, be a programmable parameter. HB triggers can be either a HB accept (HBa) signalling CRUs to read out or a HB reject (HBr) signalling CRUs to discard data. Thus the HBa/HBr mechanism is logically similar to the BUSY protection in RUN2. The decision on HBa/Hbr is made by the CTP according to the status of the CRUs, see section 6.4 and note [8].

A preloaded sequence of HBa and HBr triggers may be used to effectively downscale the continuous readout detectors if required.

All detectors must be compatible with triggered readout. The CTP will provide one trigger signal with several latencies, i.e. LM, L0 and L1. (Exceptionally two trigger levels may be provided if required by a detector.) Upon reception of the trigger signal, each detector needs to respond and send data corresponding to the trigger time period. (For details see [8].) In triggered mode, the HB trigger serves only as a delimiter of HB time frames.

6.2 Interfaces to detectors

Triggers and trigger data will be distributed to detectors using three different protocols: PON from LTU to the CRUs (GBT as a back-up solution), GBT for upgraded detectors receiving triggers directly (i.e. not through CRUs), and TTC for detectors that are not being upgraded. The full information about the triggered event consists of data summarised in Table 6.1 below. Only part of this information is sent to detector with every trigger. **The trigger data sent to detectors consists of Trigger Type (TType), Bunch Cross Identification (BCID) and Orbit number (ORBIT), 60 bits in total.** The data format for each case is summarised in section 14. The rest of the data from Table 6.1 are sent to O2 only via the CTP readout.

Table 6.1 Summary of trigger data

Data name	Acronym	No. of Bits	Description
Trigger Type	TType	32	Trigger Type e.g. physics, calibration, heartbeat, etc.
Bunch Cross No	BCID	12	Event ID: ORBIT + BCID equates to 4.4 days.
Orbit Number	ORBIT	32	
Trigger input mask	TIM	74	Trigger inputs activated.
Detector Mask	DM	18	Detectors included in event

6.3 Trigger Data Protocol

Detectors fall in to three categories as far as the trigger protocol is concerned. These categories are:

1. Detectors with fast links (PON or GBT) where the latency is not critical
2. Detectors with fast links where the latency *is* critical
    a. TRD trigger via TTC
    b. ITS and MFT trigger via GBT
3. Detectors using the TTC system

For Detectors with fast links where the latency is not critical:

- The trigger and data will be sent as a synchronous message with 60 bits (PON) or 60 bits (GBT) to the CRUs from the CTP ..

For Detectors with fast links where the latency is critical:

- A synchronous trigger message will be sent to the detector Front End at the time of the LM trigger.
- A synchronous message with the trigger data (60 bits) will be sent from the CTP.

For Detectors using the TTC system:

- One synchronous trigger via channel A, sent at LM, L0 or L1 time.
- An asynchronous message in channel B, containing the trigger data (60 bits) sent from the CTP at L1 time.

6.4 Software triggers (Trigger Types)

Software triggers, including calibration triggers, are recognised via Trigger Type (TType) of 16 bits. To date, eleven types of triggers have been defined although this is likely to increase. The current trigger types are summarised in table 6.2.

6.5 Throttling, Busy, and Heartbeat (HB) triggers

Heart-Beat (HB) triggers, containing the HBid, are sent to **all** detectors in **all** modes of operation, even when their status is full/busy, nominally every LHC Orbit.

6.5.1 Detectors using CRUs in Continuous readout mode

The CTP will send Heartbeat (HB) triggers, nominally every LHC Orbit (89μs), to the CRUs via the LTUs. The HB period, however, will be a programmable parameter.

6.5.1.1 Heartbeat Triggers

Two types of HB triggers are envisaged, HB-accept (HBa) and HB-reject (HBr) depending on the status of CRUs. The HBa and HBr triggers will contain the HBid and a bit to signify whether it is a HBa or HBr.

6.5.1.2 CRU HB acknowledge message

After receiving a HB trigger, each CRU will transmit a HB acknowledge message to the CTP, via their LTU.The payload of message is defined in [8], table 7.The CTP will collect the HB acknowledge of all CRUs, within a time-frame of 8 Orbits and form a HB map.

Table 6.2 Trigger types

1	Orbit	Orbit
2	HB	HB
3	HBr	HB reject
4	HBc	Health check
5	Physics	Physics trigger
6	PP	Prepulse
7	Cal	Calibration
8	SOT	Start of Triggered Data
9	EOT	End of Triggered Data
10	SOC	Start of Continuous Data
11	EOC	End of Continuous Data
12	TF	Time Frame delimiter
13	TOF	TOF special trigger to signal transferring data from FM to DRM
14	SYNC	Synchronisation, e.g. for TPC
15	RST	Reset, e.g. for TPC
16	Spare	Spare
⋮	⋮	⋮
32	Spare	Spare

6.5.1.3 HB Map

The HB acknowledge arrival time is programmable, but nominally it could take up to eight Orbits for the CRUs to send their HB acknowledge and thus the CTP shall maintain three HB maps at any time; one for the current HB and one for each of the two previous HB time frames. The CTP shall sort the HB acknowledge messages to the correct HB map but have a timeout of two Orbits for any given HB acknowledge.

6.5.1.4 Throttling

The CTP will use a pre-loaded set of conditions on the HB map to determine whether to transmit a HBa or HBr trigger after the next HB timeframe (nominally one Orbit). Based on this information, the front end accepts or rejects the time frame. In the detector readout document [8], this is referred to as the *continuous scaling* mode of throttling. (More complicated modes are discussed in the document.) Note, due to the latency of the CRU status message, CRUs must be able to accept further HBa triggers even when their status is full. Additional rejection of discarded HB frames at the FLP, by O2 according to information from CRU statuses received by O2 from CRU and CTP readout, is necessary

6.5.1.5 Fixed scaling of continuous readout detectors

A different operation scheme is the scaling mode which consists of sending a predefined sequence of HBa and HBr triggers, where the CTP will be able to downscale the data flow

rate of the CRUs. A different predefined sequence may be uploaded to the CTP during a run but HBa triggers will always be sent in pairs to allow time for the TPC readout. Hence such a sequence could be: HBa, HBa, HBr, HBr, HBr, HBr, HBa, HBa HBr, HBr, etc.

6.5.1.6 Additional HB Decision option

In addition to the synchronous HB triggers, an asynchronous HB Decision message could be sent to all CRUs when a pre-loaded set of conditions on the HB map is met. The HB decision message contains a bit for the positive/negative decision and the HBid. The CTP shall guarantee to send only one HB Decision per HB. However, additional rejection of discarded HB frames, by the O2 at the FLP, will be necessary due to the latency between the CRUs and CTP. This mode is employed provided it is not a significant complication to the CTP firmware.

6.5.2 Detectors using CRUs in Triggered mode

All detectors must be capable of operating in trigger mode. In this case, triggers are sent, via the LTUs, to the CRUs. If a triggered detector becomes busy, its CRU will inform the CTP via an acknowledge message, using the same channel and format as for the HB acknowledge message, and the CTP will stop sending triggers to this detector until a not-busy status is received. However, due to the latency of the CRU status message to the CTP, these detectors must be able to handle further triggers after their busy is set. However, the CTP will send HB triggers (as well as standard triggers) in triggered mode, even if detectors become Busy.

6.5.3 Detectors using the current TTC system

Detectors using the current TTC system will provide one Busy signal to their LTU via a LVDS Lemo cable or by an optical GBT link. The CTP will ensure that detectors are protected for the time interval of Busy propagation from detector to LTU. All detectors using the TTC system, except the TRD, will receive the HB frame id in the TTC message. The TRD will receive its HB triggers via its CRU.

6.5.4 Detector readout during Run 3 and Run 4

The ALICE electronics coordinator and DAQ project leader have set out a proposal for detector readout during Run 3 and 4 [8]. The document sets out their proposal for HB trigger and CRU status message handling in more detail than presented here. However, the exact details of implementation will only be decided, in consultation with the electronics coordinator and DAQ project leader, once the LTU and CTP firmware development is underway.

6.6 CTP logic

The CTP internal logic is similar to that in RUN2. It keeps options for

- several trigger levels (e.g. CPV),
- different trigger input conditions,
- the clustering of detectors.

Therefore the concept of trigger class defined as a combination of trigger input condition and group of detectors to be read out is also kept at least in internal CTP logic. However, the expected number of classes is less than in RUN2, i.e. ~ 20. However, the extension of classes in the CTP is fully transparent for the rest of the system.

6.7 CTP readout

The information sent from CTP/LTU system to O2 is:

- copy of all triggers,
- TIM (64 bits) and DM (18 bits) for every bunch crossing,
- HB map with payload of
    - HB id – Orbit (32 bits) + BC id (12 bits)
    - 1 acknowledge bit and 2 buffer status bits per CRU

In the proposed CTP readout model, the CTP behaves with respect to O2 almost as a normal detector. The logic is shown in Figure 6.1.

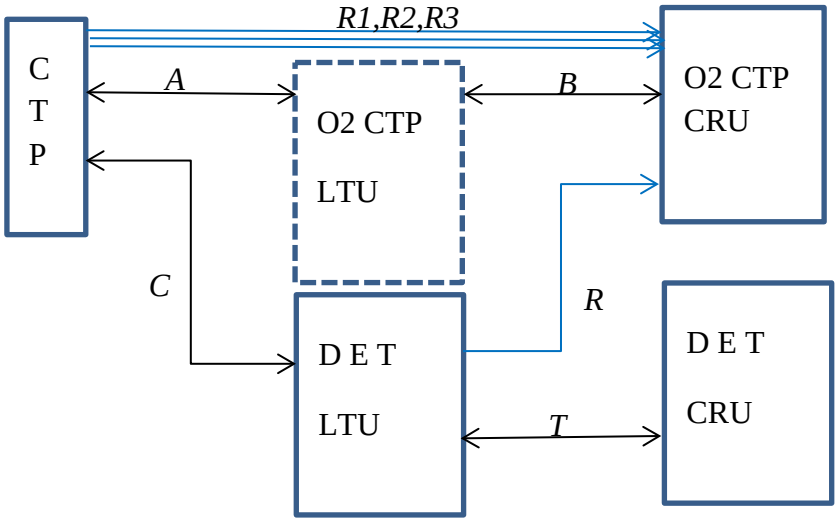


Figure 6.1 CTP readout

The CTP sends, at every bunch crossing, the data containing the TIM ,DM and HB mask via links *R1, R2, R3* to the O2 CTP CRU. Every detector LTU sends a copy of all triggers to the O2 CTP CRU over link *R*. The status of the CRU as seen by the LTU is also sent on the same link *R*. Other possible implementation is that the statuses of the CRUs are sent from LTU to CTP over link *C* where they are collected and sent to O2 over link *R3*. In this baseline solution the links *A,B,C* and *T* are PON and *R1,R2,R3* and *R* are GBT. The data format for PON links is Table 14.1 PON data format, data on links *R1,R2,R3* and *R* are in Table 14.4, Table 14.5 and Table 14.6 This readout model is the first proposal and it is expected to be discussed with O2/CRU for further optimisation..

In the following the upstream data rate is estimated and compared with PON bandwidth. The status of the CRUs is transmitted from CRU to O2 in three steps. First it goes from detector

CRU to detector LTU (link *F*), then from detector LTU to CTP (link *C*) and finally from CTP to O2 (links *A,E*) As discussed in section 6.5 each CRU sends HBid and CRU status bits corresponding to (44+48) bits per 100μs assuming 10kHz HB frequency resulting in about 1Mbitps data rate. The upstream PON bandwidth is 48 user bits per Optical Network Unit (ONU) per 125 ns (see [9]) corresponding for 64 ONU per splitter to 6Mbitps data rate giving us safety margin of six for upstream traffic on link *F*. In the next step LTU collects status of all detector CRUs and sends it to CTP via link *C*. Maximum number of CRUs per detector is 360 (TPC) and so maximum traffic on link *C* is 360x1Mbps=360Mbps below 384 Mbps available at PON. Finally the links *A,E* from CTP to O2 are upstream links with bandwidth higher than 1Gbps not creating bottleneck.

7. Hardware implementation

In this section a universal board, which can be used in both the LTU and CTP roles, is described. The board will be a 6U VME-type board and will use the existing CTP/LTU VME crate for power only. (It will not be possible to program or communicate with this board via VME.) The board may be reconfigured remotely via a USB-JTAG connector, where a USB module (Anywhere© USB) will be used which performs USB to Ethernet translations allowing the use of a remote computer.

The board will be provided with:

- a new XILINX series KINTEX Ultrascale (XCKU040-1FFVA1156C) FPGA with sufficient frequency range to implement PON and GBT thus keeping flexibility to use PON or GBT,
- 2 GB of DDR4 memory, partitioned so as to allow adequate storage of snapshot data, with reserved space for future applications,
- a universal FMC connector (connected to a simple mezzanine card for 96 LVDS inputs/outputs in the CTP case or to a mezzanine card with an additional eight optical connections in the LTU case),
- a 12 slot cage for optical input/output GBT or PON. These inputs/outputs will be populated in accordance with the board's given role (CTP/LTU) and detector (number of outputs),
- an optical SFP+ link to a O2 (or dedicated Trigger) PC using IP-BUS protocol for monitoring and control. An electronic Ethernet SFP+ module, instead of an optical module, will be used for IP-BUS communications when using the CTP/LTU in the lab.

The interface between the CTP and LTUs is standard PON (GBT being a backup solution).

Additional Input/Output:

1. A USB-JTAG connector for configuring the Kintex-Ultrascale FPGA. In the ALICE cavern, the JTAG will be connected to the Trigger PC located on the surface via a USB to Ethernet module (Anywhere© USB), which makes an interface between USB and Ethernet.

2. Six LEMO 00 b ECL connectors
3. 2 LEMO LVCMOS connectors for scope outputs
4. 5 LVDS LEMO

The Kintex-Ultrascale series also provides a facility for automatic recovery from single and double event upsets for configuration. It is self-correcting after a CRC check. Since the CTP/LTU will be placed in a site of only moderate radiation (total radiation dose being 4.8 rad [7]), this automatic recovery procedure is sufficient.

7.1 The Central Trigger Processor

The functions discussed in section 6 can be realised with a new CTP board combining the functions of the current CTP BUSY, L0, L1, L2 and FO boards. This obviates the need to transfer data across the backplane and therefore eliminates the CTP dead time. The universal board is used in the role of CTP board by

- adding a simple FMC mezzanine board for 96 LVDS input/output,
- using the optical links to distribute triggers to LTUs,
- using the optical links for CTP readout.

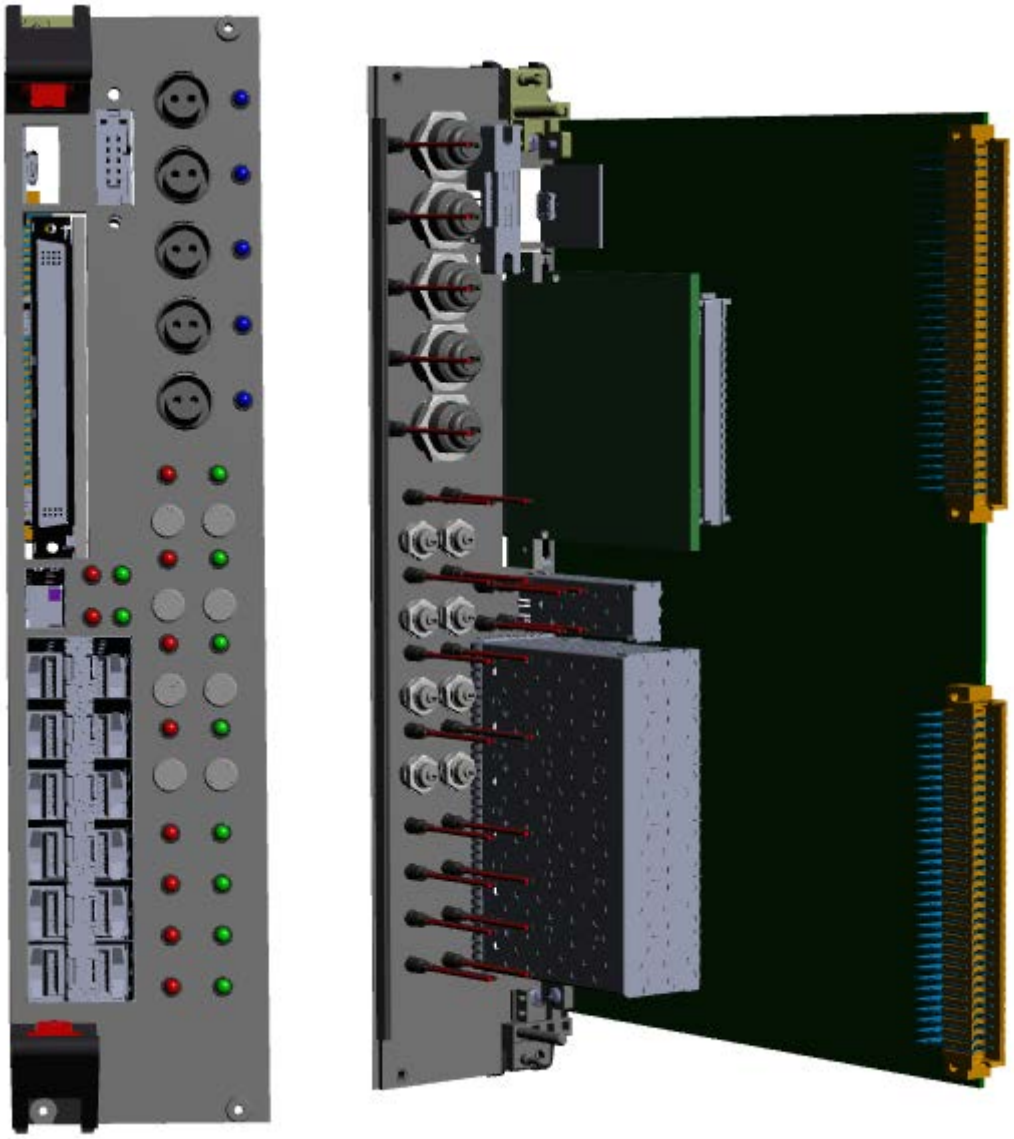


Figure 7.1 CTP board front panel connections and side view

7.1.1 LM0 board prototype

As mentioned in section 4.3, the existing CTP level-0 board has been replaced with a new board, the LM0 board, in order to incorporate the pre-trigger for the TRD into the trigger system and to provide additional features to the trigger system for Run 2. This LM0 board was designed with the Run 3 trigger upgrade in mind and serves as a CTP prototype, containing some of the features required for Run 3. Figure 7.2 shows a picture of the CTP prototype board.

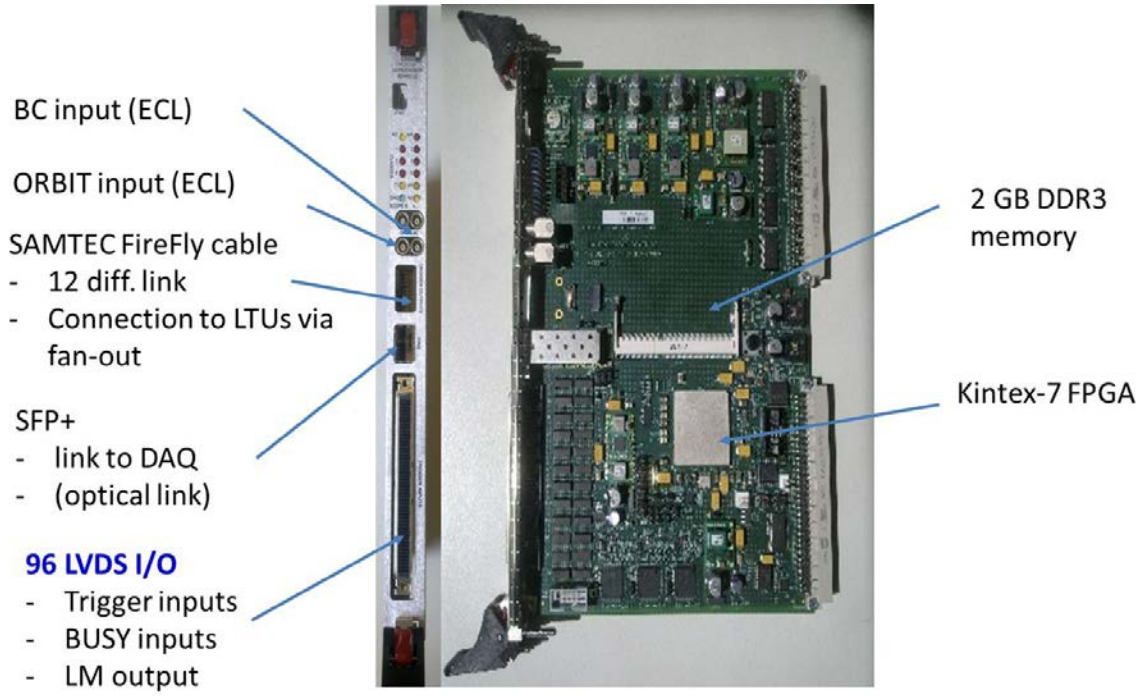


Figure 7.2 CTP prototype board

This CTP prototype board already has some of the functionality of the final CTP board and has performed well in the ALICE cavern using the 2015 data-taking period.

7.1.2 CTP Input and Output Connectors

All inputs/outputs to/from the CTP will be performed via the front panel. The I/O connections are as follows (see also Figure 7.1):

1. A USB-JTAG connector for configuring the Kintex-Ultrascale FPGA. In the ALICE cavern, the JTAG will be connected to the Trigger PC located on surface via a USB to Ethernet module (Anywhere© USB) which makes an interface between USB and Ethernet.
2. Six LEMO 00 b ECL connectors
    a. One for the LHC bunch-crossing (BC) signal
    b. One for the LHC Orbit signal
3. Two LEMO LVCMOS outputs for an oscilloscope
4. 12 optical connections.
5. A SFP+ optical connector for the control and monitoring interface to the O2 (or dedicated Trigger PC).
    a. Note the optical connector unplugs and can be replaced by an electrical Ethernet SFP+ connector for control and monitoring in the lab.
6. 96 LVDS I/O (200 pin Molex) connector on the mezzanine FMC board for trigger inputs, BUSY inputs (via LTUs), and a special fast LM trigger output for the TRD detector.
    a. Note the current number of trigger inputs is expected to be 31 (see **Table 8.1**), the number of BUSY inputs is 6 (one per detector using current TTC

system), and one output is reserved for the fast LM (pre-trigger) signal to the TRD. This leaves a total of 59 spare I/Os.

b. An adaptor cable, known as the spider, has a 200 pin Molex connector on one end and LVDS LEMO connectors on the other end so that the connectors for trigger and BUSY inputs will remain the same as for Runs 1 and 2.

7.1.3 Trigger Inputs and Synchronization

Trigger inputs should have the same negative logic of LVDS signals as the current CTP. The format of the trigger outputs and data will be discussed in the Data Format section.

The CTP will accept and process LM, L0, and L1 trigger inputs.

All trigger inputs will be generated with the *time precision of a single bunch crossing*. In exceptional cases, trigger inputs with somewhat lower time precision might also be acceptable. These signals will remain asserted during the full length of their uncertainty interval.

The trigger inputs will be synchronous with the detector **BC** clock and have the maximum edge jitter of ±1 ns.

The CTP will *synchronize* all the trigger inputs with the local **BC** clock, and *align* them in time so that the data presented to the processor logic correspond to a common bunch crossing.

The *alignment* assures that the trigger signals originating from the same bunch crossing reach the processor logic in the same clock cycle; it is achieved by delaying signals by an appropriate number of *full clock periods*. The *synchronization* adjusts the phase of the trigger inputs in respect to the **BC** clock (and, indirectly, to the LHC bunch crossing time); each CTP input will have possibility to strobe trigger input with positive or negative edge of the clock.

The *synchronization* will be automatic; during the process, the trigger detectors will be required to continuously transmit a pattern of "triggers" in alternating bunch-crossing intervals (as was the protocol in Runs 1 and 2)**.**

In order to be *aligned*, the trigger signals must reach the CTP inputs within a *window of 16 **BC** intervals (400ns) preceding the corresponding trigger decision time*; the alignment within the window will be carried out by the CTP logic.

7.1.4 Monitoring and Snapshot Memory

As with the current CTP, many internal counters, including trigger inputs and detector BUSY signals, will be monitored continually and this information will be read out via the optical SFP+ link to the O2 (or Trigger) PC. The new CTP will also incorporate a snapshot memory, since this has proved to be useful in Runs 1 and 2. The 2GB of DDR4 memory on the CTP board will enable the new CTP to take snapshots for $5x10^8$ bunch crossings.

7.2 CTP-LTU Interface

The nine optical outputs from the CTP have to be shared between eighteen detectors, two detectors per optical link. This default topology may be optimized by grouping detectors with identical data flow.

7.2.1 PON Interface

Downstream data:

80 bits per detector/BC: ~~EventID (44 bits), TType (16 bits), Detector Mask (18 bits), Level (2 bits)~~

New: EventID (44 bits), TType (32 bits) Detector Mask (2 bits), Level (2 bits)

Upstream:

The PON bandwidth available for user is 384Mbit/sec (48 bits per ONU per 125 ns) allowing to transfer 384* 88/432=72 bits per HB per CRU. GBT Interface (backup solution)

7.2.2 GBT Interface

Downstream:

40 bits per detectors/BC: Reduced EventID (22), TType, (16 bits), Level (2 bits)

Upstream:

Not possible with passive splitting. An extra BUSY board derived from the universal trigger board is necessary for CRU status collection. Alternatively the CRU status can be evaluated at LTU and simple decision sent to CTP via electrical BUSY connection.

7.3 Local Trigger Unit (LTU)

The Local Trigger Unit (LTU) serves as an interface between the ALICE Central Trigger Processor (CTP) and the detector readout electronics. The existence of a uniform interface throughout the experiment greatly simplifies configuration and run-control tasks and makes system modifications easier to develop and implement. The LTU is a 6U VME-type board, taking only power from the VME crate, connected to the CTP via the CTP-LTU optical PON fan-out, and has two modes of running, *global* and *stand-alone*.

In a *global run*, the LTU serves as a “transparent” link between the CTP and the detector readout electronics; the board performs the necessary conversions of signal levels and provides some on-line monitoring options.

In the *stand-alone mode* of operation, the LTU *fully emulates the CTP protocol* and enables detectors to carry out development, test and calibration tasks independently of the CTP, at remote sites, or at times when the CTP is either not available or not required. The LTU will generate programmable *trigger sequences.* The sequences could be “linked” to form a *burst*. A *sequence*, or a *burst* can be executed either as a *single-shot,* or as a *continuous* loop. The timing is controlled by the software; by an internal random signal generator, with a

programmable average rate; by a pre-scaled **BC** clock, with a programmable pre-scale factor; or by an external local pulser. Mode selection is carried out by the software.

Like the CTP board, the LTU board will use the XILINX series KINTEX Ultrascale FPGA, and be provided with 2 GB of DDR4 memory. In order to allow for the many connectors required, the LTU will have a triple front panel as shown in Figure 7.3. The hardware implementation will be similar to CTP board leaving the FMC connector empty for most of the detectors, or adding an FMC board with extra optical outputs if necessary.

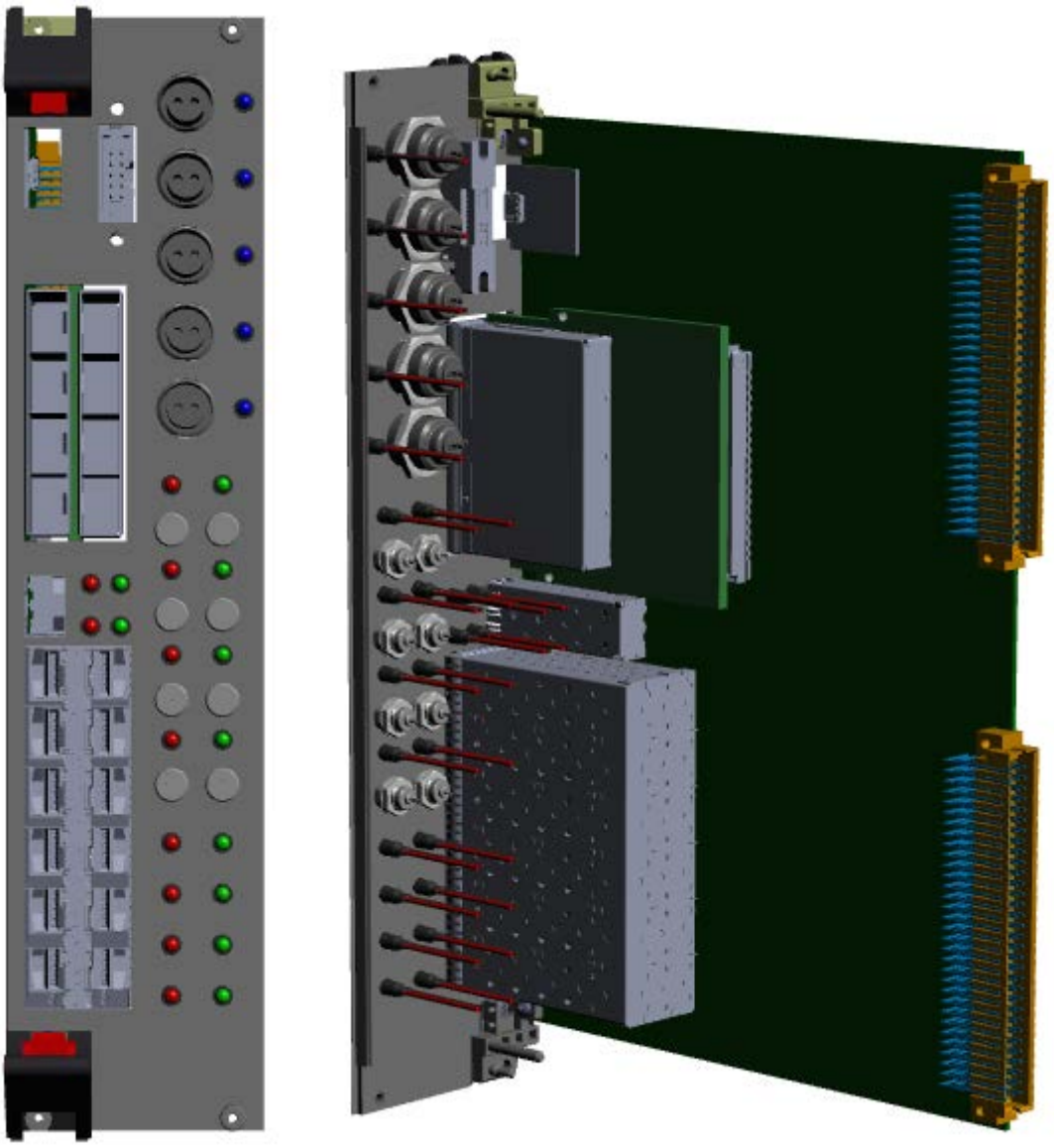


Figure 7.3 LTU front panel connections and side view

7.3.1 LTU Input and Output Connectors

All inputs/outputs to/from the LTU will be via the front panel. The I/O connections are as follows:

1. A USB-JTAG connector for configuring the Kintex-Ultrascale FPGA. In the ALICE cavern, the JTAG will be connected to the Trigger PC via a USB module which makes an interface between USB and Ethernet.
2. Five LVDS LEMO connectors
    a. Two for LM and L0 outputs (for detectors requiring LM or L0 triggers via LVDS copper cable, e.g. CPV, HMPID,ZDC).
    b. One for BUSY in signal from the detector (note only 1 BUSY in per detector)
    c. One for BUSY out (to be sent to CTP board)
    d. One for FAST LM trigger input, direct from CTP (ITS,TRD,CPV,HMPID,ZDC)
3. A PM Bus connector for voltage and temperature monitoring
4. Eight LEMO 00 b ECL connectors
    a. One for the LHC bunch-crossing (BC) signal
    b. One for the LHC Orbit signal
    c. Two outputs for an oscilloscope
    d. TTC channel A and B outputs to TTCex board (for detectors using the existing TTC system)
    e. Pulser input (for pulser trigger input in *stand-alone mode*)
    f. Spare i/o
5. A SFP+ optical connector for the control and monitoring interface to the O2 (or dedicated Trigger PC) using IP Bus.
    c. Note the optical connector unplugs and can be replaced by an electrical Ethernet SFP+ connector for control and monitoring in the lab.
7. Ten SFP+ optical links available for trigger outputs and data to be sent directly to detectors, CRUs, or detector optical fan-out units (plus an additional two for CTP use). The skew of the trigger signals will be less than 1 ns with the jitter less than 20ps.

7.3.2 LTU Trigger and Clock Outputs

Each LTU board will transmit the LHC clock and Orbit signal continuously to the detectors (or CRUs) via the optical SFP+ connectors. Other data (e.g. bunch crossing number etc.) will only be transmitted when a trigger is issued.

Each LTU will transmit only one trigger signal (LM, L0 or L1). The trigger signal latency to be transmitted will be programmable and depend on the particular detector's requirements.

The LTUs will be compatible with detectors using the current TTC system, GBT and 10GB PON.

7.3.3 LTU Control and Monitoring

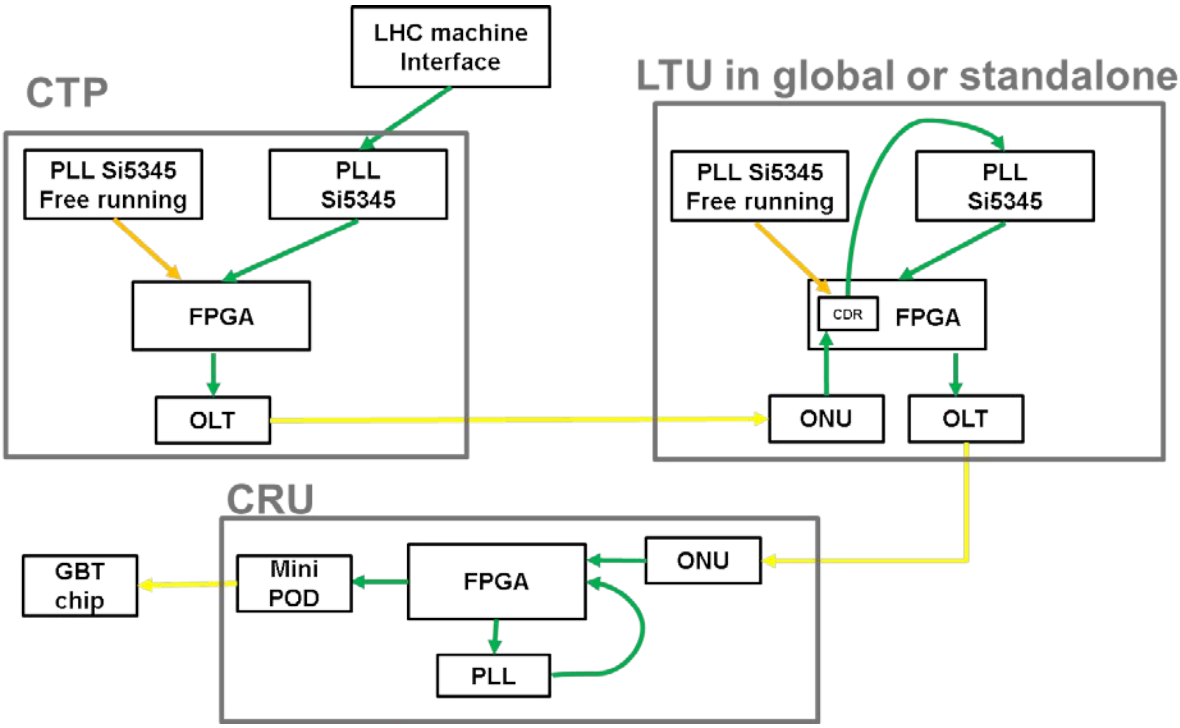
As with the current LTUs, many internal counters, including trigger inputs and detector BUSY signals, will be monitored continually and read out via the optical SFP+ link to the O2 (or Trigger) PC. The new LTUs will also incorporate a snapshot memory, since this has proved to be useful in Runs 1 and 2. The 2GB of DDR4 memory on the LTU boards will enable the new trigger system to take snapshots 10^9 bunch crossings long.

7.4 Clock

In this section clock scheme is described in case of system at P2 and in the lab.

7.4.1 Si5345 Clock priorities

1. Clock from CTP (via GBT or PON).If clock from CTP not present then
2. clock from TTCmi. If clock from TTCmi not present then
3. standalone clock from local oscillator.



7.4.2 System start-up at Point 2

1. Initial state:

- CTP: LHC clock present from LHCmi crate
  - LTU: ONU uses free running 240 MHz clock, FPGA works with 40.078MHz back-up clock from Si5345, OLT in reset state, ONU upstream in reset state
  - CRU: ONU on CRU uses 240MHz free running clock

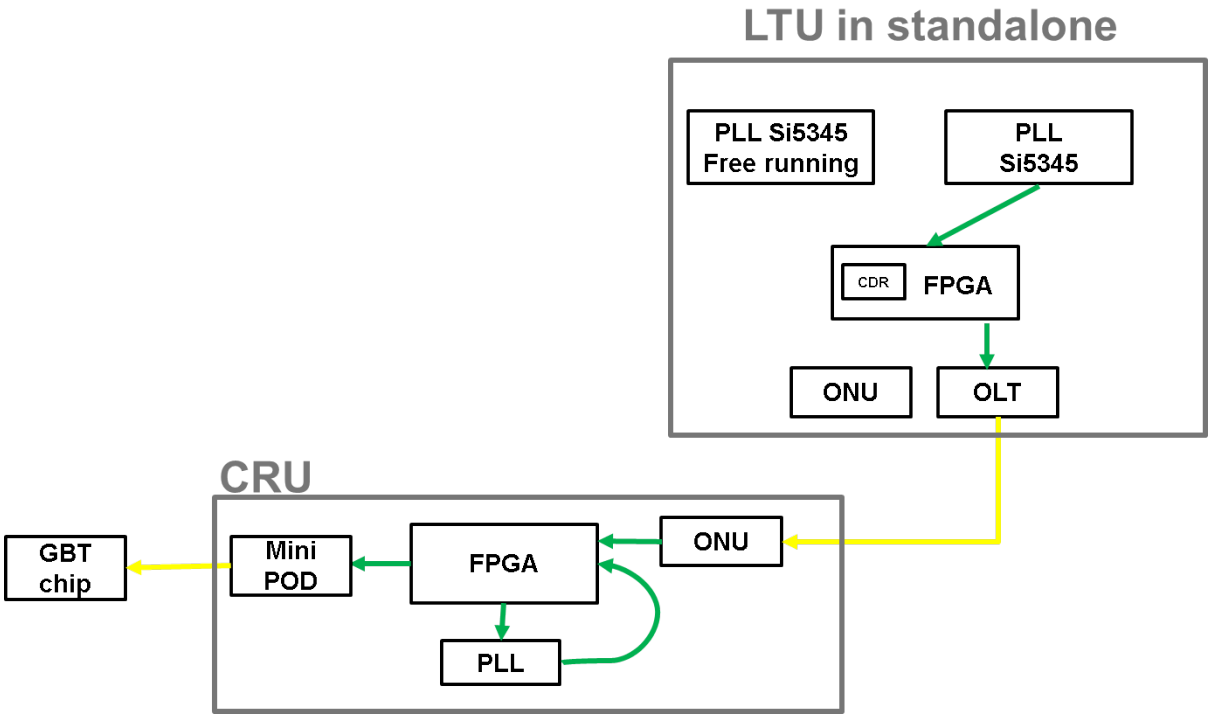
2. LTU locks to LHC clock

- CDR inside LTU FPGA delivers 40.078 MHz clock to jitter cleaner PLL
- PLL switch from back-up clock to LHC clock, some glitches on clock are present
- Reset FPGA (glitches on clock could cause problems)

- Enable OLT

3. CRU locks to LHC clock

- CRU FPGA delivers 40 MHz clock to the jitter cleaner PLL
- CRU switch to LHC clock



7.4.3 System start-up at Lab

1. Initial state:

- LTU: PLL generate free-running 40.078 MHz clock (back-up clock)
- OLT always enabled

2. CRU locks to LHC clock

- CRU FPGA delivers 40 MHz clock to the jitter cleaner PLL
- CRU switch to LHC clock

8. Estimated Trigger Latencies

The latest times for LM, L0, and L1 trigger inputs to reach the CTP are 425ns, 1200ns, and 6100ns respectively. The estimated trigger input latencies for the 31 known trigger inputs are summarised in Table 8.1.

In all cases, the trigger system (CTP input to LTU output) is expected to have a latency of about 210ns broken down as follows:

- CTP processing time – 100ns,
- CTP-LTU PON fan-out – 85 ns,
- LTU – 25ns

The total latency for the trigger to reach the detector will depend on a number of factors, including the length of the optical cable, whether the detector uses GBT or PON, and if the signal is sent directly to the FE or via the CRUs. However, the estimated latencies for trigger distribution via GBT (e.g. the ITS), CRUs, and TTC are given in Tables 8.2, 8.3 and 8.4 respectively.

The skew of the trigger signals will be less than 1 ns with the jitter less than 20ps.

Table 8.1 Trigger Input Latencies

Detector	#CTP inputs	Time-of Flight [ns]	Processing [ns]	Cabling [ns]	Cable To CTP	Total [ns]
FIT	5	12	192	175	46	425
ACO single/mult	2	110	75/125	160	240	585/635
EMC L0	2	15	732	0	96	843
EMC L1	8					6100
PHS L0	4	15	732	0	96	843
PHS L1	3					6100
TOF	4	12	800	0	50	862
ZDC ZNA L0	1	375	92	694	5	1166
ZDC ZNC L0	1	375	92	549	5	1021
ZDC L1	4	375	268	966	500	2110

Table 8.2 Estimated Latencies for trigger distribution via GBT e.g. for ITS

Time (ns)	Total Latency (ns)			Description
	L1	L0	LM	
6100 / 1200 / 425	6100	1200	425	L1 / L0 / LM inputs to CTP board
100	6200	1300	525	CTP processing time
125	6325	1425	650	CTP-LTU fan-out time
25	6340	1450	675	LTU processing time
175	6525	1625	850	Transmission via 35 metres of optical cable
150	6675	1775	1000	GBT downstream latency (decoding time)
250	6925	2025	1250	Distribution of triggers from ITS readout module to detector
TOTAL: 6925 / 2025 / 1250				**Total latency from interaction to detector for L1 / L0 / LM trigger**

Table 8.3 Estimated Latencies for trigger distribution to FEE via CRU

Time (ns)	Total Latency (ns)			Description
	L1	L0	LM	
6100 /1200 / 425	6100	1200	425	L1/ L0 / LM inputs to CTP board
100	6200	1300	525	CTP processing time
125	6325	1405	650	CTP-LTU fan-out time
25	6350	1450	655	LTU processing time
600	6950	2050	1275	120 metres of optical cable to CRU (ALI-CR4)
125	7075	2175	1400	PON downstream latency (only active components)
25	7100	2200	1425	CRU latency
130	7230	2330	1555	GBT downstream latency (using Aria 10 FPGA)
600	7830	22930	2155	120 metres of optical cable CRU to detector FEE
TOTAL: 7830 / 2930 / 2155				**Total latency from interaction to detector FEE for L1 /L0 / LM triggers**

Table 8.4 Estimated Latencies for trigger distribution via TTC

Time (ns)	Total Latency (ns)			Description
	L1	L0	LM	
6100 / 1200 / 425	6100	1200	425	L1 / L0 / LM inputs to CTP board
100	6200	1300	525	CTP processing time
125	6325	1425	650	CTP-LTU fan-out time
25	6350	1450	675	LTU processing time
70	6420	1520	745	TTC latency for L1A signal (TTCex + TTCrx)
140	6560	1669	885	optical cable (28 m long) from CTP to the readout electronics
TOTAL: 6560 / 1660 / 885				**Total latency from interaction to detector for L1 / L0 / LM trigger**

9. Software for Control and Monitoring

Monitoring and control of the CTP and LTU boards will be via the IP Bus. A LTU GUI will be written using the IPbus library allowing its interactive control in standalone mode. The LTU GUI will be written for the Linux operating system in C++ and python.

The main functionality provided by the CTP software will be:

- the CTP configuration and control,
- CTP monitoring.

The main functionality provided by the LTU GUI will be:

- the LTU configuration and control,
- CTP emulator programming and control (setting the trigger types and rate),
- BUSY monitoring and trigger signal counting.

10. Detectors

In this section the detectors are divided into groups according to their readout and trigger distribution. The three basic groups are summarised in Figure 5.1: detectors with triggers distributed via CRUs, detectors with triggers distributed via GBT and detectors with triggers distributed via TTC.

10.1 Detectors with triggers via CRU (group A)

All detectors in this group receive HB triggers and triggers distributed from the CTP via their LTU to CRUs. The trigger contains the Event ID and Trigger Type, see 6.2. It is transmitted synchronously over PON. By default all these detectors send the status of their CRUs (see table 7 in [8]) upstream to their LTU via PON.

10.1.1 TPC, MCH, MID, FIT, ZDC

These detectors can run in both continuous and triggered modes.

10.1.2 ACO

ACO is updated having multievent buffer of about 10 events. As such it can run in triggered mode with proper protection. It can run also in continuous mode triggered by itself.

10.1.3 TOF

TOF transfers FE buffers to the TOF Data Readout Module (DRM) on arrival of a special trigger. A special trigger is a regular BC downscaled trigger with a frequency between 5.6 kHz and 250 kHz. This trigger is to be transmitted from the CTP/LTU to the CRU as a normal trigger via PON and subsequently retransmitted from the CRU to the FE via GBT. The status of CRUs is transmitted from the CRUs to its LTU over PON as expected by a detector with a CRU. TOF can operate in both continuous and triggered modes.

10.2 Detectors with triggers via GBT (ITS and MFT, group B)

Detectors in this group receive HB triggers or triggers distributed from the CTP via their LTU to their FE. The trigger is identical with the trigger message and contains Event ID and Trigger type, see 6.2. It is transmitted synchronously over GBT. By default all these detectors send the status of their CRUs (FULL/NOTFULL) upstream to their LTU via PON.

10.3 Detectors with triggers via TTC (group C)

These detectors follow the RUN2 protocol with two level trigger:

- LM trigger over cable or as code 10 in TTC A channel,
- L0 trigger as code 11 in TTC A channel (optional),
- Asynchronous trigger message over TTC B channel (EventID and Trigger Type),
- BUSY from FE to LTU over LVDS.

10.3.1 CPV, EMC, HMP, PHS

These detectors have no additional features with respect to default protocol above.

10.4 TRD

The trigger distribution for the TRD is special. LM triggers are sent from LTU to FE over the TTC system. In parallel they are also transmitted from LTU to CRU via PON. The trigger protocol is one level trigger at LM latency realised by a pulse in TTC A channel. The TRD requires also special calibration triggers every 1000 LM physics triggers (programmable). For the calibration trigger the LM pulse in A channel is followed by another single pulse with fixed programmable latency with respect to the LM pulse. No information is required in TTC B channel in either case. The calibration triggers have both physics and calibration type of trigger bits active in PON trigger message.

After each trigger the TRD is protected by CTP for programmable time interval of order of couple microseconds until TRD BUSY arrives. TRD needs to communicate its BUSY status to CTP in few microseconds in order to optimise the data taking efficiency .To achieve this the BUSY should be fan-in from all CRUs in control room (e.g. using additional CRU) and transmitted to CTP/LTU electrically or optically. In addition the CRUs transmit standard HBT acknowledge message to CTP.

10.5 LTU detector connections

The Table 10.1 summarises the use of detector LTU's optical links. The 1st column is detector name and the 2nd column is number of CRUs detector uses. The 3rd column is number of FE links to be triggered, applicable only to ITS and MFT. The 4th column is number of GBT links on LTU, default is one used for CTP readout. ITS and MFT needs special GBT links to deliver trigger at their FE, in this case passive GBT splitting is foreseen. The 5th column is number of ONU links at LTU used for receiveing data from CTP. The 6th column is number of OLT links used from transmitting data from LTU to CRU. In the last column there is splitting ratio used for PON /GBT (passive splitting in both cases).

Table 10.1 LTU detector connections.

Detector	# CRU	FE links	#GBT links	#ONU links	#OLT links	Splitting PON/GBT
TPC	360	-	1	1	6(12)	1:64(1:32)
MCH	25	-	1	1	1	1:32
MID	2	-	1	1	1	2
FIT	1	-	1	1	1	-
ACO	1	-	1	1	1	TBC
TOF	3	-	1	1	1	3
ITS	8	192	1+12	1	1	1:8/1:16
MFT	4	80	1+5	1	1	1:4/1:32
TRD	36	-	1	1	2	1:32

ZDC	1	-	1	1	1	-
TOTAL	441	272	27	10	16	-

`

11. Responsibilities of Trigger Group and Detector Groups

The division between the responsibilities of the Trigger Upgrade Project and the detectors and other systems will be the same as in RUN1 and RUN2.

The responsibilities of the trigger upgrade project are as follows:

- To provide and maintain the CTP boards
  - One for the cavern, one for the CTP/DAQ lab, one for CTP system development, one or two spare (4/5 CTP boards in total)
- To provide and maintain the LTU boards
  - 14 for the detectors, 1 for the DAQ readout, 1 for the CTP/DAQ lab, 1 for CTP system development, 3 spare (20 boards in total)
- To provide and maintain the CTP-LTU PON Fan-out
  - One for the cavern, 2 spare (3 in total)
- To provide and connect cables between the CTP and LTUs.

It is the responsibility of the detectors, sub-systems, or electronics coordination to provide all the necessary cables to the CTP and from the LTUs as well as to supply all necessary fan-in and fan-out units. These responsibilities are summarised below.

- It is the responsibility of detectors, delivering trigger inputs, to provide LVDS inputs, with LEMO connectors, at the CTP crate in the cavern.

- It is the responsibility of all detectors to connect their optical cable to the corresponding LTU in the ALICE cavern.

- Optical fan-out units, if required, are the responsibility of the detector (there will be ten available optical outputs on each LTU board).

- It is the responsibility of all detectors to deliver their LVDS Busy signals, with LEMO connectors, directly to the LTUs (**1 Busy input only**) or via their CRUs. In the case of detectors using CRU the busy can be transmitted via GBT and PON.

12. CTP and LTU Milestones

The milestones for the trigger project, assuming a second prototype is not required, are summarised in Table 12.1 below with the key milestones written in bold type. Table 12.2 shows the effect of the milestones if a second prototype is required.

Table 12.1 Summary of trigger milestones

Date	**LTU Milestone**	**Comments**
Sept 2015	LTU pre-prototype delivered to test concepts and enable FW & SW development.	Delivered end of March 2015
Dec 2015	LTU specifications finished	Finished subject to Design Review
Jan 2016	CTP and LTU Design Review	Finished but modified design required.
March 2016	CTP revised specifications completed	Finished subject to 2nd Design Review
May 2016	**Second CTP design Review**	
July 2016	Schematic capture of Trigger board	
July 2016	CTP electronics design review (EDR)	
Sept 2016	PCB layout complete (RAL)	Subject to RAL TD availability and EDR
Nov 2016	Board prototypes complete	
Jan 2017	I/O interface FW for LTU ready	For testing LTU I/Os
Feb 2017	LTU I/O interface tests complete	
March 2017	CTP emulator for LTU ready	For testing CTP-LTU chain
March 2017	LTU slice test	
April 2017	Testing of prototype boards complete	
April 2017	**Trigger board production readiness review**	
June 2017	Trigger boards production completed	
Sept 2017	Trigger boards fully tested	
Dec 2017	LTU firmware complete	
Dec 2018	CTP firmware complete	
April 2019	**Integration tests of trigger system with DAQ (in CERN lab) completed**	
June 2019	Installation and testing of trigger system in ALICE cavern completed	
June 2019	Commissioning of trigger system with all ALICE sub-detectors and systems starts	

Table 12.2 Summary of trigger milestones assuming second prototype board

Date	LTU Milestone	Comments
Sept 2015	LTU pre-prototype delivered to test concepts and enable FW & SW development.	Delivered end of March 2015
Dec 2015	LTU specifications finished	Finished subject to Design Review
Jan 2016	CTP and LTU Design Review	Finished but modified design required.
March 2016	CTP revised specifications completed	Finished subject to 2nd Design Review
May 2016	**Second CTP design Review**	
July 2016	Schematic capture of Trigger board	
July 2016	CTP electronics design review (EDR)	
Sept 2016	PCB layout complete (RAL)	Subject to RAL TD availability and EDR
Nov 2016	Board prototypes complete	
Jan 2017	I/O interface FW for LTU ready	For testing LTU I/Os
Feb 2017	LTU I/O interface tests complete	
March 2017	CTP emulator for LTU ready	For testing CTP-LTU chain
March 2017	Testing of 1st prototype boards complete	
April 2017	**Board modifications complete**	Assuming second prototype required
April 2017	**New PCB layout complete**	Assuming second prototype required
June 2017	**Production of modified prototype**	Assuming second prototype required
July 2017	**Testing of modified prototype**	Assuming second prototype required
Aug 2017	LTU slice test	
Aug 2017	Testing of 2nd prototype boards complete	
Aug 2017	**Trigger board production readiness**	

	review	
Oct 2017	Trigger boards production completed	
Jan 2017	Trigger boards fully tested	
Feb 2018	LTU firmware complete	NB Hw delayed by 4 months but FW only delayed by 2 months.
Feb 2019	CTP firmware complete	
June 2019	**Integration tests of trigger system with DAQ (in CERN lab) completed**	
Aug 2019	Installation and testing of trigger system in ALICE cavern completed	
Aug 2019	Commissioning of trigger system with all ALICE sub-detectors and systems starts	

12.1 Trigger Project Gantt Chart

The Gantt Chart of the trigger project is shown in figure 13.1 below. The critical path is shown in red and is governed by firmware development. Figure 13.2 shows how the Gantt chart is modified in the case a second prototype is required. In this case, although the final production of the trigger board would be delayed by four months, the project as a whole would be delayed by two months.

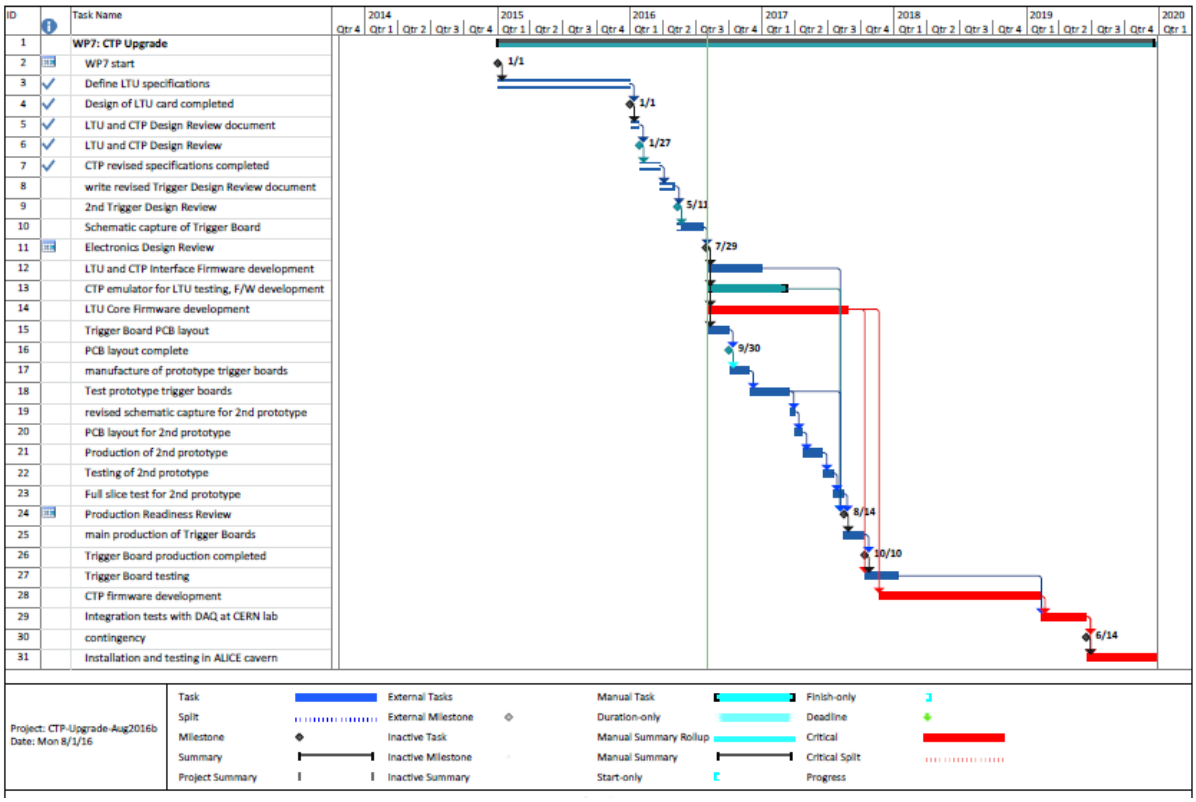


Figure 12.1 *Gantt chart of the trigger project*

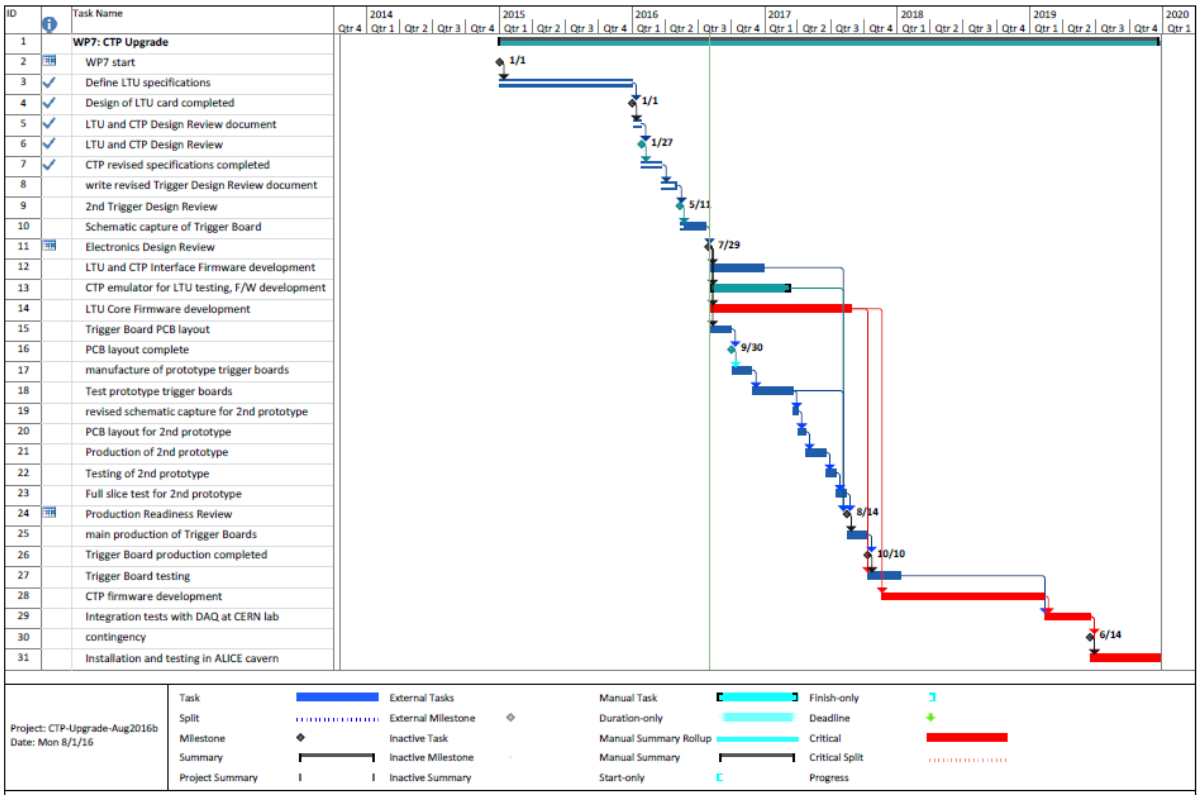


Figure 12.2 *Gantt chart assumming a second prototype is required*

13. ALICE Trigger System – At a Glance

13.1 The Central Trigger Processor (CTP)

- The ALICE trigger system, situated in the experimental cavern, will consist of a Central Trigger Processor (CTP) and detector interfaces, known as Local Trigger Units (LTUs).

- ALICE detectors consist of 2 groups:

    - Upgraded detectors with continuous readout. They should cope with triggers at any time, even in the case of detector busy.

    - Detectors with old readout which propagate the BUSY signal to the CTP in the same way as in run2. The CTP stops sending triggers if detector busy.

- The ALICE CTP will generate *hardware triggers at three different latencies* – **LM**, **L0** and **L1,** to all detectors with continuous readout and to detectors with old readout

which are not *busy*, and will have the ability to partition the detectors into up to 14 *detector clusters* i.e. the same number as the number of detectors.

- The CTP will also be able to deliver software, calibration, and Heartbeat (HB) triggers.
- The CTP will send **all** detectors HB triggers every LHC Orbit whether they are Busy or not and in whatever mode they are running.
- The CTP will operate with no Dead-Time.
- The ALICE CTP receives and generates the following signals:
    - 2 LHC timing signals (**BC** and **Orbit**) via ECL inputs,
    - Trigger inputs and detector BUSY signals (up to 88 LVDS inputs and 8 outputs in total.) The LVDS outputs will be reserved for a fast LM trigger, for the TRD, CPV and HMPID via its LTU (see section on LTU).
    - For detectors with continuous readout BUSY signals (HB acknowledge messages) are sent over PON/GBT and for old readout detectors via LVDS.
    - A SFP+ optical link (using IP Bus) to the O2 for control and monitoring or a SFP+ Ethernet link when used in the lab,
    - PON protocol to send trigger outputs and trigger data to the LTUs via PON splitters. GBT protocol with passive optical splitting is the backup solution.
- The CTP will generate and transmit the following data to detector for each trigger
    - Trigger Type (16 bits),
    - Event ID (ORBIT 32 bits+ BCID 12 bits = 44 bits),
- In addition, the CTP will generate and transmit following data to O2 for each trigger
    - Trigger Input Mask (74 bits),
    - Detector Mask (18 bits).
- The CTP may receive the status of CRUs (HB acknowledge) from LTUs and transmit it regularly (once per Heartbeat) to O2. In the baseline proposal presented in this document the HB acknowledge is sent to O2 directly from the LTUs.
- The CTP shall consist of a single 6U VME board.
    - The CTP board shall use the VME crate for power only and will be controlled via the optical link to the DAQ computer when in the ALICE cavern (Ethernet link when used in the DAQ/CTP lab).

13.2 The Local Trigger Units (LTU)

- There will be one Local Trigger Unit (LTU) for each detector, plus spares. An LTU may be configured to deal with either GBT or PON signals, or indeed both.

- The LTUs will be able to operate in two modes, global mode, as an interface between the CTP and detectors, and standalone mode for detector development and testing.

    - In standalone mode, the LTU will have a programmable CTP emulator which can send CTP sequences with an adjustable, pseudorandom or fixed frequency. There will also be an ECL "Lemo" 00 input for an external pulser.

- Each LTU will receive and generate the following signals:

    - 2 LHC timing signals (**BC** and **Orbit**) via "Lemo" 00 ECL inputs needed for standalone LTU operation in lab

    - TTC Channel-A and Channel-B Lemo 00 ECL outputs for detectors using the current TTC system (i.e. not upgrading their frontends, see Table 5.2)

        - These outputs will connect to a TTCex board which has 10 TTC optical links for sending triggers and trigger data to the non-upgraded detector FEs.

    - Four further "Lemo" 00 ECL connectors for connection to oscilloscope (Scope-A and Scope-B), pulser input, and one spare i/o.

    - Five LVDS LEMO connectors (1 for LM out, 1 for L0 out, 1 for BUSY in, 1 for BUSY out, and 1 for fast LM input from CTP).

    - Ten available SFP+ optical links (GBT and/or PON protocol)

        - for distributing trigger signals and data to the detectors (either directly on detector, via detector specific readout systems or via the Common Readout Units (CRUs)). The skew of the trigger signals will be less than 1 ns and jitter less then 20 ps.

        - for receiving HB acknowledge from CRUs

        - for transmitting a copy of triggers and CRU status to O2

    - An additional SFP+ optical link (using IP Bus protocol) to the DAQ for control and monitoring.

    - A Power Management bus connector for voltage and temperature monitoring, and

    - A USB-JTAG connector for programming FPGA and SPI memory

- Each LTU shall consist of a single 6U VME board.
    - The LTU boards shall use the VME crate for power only and will be controlled via the optical link to the DAQ computer. The optical link can be replaced with an Ethernet link (electrical RJ45 SFP module) for controlled and monitored in the lab, during development and testing

13.3 Trigger Latencies and Timings

- The current requirements for the ALICE trigger upgrade are to deliver the triggers with three different latencies (time from particle interaction to trigger at front end electronics). The actual latencies will depend on transmission protocol used by the detector (PON, GBT, or TTC) and the length of optical cable required (see section 8). The required allowed latencies for trigger inputs to reach the CTP are (for details see Table 8.1):
    - Level Minus: LM $\rightarrow$ 425 ns
    - Level Zero: L0 $\rightarrow$ 1.2 μs
    - Level One: L1 $\rightarrow$ 6.1 μs

  It is estimated that the total latency for the LM to reach the ITS detector will be about 1.210 μs. The latency for the L1 / L0 trigger to reach the CRUs is expected to be about 6.885 μs / 1.985 μs.

- Current estimates suggest the total latency of the trigger system (CTP + CTP-LTU PON fan-out + LTU i.e. time between last trigger input to CTP and output of LTU) will be approximately 210 ns.

13.4 Detector Responsibilities

These are the same as in RUN1 and RUN2 and are summarised below.

- It is the responsibility of detectors, delivering trigger inputs, to provide LVDS inputs, with LEMO connectors, at the CTP crate in the cavern.

- It is the responsibility of all detectors to connect their optical cable to their LTU in the ALICE cavern.

- Optical fan-out units, if required, are the responsibility of the detector (there will be nine optical outputs on each LTU board).

- It is the responsibility of all detectors to deliver their LVDS Busy signals, with LEMO connectors, directly to their LTUs (1 Busy input only) or via their CRUs.

14. Appendix: Data formats

14.1 PON

The TTC 10G-PON protocol sends 24 8-bit words per clock cycle (bunch crossing) of which the first 4 words are for PON internal use, leaving 20 user words or 160 bits available per bunch crossing. The data format will be as follows.

Table 14.1 PON data format

Data	PON Byte	Payload	Content
[0..7]	1	[0..7]	TType
[0..7]	2	[8..15]	TType
[0..7]	3	[16..23]	TType
[0..7]	4	[24..31]	TType
[0..7]	5	[0..7]	BCID
[0..3]	6	[8..11]	BCID
[0..7]	7	[0..7]	Orbit
[0..7]	8	[8..15]	Orbit
[0..7]	9	[16..23]	Orbit
[0..7]	10	[24..31]	Orbit

14.2 GBT

The specified bit allocation is valid for the GBT links directly connected from LTU to FE (ITS and MFT) as well as for back-up GBT case for LTU to CRU connection. The data format will be as follows.

Table 14.2 GBT data format

Data	GBT word	Payload	Content
[0..15]	G0	[0..15]	TType
[0..15]	G1	[16..31]	TType
[0..11]	G2	[0..11]	BCID
[0..15]	G3	[0..15]	Orbit
[0..15]	G4	[16..31]	Obit

14.3 TTC

For the TTC protocol, the method of sending the trigger and data will be similar to what was employed in Runs 1 and 2. Namely, the trigger signal will be sent over Channel A as a synchronous signal and the data will be sent over Channel B as an asynchronous message. For the data, we have two choices, namely as a short message (188 bits/trigger at 100 kHz) or a long message (148 bits/trigger at 100 kHz). We choose a long message as in Run1 and Run2 allowing address commands to TTCrx chip. In either case, there is enough bandwidth

to send all of the trigger data with a trigger rate of up to 100 kHz corresponding to 10 Mbits/s. The data format will be as follows:

Table 14.3 TTC data format

Data	Word	Payload	Content
[0..15]	1	TType[0..15]	Trigger Type
[0..11]	2	BCID[0..11]	BCID
[0..15]	3	Orbit[0..15]	Orbit Low 16 bits
[0..15]	4	Orbit[16..32]	Orbit Upper 16 bits

giving a total of 102 bits per trigger at a trigger rate of 100 kHz. The order of words in TTC is TType, Event ID, DN, TIM (note different from PON case).

14.4 CTP readout GBT format

GBT data format on links *R1,R2 and R3*, see Figure 6.1 CTP readout, is discussed below. On link *R1* detectors record is sent, see Table 14.4 CTP readout GBT format: Detector Record. There are 5 GBT words per GBT frame corresponding to one bunch crossing [10].

Table 14.4 CTP readout GBT format: Detector Record

Data	GBT Frame	GBT word	Payload	Content
[0..3]	1	G0	[0..3]	Header
[4..15]		G0	[0..11]	BCID
[0..15]		G1	[0..15]	Orbit
[0..15]		G2	[16..31]	Obit
[0..15]		G3	[0..15]	DM
[0..1]		G4	[16..17]	DM

The list of interactions records, i.e. the bitwise mask of trigger inputs for given BC is sent on link *R2*, see Table 14.5 CTP readout GBT format: Interaction record. The table allows for 64 trigger inputs. There are two types of GBT frames recognised by first four bits in the first word G0 of the frame. The first type of GBT frame keeps the orbit of the interaction record while the other frame corresponds to single interaction record, i.e. the BCID and trigger input mask.

Table 14.5 CTP readout GBT format: Interaction record

Data	GBT Frame	GBT word	Payload	Content
[0..3]	1	G0	[0..3]	Header
[4..15]		G0	-	Spare
[0..15]		G1	[0..15]	Orbit
[0..15]		G2	[16..31]	Orbit
[0..15]		G3	-	Spare
[0..15]	1	G4	-	Spare
[0..3]	2	G0	[0..3]	Header
[4..15]		G0	[0..11]	BCID
[0..15]		G1	[0..15]	TIM
[0..15]		G2	[16..31]	TIM
[0..15]		G3	[32..47]	TIM
[0..15]		G4	[48..63]	TIM
…	…	…	…	…
[0..3]	N	G0	[0..3]	Header
[4..15]		G0	[0..11]	BCID
[0..15]		G1	[0..15]	TIM
[0..15]		G2	[16..31]	TIM
[0..15]		G3	[32..47]	TIM
[0..15]		G4	[48..63]	TIM

For every HB the CTP sends on link *R3* also HB map. It is also fragmented to GBT frames with five words. It contains two types of frames. The first type of GBT frame contains event ID corresponding to HB map and number of CRUs in the map. The other type of frame contains CRU ID and status of five CRUs.

Table 14.6 CTP readout GBT format: HB map

Data	GBT frame	GBT word	Payload	Content
[0..3]	1	G0	[0..3]	Header
[4..15]		G0	[0..11]	BCID

[0..15]		G1	[0..15]	Orbit
[0..15]		G2	[16..31]	Obit
[0..15]		G3	[0..15]	# of CRU(=N)
[0..15]		G4	-	Spare
[0..3]	2	G0	[0..3]	Header
[4..15]		G0	-	Spare
[0..8]		G1	[0..8]	CRU ID
[9..15]	2	G1	[0..6]	CRU status
[0..8]		G2	[0..8]	CRU ID
[9..15]		G2	[0..6]	CRU status
[0..8]		G3	[0..8]	CRU ID
[9..15]		G3	[0..6]	CRU status
[0..8]		G4	[0..8]	CRU ID
[9..15]		G4	[0..6]	CRU status
…		…	…	…
[0..3]	N+1	G0	[0..3]	Header
[4..15]		G0	-	Spare
[0..8]		G1	[0..8]	CRU ID
[9..15]		G1	[0..6]	CRU status
[0..8]		G2	[0..8]	CRU ID
[9..15]		G2	[0..6]	CRU status
[0..8]		G3	[0..8]	CRU ID
[9..15]		G3	[0..6]	CRU status
[0..8]		G4	[0..8]	CRU ID
[9..15]		G4	[0..6]	CRU status

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