DESIGN AND DEVELOPPEMENT OF THE ALICE CRU USER LOGIC FIRMWARE FOR THE MID READOUT CHAIN

A research project proposal submitted to the Faculty of Engineering and Built Environment, Cape Peninsula University of Technology, in fulfilment of the requirement for the degree of Master of Engineering.

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1st September 2020

Declaration

I declare that, this proposal is my original work. It is being submitted for the Master of Engineering at the Cape Peninsula University of Technology at Bellville campus. It has not been presented before for any degree or examination in any other university. Furthermore, it represents my own opinion not necessarily those of the Cape Peninsula University of Technology.

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Declaration by the supervisor

This research proposal has been submitted for examination with my approval as university supervisor from the department of Electrical, Electronics and Computer Engineering.

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Declaration by the co-supervisors

This research proposal has been submitted for examination with our approval as co-supervisors from a facility of the National Research Foundation (NRF) iThemba LABS.

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Abstract

To adapt with the increase in luminosity of the LHC at CERN in Geneva (Switzerland), ALICE has embarked on a major upgrade of its detectors during the long shutdown 2 period which started in 2019. The upgrade comprises, in part, of new detectors for the central system while other existing detectors such as the Muon Spectrometer will change the front-end electronics and readout. At the centre of the readout upgrade is the new approach based on the common readout unit developed to meet the ALICE requirements. This proposal concerns the user logic developed for the MID common readout unit firmware. Recent tests conducted on the MID readout chain showed potential limitations in data rates if data are collected without a pre-analysis performed with the firmware of the CRU. Therefore, alternative solutions are required. This research project will provide a new approach of processing data using a customized common readout unit user logic firmware, to meet these requirements.

1 - Background

1.1 - CERN, ALICE and MID

CERN is the world's leading laboratory for scientific research located on the border of Switzerland and France. CERN houses the Large Hadron Collider (LHC), [1]. The LHC is about 100 meters below the surface and 27 kilometres in circumference. It produces particle beams i.e. proton-proto (p-p), proton-lead (p-pb) and lead-lead (pb-pb) at ultra-relativistic energies to create, amongst other, a highly dense form of matter reminiscent of the early universe a microsecond after the big bang. Spread along the LHC ring are four individual experiments positioned around the four collision points where the beams collide. One of these experiments is A Large Ion Collider Experiment (ALICE) [2].

ALICE is a heavy-ion detector designed to reconstruct and identify a myriad of particles created in the collisions. Its main field of research is the study of the Quark-Gluon Plasma (QGP) [3], which is produced in collisions and is believed to help us understand the origin of the early universe. ALICE is an international collaboration that counts more than a thousand physicists and engineers from 132 institutes in 36 different countries including iThemba Laboratory Accelerator Based Science (iThemba LABS) [4]. The ALICE detector consists of about 18-20 sub-detectors extending over a length of 26m and 16m in height and width, weighing over 10 000 tons. The detector consists of the central and forward detectors. The forward detectors are known as the muon spectrometer. As depicted in Figure 1, the central part is located symmetrically around the interaction point (z = 0 cm) with the muon spectrometer located on the C-side (z > 0cm). One denotes the side of the interaction point for z < 0 cm as the A-side.

The Muon Identifier (MID) is one of the muon spectrometer detectors. It is composed of 72 single gap Resistive Plate Chamber (RPC) [5] detectors, arranged in 2 stations of 2 chambers each at a distance of about 16 m and 17 m from the interaction point respectively. These stations are mounted behind a 120 cm thick iron wall (muon filter) situated following the tracking stations of the spectrometer [6].

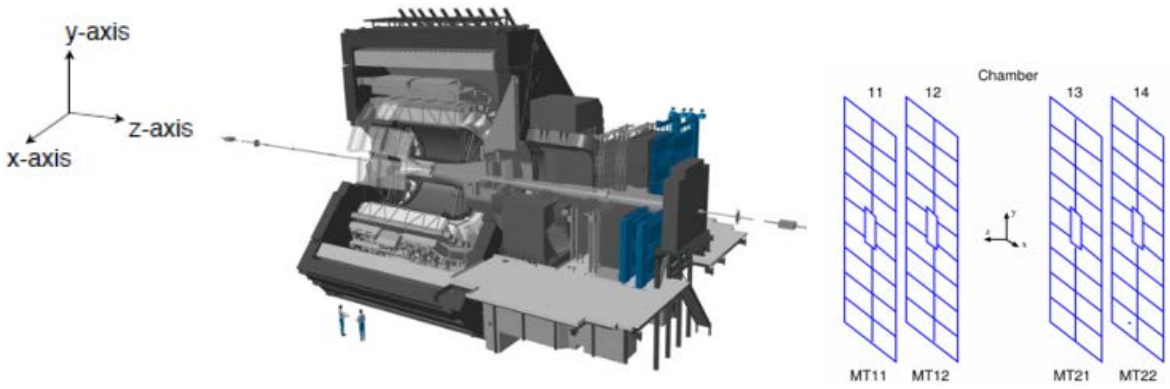

Figure 1 - Left panel: outline of ALICE detector, with its MID highlighted. Right panel: the layout of the MID stations

The RPCs as shown in figure 2 [7] consist of two plates, a positively-charged anode and a negatively-charged cathode, both made of very high resistivity plate plastic material and separated by a gas volume. Once a charged particle such as a muon passes through the chamber, electrons are knocked out of the gas atoms. These electrons in turn hit other atoms causing a mass of electrons. The electrodes are transparent to the electrons, which are instead picked up by external metallic strips after a small but precise time delay. The pattern of hit strips gives a quick measure of the muon momentum, which is then amplified by the Very Front-End (VFE) electronics, in this case by the Front-End Electronics Rapid Integrated Circuit (FEERIC) cards [8]. The signals from the FEERIC cards are then propagated to the readout chain electronics to make immediate decisions about the validity of the data.

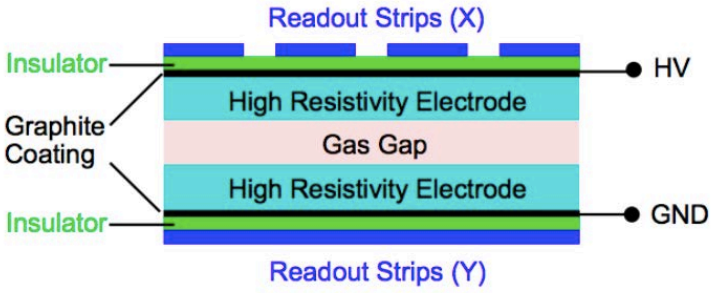

Figure 2 - Diagram of a RPC

1.2 - MID readout chain

In line with the ALICE new readout upgrade requirement [9], the MID readout chain had to be redesigned. The newly upgraded chain is composed of four different systems: The Front-End (FE) electronics, the Common Readout Unit (CRU) [10] , the Central Timing Processor (CTP) [11] and the Online and Offline (O^2) computing facility [12].

1.2.1 – FE Electronics

The FE electronics system is divided in 16 vertical regions. Each of the 16 regional areas is read out by a single VME crate [13]. Each crate contains a single regional card [14] which is then divided into two sections. Each section connects up to 8 local cards [15] via a backplane bus called J2 card [16], and transfers data to the CRU via a single Gigabit Transceiver (GBT) [17] bi-directional optical link. Each local card connects to 128 VFE channels. The GBT is an optical serial data link developed at CERN, designed for the use of the LHC, which requires high data rates and components capable of sustaining a high radiation dose. It is based on a 4.8 Gbps Serializer-Deserializer (SerDes) [18] circuit, which converts the input data, transmitted by the FE electronics to the CRU, into a serial stream of data, and deserializes the stream of data transmitted by the CRU to the FE electronics. The serial data rate of 4.8 Gbps corresponds to a 120-bit frame transmitted continuously at the interval of 25 ns, equivalent to a single LHC bunch crossing interval. The bunch crossing interval is the time between bunches of beam particles crossing each other in the LHC. In total, the FE electronics system is equipped with 16 crates, 16 regional cards, 16 J2 cards, 32 GBT links and up to 234 local cards.

1.2.2 – CRU

The CRU acts as an interface between the FE electronics, CTP and O^2 computing facility. It combines and multiplexes data from multiple FE electronics cards before forwarding it to the O^2 for data processing and storage. In total 2 CRUs are required to read out the complete FE electronics system. Each reads out 16 GBT links from 8 regional cards. The CRUs are mounted in servers located in the intermediary computer room referred to as counting room, at a distance from the radiated area in the ALICE cavern.

1.2.3 – CTP

The CTP is the decision maker of the ALICE experiment, it communicates with up to 24 Local Trigger Units (LTUs) [11] via custom serial links, including for MID detector. The LTU performs the transmission of trigger signals and emulates the CTP for use of detector development. It transmits different trigger signals to the CRUs, which are also forwarded to the FE electronics via the GBT links. In turn, the FE electronics respond to these trigger signals with potential data of interest. The LTU makes use of periodic signals called heartbeat triggers which cycle approximately every 89.4 µs (equivalent to 11.2 KHz). This serves as a timestamp for the data acquisition. The data collected by the CRU between 2 heartbeats (one LHC orbit period) is called heartbeat frame. The protocol CTP-LTU is referred as Timing and Trigger Control (TTC), which serves as communication between CTP-LTU and the CRU firmware.

1.2.4 - O^2 computing facility

The O^2 computing facility contains a hierarchy of processing units comprised of the First Level Processors (FLP) server [19], Event Processing Nodes (EPN) [20] as well as networking and storage resources. Each level of this hierarchy performs work on the data in real-time until the data are of sufficient quality for storage. The CRUs used in the chain are housed by and connected to the FLP via PCI express. The CRU-O^2 protocol requires that the O^2 is able to identify the timestamp of the heartbeat frames. This is achieved by a Raw Data Header (RDH) [21] format generated by the CRU firmware.

A block diagram overview of the MID readout chain is shown in figure 3.

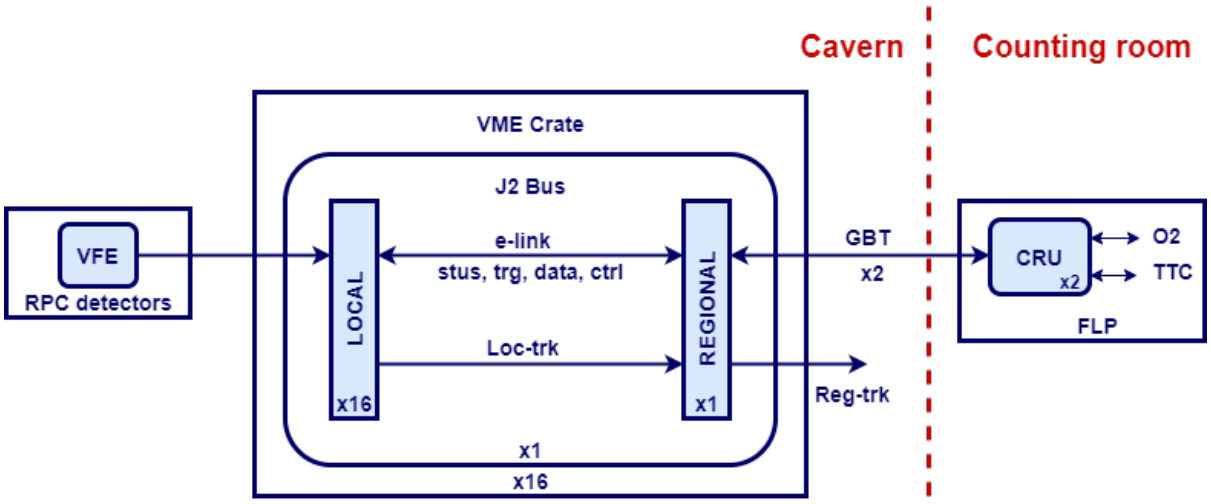

Figure 3 - MID Readout chain architecture

2 - Research problem

During the preliminary series of tests conducted on the MID systems, the newly upgraded MID readout chain showed limitations when operating without data pre-analysis performed in the CRU firmware. Among these limitations are: large data rate and incapability to process data from the complete FE electronics system.

2.1 - Large data rates

As already mentioned in the previous section, the FE electronics generate a data rate of 4.8 Gbps. This large amount of data poses a challenge to the O^2 to simultaneously perform data processing without data compression done already at the CRU firmware level. Furthermore, the MID detector is expected to read out data from collisions every 20 μs [22] and the FE electronics transmits data to the CRU every 25 ns. This means that out of 4.8 Gbps only 4 Mbps are valuable data. The rest are insignificant data that need to be suppressed. Keeping all these data in the memory leads to a low performance and inefficient usage of memory. Hence data filtering is also required at the CRU firmware level.

2.2 - Incapability to process data from the complete FE electronics

The O^2 is able to handle the data rate from a single crate (2 GBT links) at the cost of 2 core processors. Attempting to use one core to decode a single crate leads to irreversible data loss. Hence, it requires 1 core to decode 1 GBT link. However, the FLP used for the MID readout chain contains 20 cores [19]. In order to decode data from the complete FE electronics system (32 GBT links), the FLP will require 32 cores not to mention some additional extra cores needed to perform further processing of the decoded data. This makes it impossible for the FLP to process data from the complete FE electronics system without data filtering being performed at the CRU firmware level.

The MID is searching for alternative ways to process data. The most efficient and cost-effective solution is to design a customized user logic, that will be implemented in the CRU firmware, to facilitate first stage data pre-analysis before transmission to the O^2 computing facility.

3 - Literature review

The ALICE upgrade [9] entails the replacement of some detectors while most others, including the muon spectrometer (Muon Tracking and Muon Identifier) are equipped with a new readout system to allow the detectors to be read-out at near the expected interaction rate of 50 kHz Pb-Pb collisions.

The experiment will generate ~3.5 Terabytes per second [23]. To keep up with this new specification, the detectors will use a high-speed readout approach based on a CRU. The development of the CRU has been the focus of many researchers for quite a few years now to name few:

O.Bourrion, J. Bouvier from *the Institute of Engineering at the university of Grenoble, France*, F.Costa from CERN, E.David, J, Imrek, T.M Nguyen from *Wigner Research Center for Physics in Budapest, Hungary* and S. Mukherjee from *Bose Institute in Mumbai, India*.

As illustrated in figure 4 [24], the CRU board is based on an Intel ARRIA 10 high performance Field Programmable Gate Array (FPGA) [25] processors equipped with multiple gigabit optical inputs and outputs connectors and a PCI-express interface.

Figure 4 - Overview of ALICE CRU

The CRU firmware is developed to accommodate most detectors in the ALICE experiment. In particular, to share the common features and interfaces, to provide the possibility to all detectors to transmit data with no data processing done in the CRU, to authorize timing and trigger-signals distribution and initiate the FE electronics configuration. In addition, some specific detector features, called user logic, can be integrated in the CRU firmware via a specific compilation [23]. It is developed by the detector teams and has the capability to perform low-level data processing and other additional features via the CRU firmware before forwarding it to the O^2 computing system for further analysis. Each detector group has their own requirements. For this purpose, a user logic module at the heart of the CRU firmware is left to be customized by the individual detector group. Each has the responsibility to develop their own custom user logic.

4 - Objectives of the research

The eventual aim of the research, is to improve the data processing with the CRU firmware. This will be done by designing and developing a customized user logic firmware capable of meeting the requirements stipulated in the research problem. To achieve this goal, the following steps have to be met:

- Filter the incoming GBT data by suppressing insignificant data
- Identify all possible event frames in the e-link data
- Identify and report errors in the GBT data
- Synchronize the processed data with the TTC information
- Operate in both trigger and continuous readout mode

- Multiplexing of GBT data
- Generate heartbeat frames
- Transmission of heartbeat frames to the FLP

5 - Research design and methodology

5.1 – Constraints and requirements

The requirements and constraints for the proposed research are discussed and agreed upon with the co-supervisors at iThemba LABS, ALICE MID experts responsible for the readout in France as well as CERN experts responsible for the development of the CRU firmware. Similar to the CRU firmware, the MID user logic will interact with different interfaces such as the TTC, GBT and the PCIe end points. Each interface has their own requirements. Therefore, the user logic must be able to accommodate a variety of specifications and constraints. Figure 5 gives an overview of the CRU firmware block diagram incorporating the MID user logic and the main interfaces.

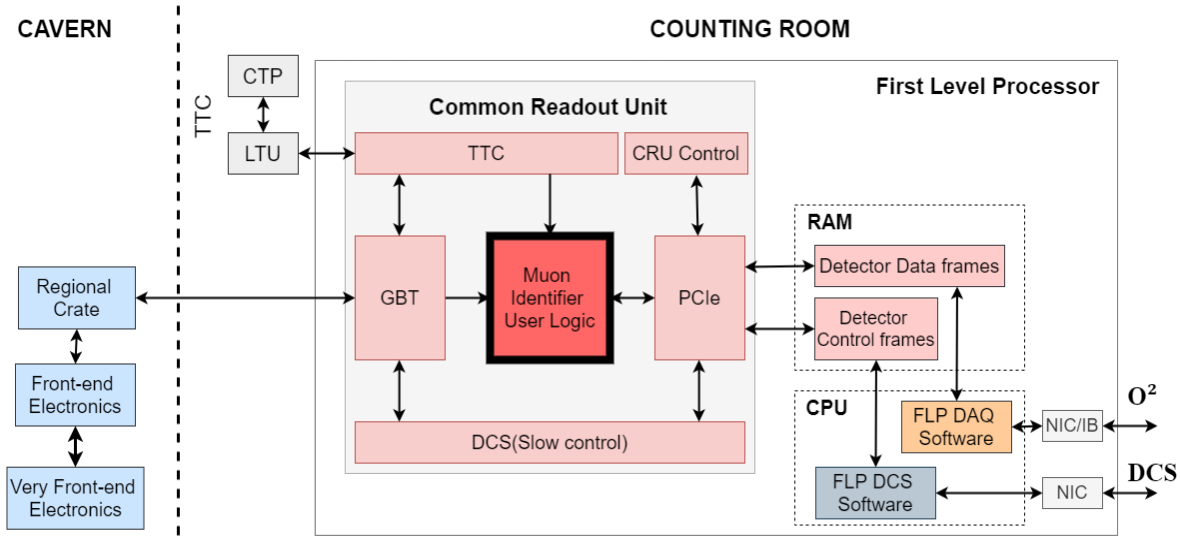

Figure 5 - Overview of the CRU firmware incorporating the MID user logic

CRU software and firmware components provided by ALICE CRU teams at CERN

MID user logic provided by CPUT and iThemba LABS (this research project)

FLP Detector control system (DCS) software provided by the MID DCS team: Laboratory of Physics Clermont-Ferrand (LPC) [26] at Clermont-Ferrand university

VFE and FE electronics provided by the MID FE team in France: LPC and Subatomic Physics and Associated Technologies (Subatech) [27] at the university of Nantes

FLP Data acquisition software provided by MID O^2 team at Subatech

5.2 – Conceptual design of the user logic

At this stage the needs have been defined and the initial research completed. The conceptual design shown in Figure 6 provides a brief description of the proposed research project in terms of sets of integrated ideas and concepts.

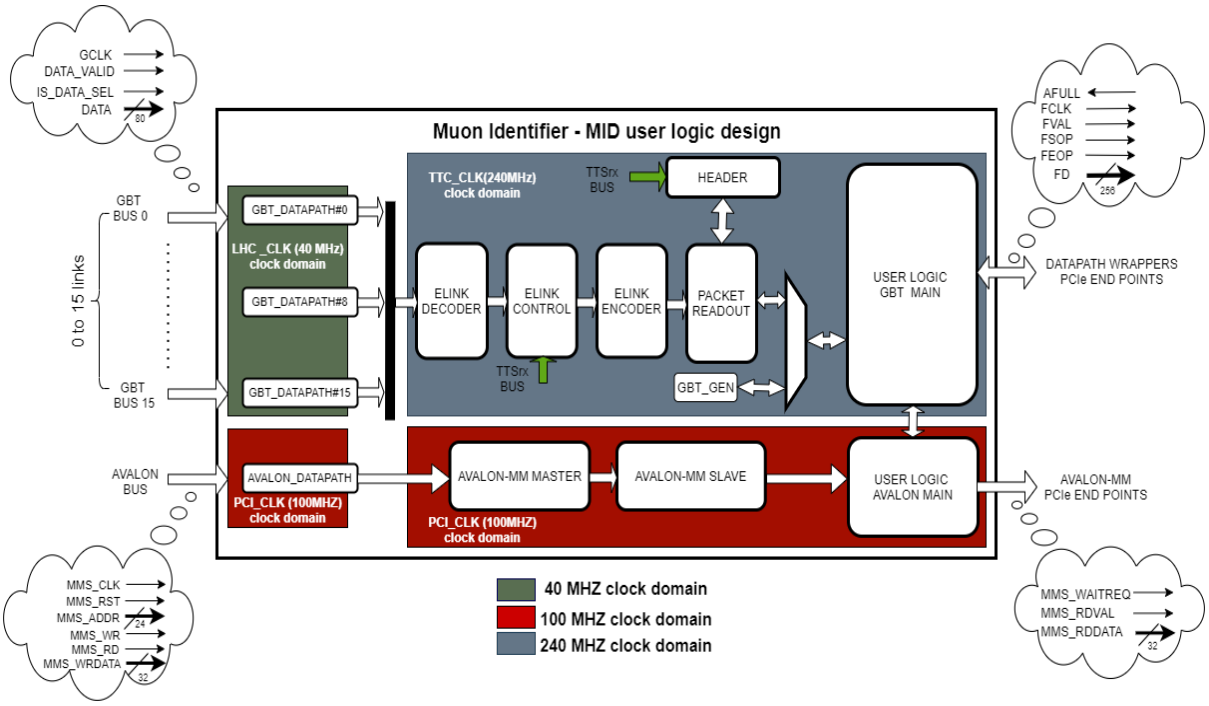

Figure 6 - MID user logic conception design

The conceptual design of the user logic is broken into multiple components and these components will perform the following functions:

- **Elink decoder** will be used to deserialize the serial stream of data transmitted from the FE electronics into 10 individual sub-frames, suppress the insignificant data and decode the sub-frame data
- **Elink Control** will be used to identify potential errors located in the decoded sub-frame data, synchronize it with the TTC and store the result in a memory
- **Elink encoder** will extract data from "elink control" memories, perform multiplexing of all sub-frame data and generate payloads of 256 bits each
- **Header** will generate raw data headers at the reception of every heartbeat trigger transmitted by the TTC
- **Packet Readout** will be used to generate heartbeat frame data consisting of several blocks (RDH + Payloads)
- **User logic datapath** will perform the data transmission to the FLP. The format of the data as well as the way errors will be handled are yet to decided
- **User logic Avalon** is still work in progress. The signals that will require to be configured via Avalon ports will be determined throughout the project

5.3 - Development and Tests

To integrate the user logic with the CRU firmware, it is required to develop the user logic in VHSIC Hardware Description Language (VHDL) [28] using Intel Quartus prime pro edition 18.1[29]. The functional verification of the user logic will be simulation based using Modelsim Intel starter edition 10.6b [30].

Expected tests for conformance might include testing of the user logic using a fully functional testbench setup available at iThemba LABS where the following equipment are available:

- 1 Power supply
- 1 LTU
- 1 FLP server housing a single CRU
- 1 MID VFE and FE electronics emulator prototype card
- 1 Crate (16 local cards, a single regional and a single j2 card)
- 1 Rack enclosure
- 2 MTP to LC 9/125 single mode fibre patch cables

5.4 - Collaborators

This project will be coordinated within the Cape Peninsula University of Technology and the MID collaboration: iThemba LABS, Subatech, LPC as well as CERN. In particular, this includes support from the MID FE electronics expert Dr Christophe Renard, MID O^2 expert Dr Diego Stocco as well as ALICE CRU experts at CERN Dr Filippo Costa and Dr Olivier Bourrion.

5.5 - Gantt Chart

This project has been established and scheduled into a Gantt chart. It will be performed fulltime and the tentative completion time will be July 2021. The Gantt chart is described in details in Appendix A.

6 - Delineation of the research

The delineation of the research is limited to the development of the CRU user logic firmware for the MID readout chain: FE electronics, CRU, CTP and O^2 computing system. Involvement in these systems is limited to the interfaces and input/output characteristics of these systems. Furthermore, integration with the existing system is only tested through conformance with establish requirements and practice.

For the purpose of this master project, the user logic will be developed for a single crate. The tests and verification of the code will be simulation based only. Testing the code on the testbench setup available at iThemba LABS as well as on the MID of ALICE detector at CERN is beyond the scope of this research project.

7 - Expected outcome and contributions of the research

The expected outcome of this research project will be to produce a well-documented thesis as well as a user logic prototype capable of meeting the requirements of the MID readout chain. The user logic prototype is expected to adhere to the functionalities listed below:

- **Low data rate**: The prototype must be able to significantly reduce the data rate
- **Efficient usage of memory**: The prototype must efficiently use the memory allocated
- **Reliability**: Data produced by the prototype must be reliable
- **Flexibility:** The prototype must easily be configurable and expendable
- **Stability:** The prototype is expected to run over long periods, hence it must be stable

The results of this research will contribute towards the ALICE experiment in particular towards the development of a realistic user logic capable of processing a complete MID readout chain. More importantly, it will add to the visibility in terms of technological skills for South Africa in the ALICE Collaboration at CERN, which in turn could lead to confidence for future project involvement.

8 - Summary

To summarize, this project will focus on the design and development of the user logic prototype for a single crate containing 2 GBT links. It will be designed in VHDL and integrated with the CRU firmware using “Intel Quartus prime pro edition 18.1”. This prototype will be validated in simulation using “Modelsim Intel stater edition 10.6b”. As one of the development sites, iThemba LABS houses the MID readout chain components to facilitate the conduction of the research and development of the user logic prototype. The outcome of this research will contribute towards the development of a realistic user logic capable of processing data from a complete MID readout chain.

As for the timeline, the intention is to complete the project in June 2021 as indicated in the research schedule.

9 - Keywords

CERN; Large Hadron Collider; ALICE experiment; Muon Identifier; Common Readout Unit; user logic firmware.

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Appendix A - Gantt Chart displaying project activities

Research project Gant Chart
Date: 1- Sep-2020
Student name: D.O THYS-DINGOU
Student number: 212349721
Supervisor name: Dr A. Raji
Full Time