Master of Engineering Proposal 2020

Title: ***ALICE Muon Identifier (MID) common readout unit user logic firmware***

Supervisor: **Dr. Atanda Raji**
Co-supervisor(s): **Prof. Z Buthelezi, Dr. SV Förtsch**
Student Candidate: **Dieuveil Orcel Thys-Dingou**
Student Number: **214349721**

Abstract:

This project forms part of the ongoing ALICE (A Large Ion Collider Experiment) detector upgrade for the European Organization for Nuclear Research known as CERN. NRF iThemba LABS contributes to the ALICE Muon spectrometer upgrade, in particular, the Muon Identifier (MID). NRF iThemba LABS is responsible for the CRU firmware user logic development, including setting up a testbench for the data acquisition readout chain as well as develop the firmware code and maintenance thereafter. These activities are reported and coordinated through the MID CRU collaborations composed of members from South Africa (iThemba LABS), France (Subatech, Clement-Ferrand) and Switzerland (CERN). However, this particular project will focus solely on the MID CRU user logic development and testing thereof. The introduction, project description, scope and requirements follow.

Introduction

Based on data collected in Run 1 and 2 (~10 petabytes of raw data) ALICE is the leading heavy-ion experiment in the world and is quickly expanding the knowledge gathered in previous experiments all over the world. For the Large Hadron Collider (LHC) Run 3 which will commence from 2021 onwards, ALICE identified key physics measurements to further our understanding of the hot and dense matter – the Quark-Gluon Plasma (QGP) created in these collisions and devised a strategy to facilitate these measurements. Many of the proposed observables require a shift in the data taking strategy, moving away from triggering a small subset of events to online processing and recording of all collisions delivered by the LHC. To achieve these goals, ALICE detector is being upgraded. The upgrade entails the replacement of some detectors while most other detectors, including the Muon spectrometer (Tracking and MID), are moving to new front-end electronics and readout system to allow all detectors to be read out at near the expected interaction rate up to 50 000 lead-lead (Pb-Pb) collisions per second.

Currently, the ALICE detector is going through a major upgrade in preparation for Run 3 at CERN. At the center of the ALICE upgrade strategy is a high-speed readout approach based on a Common Readout Unit (CRU) developed for detector data readout, concentration, reconstruction, multiplexing and data decoding onto the online-offline (O2) computing farm. The CRU incorporates the Intel Arria 10 FPGA (Field Programmable Gate Array) and a Gigabit transceiver board (GBTx).

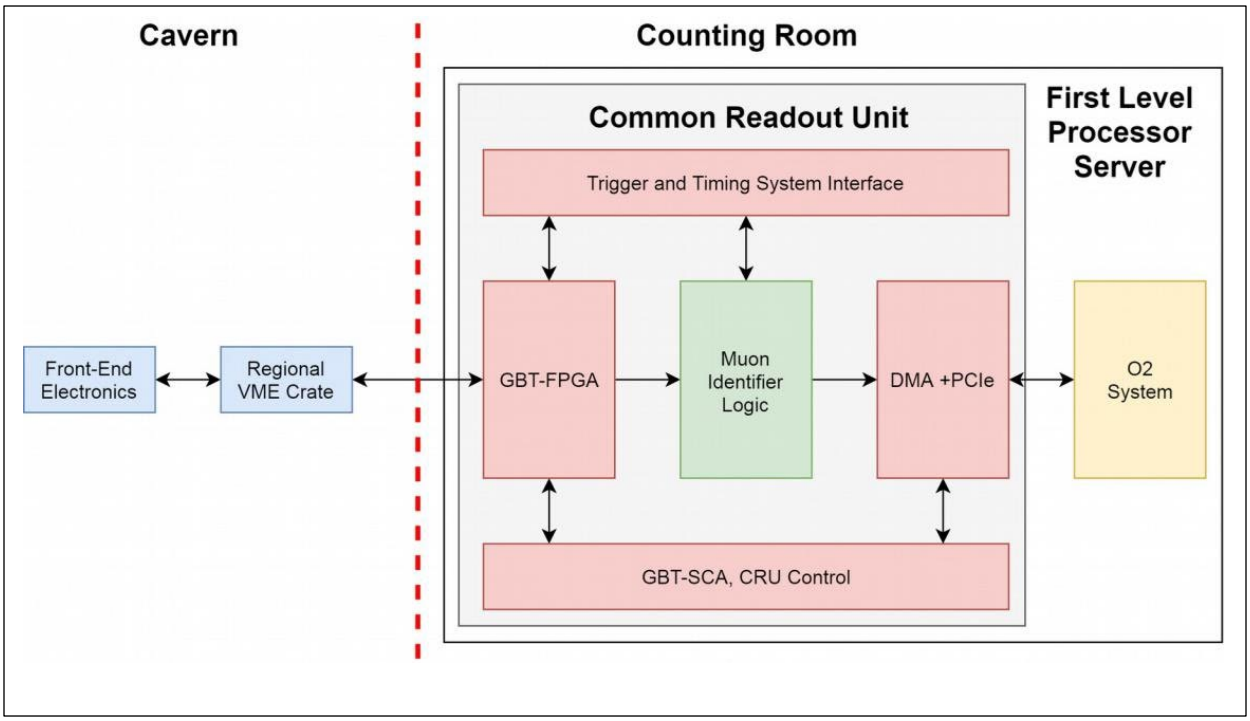
To interface the CRU to different components of the data acquisition chain: front-end electronics (FEE), central trigger processor (CTP) and online-offline (O2) system, a CRU user logic firmware is necessary. As shown in the schematic below the MID CRU user logic firmware will interface the MID FEE (composed of 16 regional cards and 234 local cards in total) via 2 gigabit

transceivers (GBTx), the central trigger processors (CTP) or trigger and timing system (TTS) and the first -level processor (FLP) which is part of the online-offline (O2) computing system.

A single MID FEE regional card is composed of two parts, each part transfers the data to the CRU via a single GBT link and connects up to 8 local cards via 8 e-links and 2 additional regional e-links using the GBT protocol. A full MID crate contains 2 GBT links, 1 regional card, resulting in up to 16 local cards per crate.

The CTP is the decision maker of the system, it transmits different signals (trigger and continuous) modes to detectors, in return, the detectors will send a signal input. The continuous readout system makes use of periodic signals called heartbeat (HB) triggers approximately to every 89.4ms (equal to the LHC orbit). This serves a timestamp of data acquisition called heartbeat. There will be new triggers for the ALICE MID along with the heartbeat triggers in continuous and trigger readout modes.

The O2 facility contains a hierarchy of processing units comprised of CRU, first level processors (FLP), event processing nodes (EPN) as well as networking and storage resources. Each level of this hierarchy performs work on the raw data in real-time until the data is of sufficient quality for storage.



The CRU-O2 protocol requires that the O2 system needs to be able to identify data packets transferred by the readout electronics. This is achieved by the raw data header (RDH) generated by the user logic firmware of the CRU.

Project description

The master of engineering part of the project concerns the development of the MID CRU user logic firmware designed program the CRU FPGA using VHDL (VHSIC-HDL, Very High-Speed Integrated Circuit Hardware Description Language). To accomplish this task, it is important to understand the requirements of the user logic firmware as well as the expectation in line with the ALICE online-offline (O2) data format. The MID CRU user logic firmware is expected to perform the following functions:

- Receiving raw data from the front-end electronics (FEE) via GBT links and transmit it to the central CRU firmware after reformat and zero suppression of data.
- Receiving continuous trigger information from the central trigger processor (CTP) or timing and trigger system (TTS) via CRU firmware.
- Handling errors found in the front-end electronics data.

Scope and expectations

The scope is limited to the development of the user logic firmware for the MID CRU readout system: FEE, CTP/TTC, FLP (O2). Involvement with the systems is limited to the interfaces and input/output characteristics with those systems. Furthermore, integration with the existing system is only tested through conformance with established requirements and practice.

For the purpose of the master engineering project, the MID user logic firmware should be developed for a full readout crate (2 GBT links) composed of 16 local cards and 1 regional card. Expected tests for conformance should include testing the user logic firmware using:

- Intel Quartus prime 18.1 pro
- Modelsim – Intel FPGA
- Realistic testbench available in room s64 at iThemba LABS as well as on the realistic detector at CERN (Geneva, Switzerland).

Requirements

The project comes with a lot of pressure and expectations. Therefore, the candidate should be someone with:

- BTech in electrical engineering with an average of 65 %
- Accustomed to the ALICE spectrometer
- Good understanding in power electronics
- Good understanding in digital electronics
- Familiarity with the Unix/Linux environment and script languages (CShell, Tcl).
- Knowledge and experience in FPGA design.

Mr. DO Thys-dingou meets these requirements. He was an electrical engineer intern at NRF iThemba LABS working on the upgrade of the ALICE muon chambers as his BTech final year project in 2018. Most importantly he has been accepted for his master of engineering at Cape Peninsula University of Technology (CPUT) in 2020 and he is already familiar with the expectations and pressure associated with this project.

Available facility/Infrastructure

A fully functional testbench setup is available in room s64 at iThemba LABS. At the moment is equipped with the MID front-end electronics prototype card, with an embedded GBT chip, CTP/Local Trigger Unit (standalone emulator of the TTS) and CRU card loaded on the new generation Dell R740 FLP server. This testbench will be improved in May 2020 as we expect to populate the VME crate with 1 regional card, 16 local cards and 1 J2 bus backplane which will be provided the collaborators from Subatech (Nantes, France). The FLP is fully equipped with the installation of the CRU-O2 software and Intel Quartus prime pro 18.1 (licensed) for the configuration and design of the user logic firmware.

Funding implications

About R20 000 will be available via the co-supervisor's RAIP funds. To top this up, we applied for the NRF iThemba LABS top-up funding for 2020. We have also expressed our intent to solicit funding from the SA-CERN program. Further discussions with SA-ALICE team leader have taken place.

Since this project requires travel to CERN (Geneva, Switzerland) for a period of time, the travel funds will fully be sponsored by the SA-CERN program.

Collaborators

These activities will be coordinate within the **Cape Peninsula University of Technology** (CPUT) and the MID collaboration: NRF iThemba LABS, Subatech and Clement-Ferrand (France) as well as experts from CERN (Switzerland). Progress will be closely monitored in house, via the and by MID experts such as **Dr. Christophe Renard** (in charge of the design of the front-end electronics), **Dr. Diego Stocco** (in charge of the online-offline system) and **Dr. Pascal Dupieux** (project coordinator). Additional support will come from CERN CRU experts such as **Dr. Filippo Costa** (in charge of the CRU software) and **Dr. Olivier Bourrion** (in charge of the CRU firmware).

Project timelines

The project timeline should be aligned with the timelines of the upgrade and commissioning at CERN, 2020 February – 2021 July.

February 2020
Visit to CERN to meet with collaborators to start improvements on the existing user logic firmware code.
Make the necessary adjustments in consultations with CRU experts at CERN.
March 2020
Improve the user logic firmware code to include a full crate define above.
Conduct test on the testbench located at iThemba LABS using the MID FEE prototype card.
Presentation of the progress to collaborators during the ALICE Mini and ALICE Weeks.
April – June 2020
Visit CERN to conduct the first test of the MID user logic firmware code on a realistic detector setup 100 meters underground in the cavern at P2. (**Postponed**).
July – Dec 2020
Improve the MID user logic firmware code for integration in core ALICE online-offline (O2) system and conduct necessary tests.

Presentation of the project at the special applied session at SAIP 2020.
Presentation of the progress to collaborators during the ALICE mini and ALICE weeks.
Jan 2021 – July 2021
Commission of the ALICE MID common readout unit user logic firmware
Thesis write up.