FEERIC, a very-front-end ASIC for the ALICE Muon Trigger Resistive Plate Chambers

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Summary

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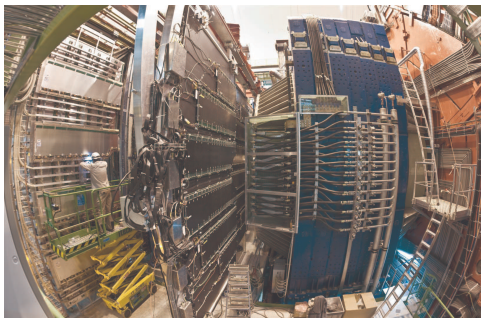
Introduction

- *The ALICE Collaboration at the CERN-LHC has started a vast program of upgrades of the detector in the context of the increase of the luminosity of the LHC from 2018 on;*
- *The present very front-end electronics (VFE) of the Muon Trigger, whose acronym is ADULT, must be replaced to limit the aging of the Resistive Plate Chambers (RPCs) in the future expected operating conditions;*
- *For this purpose, the new VFE, FEERIC (Front-End Electronics Rapid Integrated Circuit), will have to perform an amplification of the analog input signal (this is not the case for ADULT). This will allow to operate the RPCs in a low-gain avalanche mode, with a much smaller (factor 3-10) charge deposit in the detector with respect to the present set-up;*
- *This VFE represents 21,000 channels, distributed over 2400 electronics cards equipped with one or two FEERIC ASICs. A total of 3000 ASICs of 8 channels each is necessary.*



Summary

Requirements for FEERIC

- *The future ASIC has to insure mainly the following functions: amplification, discrimination and LVDS output stage.*

ASIC technology	0.35μm CMOS
Number of ch.	8
Input polarity	$\pm$
Dynamic range	Q=20 fC-3 pC
Input noise (rms)	$< 4fC$
Power cons.	$< 100mW/ch$
Power supply	3 V
One-shot	yes(100ns)
Time resolution (rms)	< 1 *ns*
Time walk	< 2 *ns*
Output format	LVDS, 23 $\pm$ 2 ns

Table: Requirements for the ASIC FEERIC.

Summary

General scheme of FEERIC

- *One channel block diagram is composed of three main stages:*
  - *The transimpedance amplifier;*
  - *The zero-crossing discriminator;*
  - *The one-shot and the LVDS output stage.*

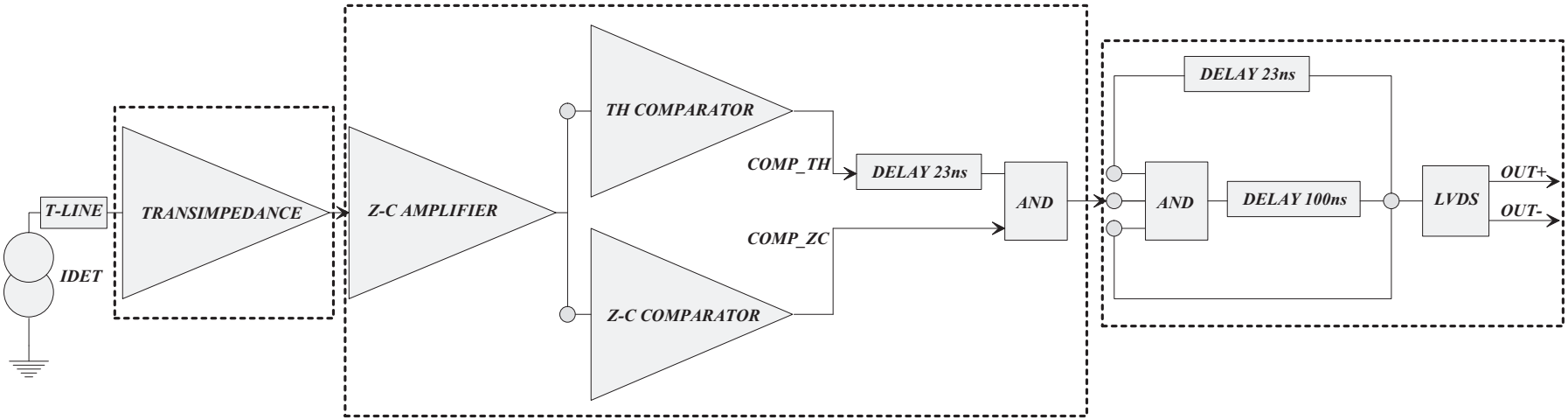


Figure: One channel block diagram of FEERIC.

The transimpedance amplifier

- *The first stage of the VFE is the transimpedance amplifier, which must be able to handle positive and negative signals;*
- *Stability issue for current preamplifier is one of the major problems. The input impedance can be represented by an RLC equivalent circuit;*
- *To obtain a stable system,* $C_f = 2 \times \sqrt{\frac{C_i}{R_f G_0 w_0}}$
  - C_i *is the input capacitance;*
  - C_f *is the feedback capacitance;*
  - R_f *is the feedback resistance;*
  - $G_0 w_0$ *is the GBW of the amplifier;*
- *The input impedance is approximately equal to* 0.1 Ω*. To obtain a proper impedance adaptation, a resistance of* 50 Ω *is added in series.*

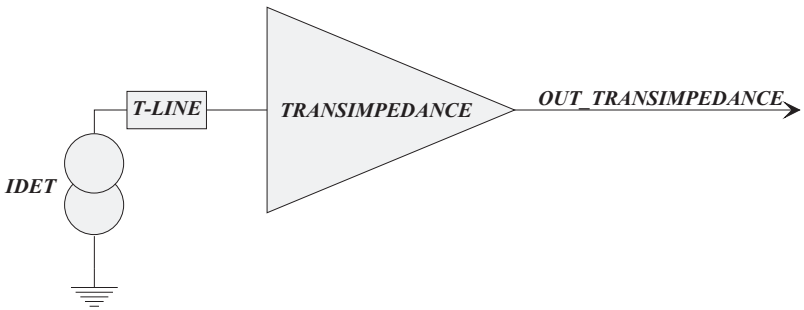


Figure: Schematic of the transimpedance.

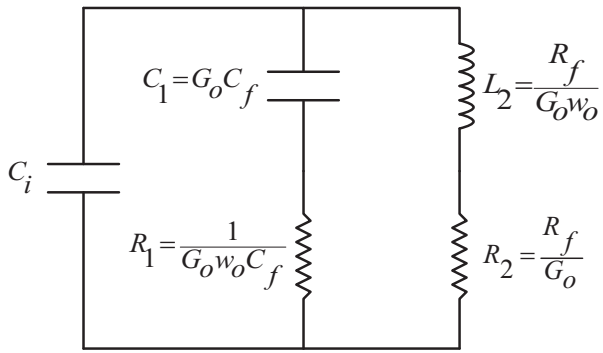


Figure: Input impedance.

The structure of the amplifier

- *The amplifier used is an OTA with a resistive feedback;*
- *The main sources of noise are the two input transistors T01 of the OTA. Their sizes and biasing current have been optimized to fulfill the low-noise requirement.*

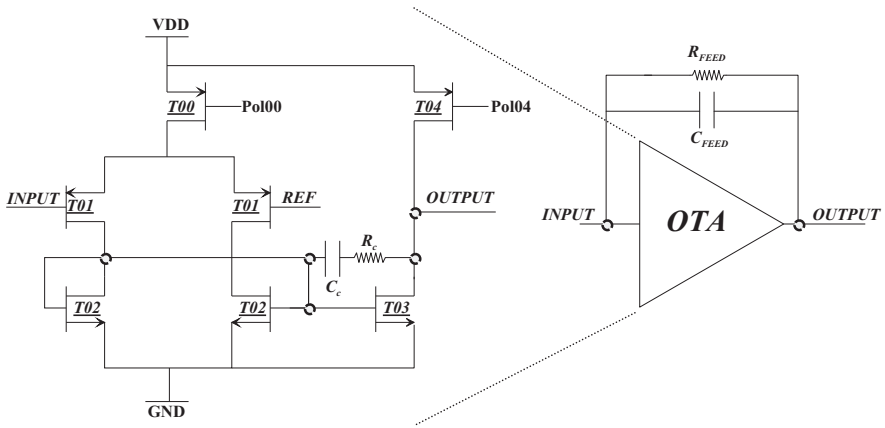


Figure: Schematic of the amplifier.

Power supply	3 V
Consumption	6.6 mW
Gain	72 dB
Bandwith -3 dB	130 kHz
GBW	3.3 GHz
Phase margin	65 degrees

Table: Characteristics of the amplifier.

The zero-crossing discriminator

- *A zero-crossing discriminator delivers a signal whose timing (relative to the input signal) is amplitude-independent;*
- *A CR network differentiates the input signal and produces a bipolar pulse crossing the zero in correspondence of the peak of the input signal. In the hypothesis that input signals have the same peaking time, the zero-crossing time is independent of signal amplitude and can be used as time reference.*

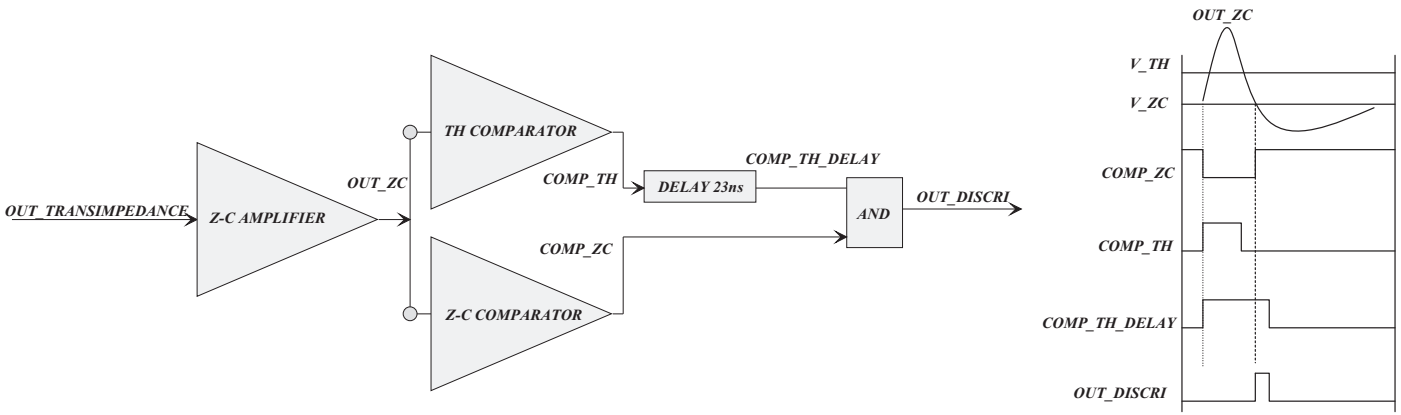


Figure: Schematic of the zero crossing discriminator.

The architecture of the comparator

- *FEERIC makes use of two comparators;*
- *The architecture of the comparator is a good trade-off between time response accuracy and power consumption.*

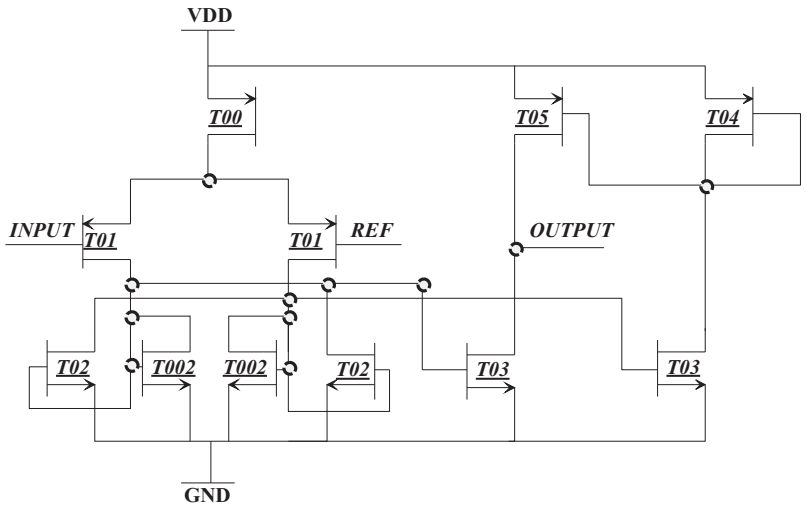


Figure: Schematic of the comparator.

Power supply	3 V
Consumption	5.3 mW
Sensitivity	400 μV
Offset	1.3 mV

Table: Characteristics of the comparator.

The one-shot and LVDS output stage

- *The one-shot system permits to obtain an output signal width equal to 23 ns and after a signal passing the threshold, the electronics is blind during 100 ns;*
- *Finally, an LVDS output stage allows to drive an output signal of ±350 mV on a resistive load of 100 Ω at the end of the 20 m long cable.*

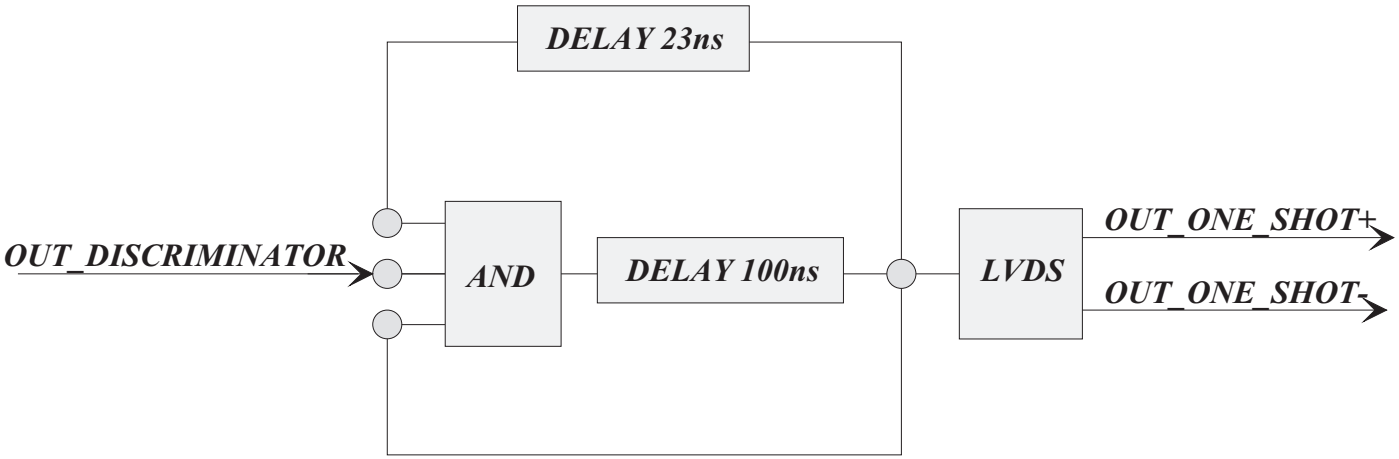


Figure: Schematic of the one shot and LVDS output stage.

Testbench

- *To characterize the FEERIC ASIC, we used two main measuring equipments.*
  - *An HP pulse generator 81110A (330 MHz), with 2 ns of rise time for input signal. This generator gives a pulse in series with a capacitance of 1 pF;*
  - *A signal analyzer Tektronix CSA7404B (4 GHz, 20Gs/s) to measure the delay between the input and the output of FEERIC.*

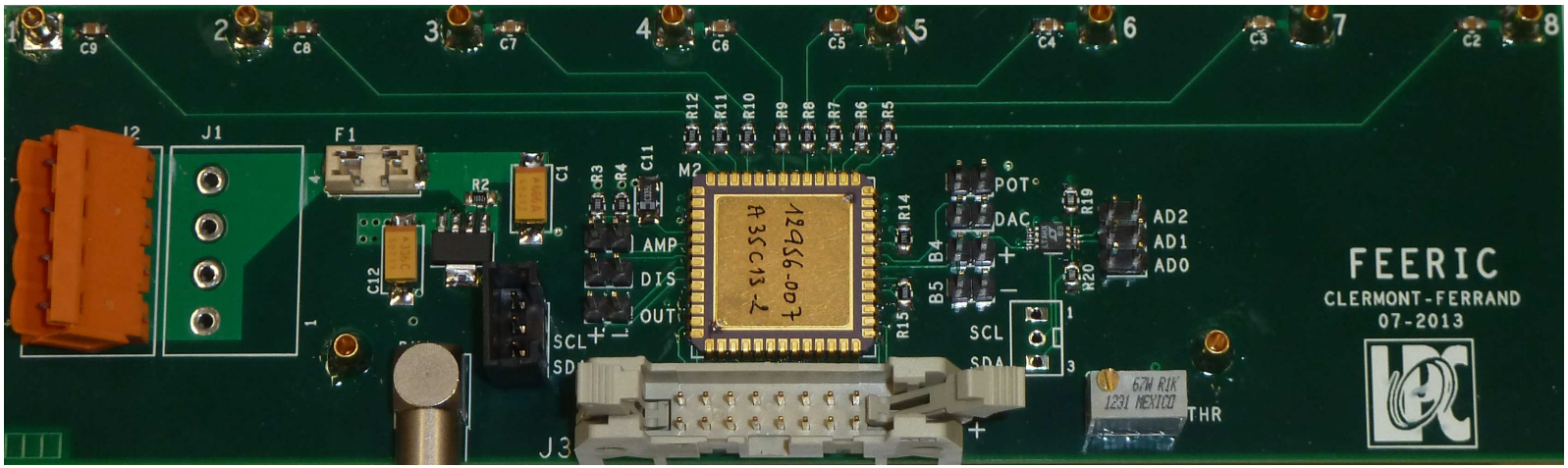


Figure: Image of FEERIC's card.

Test Results

- *The minimum threshold above noise is 8 mV (in testing conditions);*
- *The gain is 0.33 mV/fC in test and 0.4 mV/fC in simulation.*

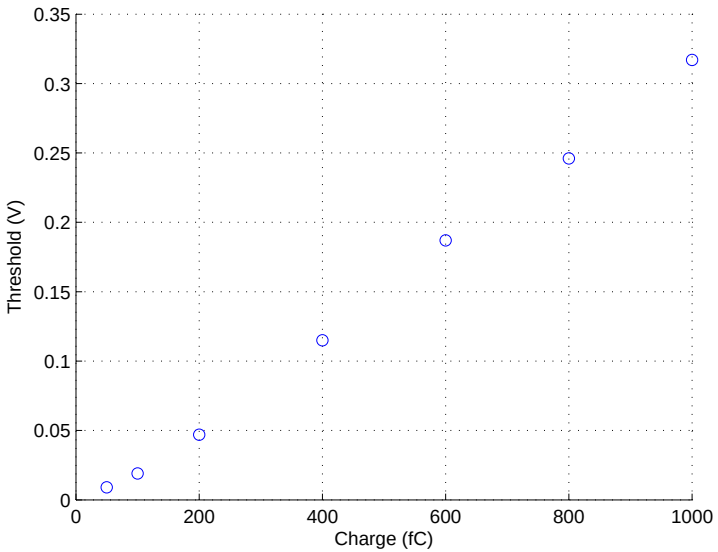


Figure: Evolution of the positive threshold with input charge.

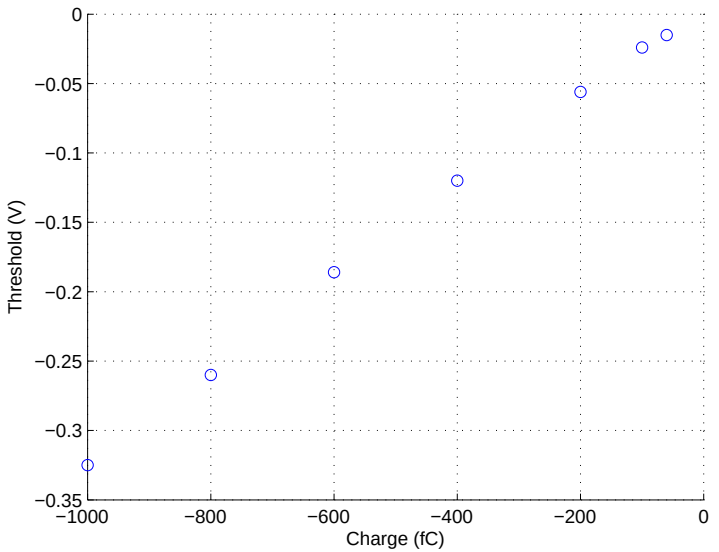


Figure: Evolution of the negative threshold with input charge.

Test Results for positive charge

- *The results are obtained for a fixed threshold value of 20 mV;*
- *In testing conditions, the time resolution is 400 ps rms for an input charge of 100 fC. In transient noise Cadence simulation (20 runs), the time resolution is 200 ps rms for an input charge of 100 fC;*
- *In testing conditions, the time walk is 900 ps for the whole positive charge range. In Cadence simulation, the time walk is less than 500 ps.*

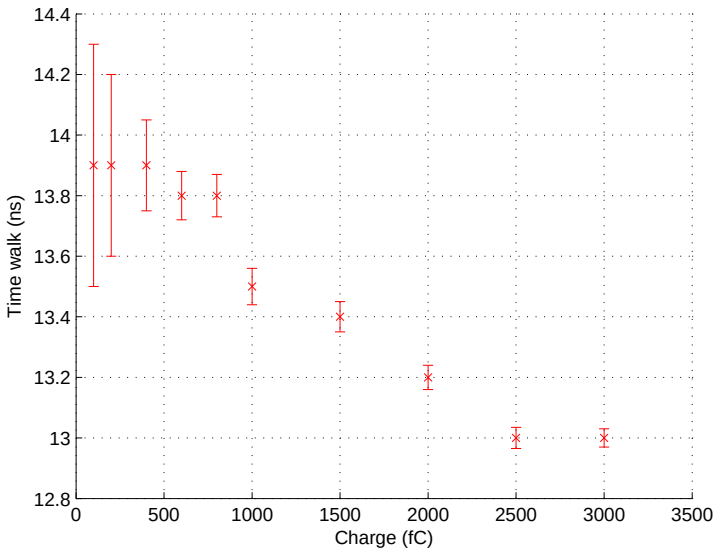


Figure: Time walk and resolution for positive charge.

Charge	Measure	Simulation
100 fC	400 *ps*	200 *ps*
200 fC	300 *ps*	100 *ps*
1 pC	60 *ps*	20 *ps*
3 pC	30 *ps*	10 *ps*

Table: Time resolution for positive charge.

Test Results for negative charge

- *The results are obtained for a fixed threshold value of - 20 mV;*
- *In testing conditions, the time resolution is 500 ps rms for an input charge of - 100 fC. In transient noise Cadence simulation (20 runs), the time resolution is 200 ps rms for an input charge of - 100 fC;*
- *In testing conditions, the time walk is 900 ps for the whole negative charge range. In Cadence simulation, the time walk is less than 900 ps.*

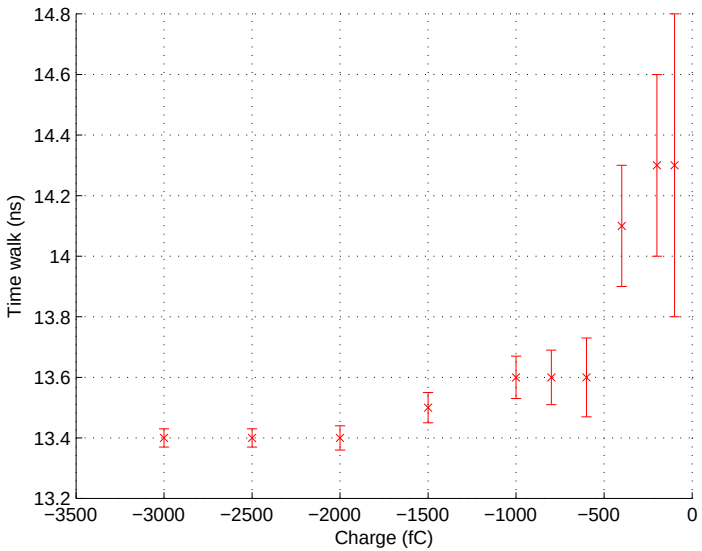


Figure: Time walk and resolution for negative charge.

Charge	Measure	Simulation
- 100 fC	500 *ps*	200 *ps*
- 200 fC	300 *ps*	100 *ps*
- 1 pC	70 *ps*	20 *ps*
- 3 pC	30 *ps*	10 *ps*

Table: Time resolution for negative charge.

Summary

Conclusion

- *The FEERIC ASIC, an 8-channel VFE for the ALICE Muon Trigger RPCs, has been designed in the AMS* $0.35\mu m$ *CMOS technology;*
- *The time resolution is less than 500 ps rms for an input charge of* ± 100 *fC;*
- *The time resolution is 30 ps rms for an input charge of* ± 3 *pC;*
- *The cross-talk is less than 2% for an input charge of* ± 3.5 *pC and a threshold of* ± 20 *mV;*
- *The global power consumption per channel is 60 mW, with a 3 V power supply voltage;*
- *The performance of FEERIC exceeds the ones required for operation in ALICE, opening a larger field of application for this ASIC.*