Abstract

A Large Ion Collider Experiment (ALICE) at the Large Hadron Collider (LHC) at CERN is undergoing a major upgrade by replacing some of its sub-detectors with new ones and others receiving new front-end electronics to handle the expected higher lead-lead collision rates in the next running period (Run 3) foreseen to start in 2022. The upgrade requires in part, new sub-detectors for the central system while other existing sub-detectors belonging to the Muon Spectrometer such as the Muon Trigger (MTR) which has been renamed to Muon Identifier (MID) will employ a continuous readout of the data from the readout electronics, in contrast to the previously triggered readout. At the center of the upgrade is a new approach based on the Common Readout Unit (CRU) developed to meet ALICE requirements. In particular, to share the common features and interfaces, and to provide the possibility to read out all sub-detectors. Due to the rise in data quantity, as well as the high collision and acquisition rates, typical methodologies are impossible to employ without massive efforts to expand processing capacity. Since the required scaling of computing infrastructure could not keep up with the MID increased data flow, a new acquisition and processing paradigm has to be established. The CRU firmware provides a specific sub-detector feature called user logic, which is a customizable component that can be used to enhance its capabilities by providing extra features such as (ie. zero suppression, synchronization, etc...) to meet the requirements of any sub-detector.

This research project provides a new approach to process the MID data based on a user logic prototype. The key aims of this thesis are to plan, build, evaluate and validate the user logic component. Innovative methods have been used to reduce the bandwidth produced by the sub-detector readout electronics, as well as adaptations to facilitate data handling later in the processing chain. Research procedures, simulations, evaluation methods, and applied methods are used to build a consistent prototype design.

Acronyms

ACORDE	-	A Cosmic Ray Detector
ADC	-	Analog-Digital Converter
ADULT	-	A DUaL Threshold
ALICE	-	A Large Ion Collider Experiment
ATLAS	-	A Toroidal LHC ApparatuS
CRU	-	Common Readout Unit
EMCal	-	Electromagnetic Calorimeters
FMD	-	Forward Multiplicity Detector
HMPID	-	High Momentum Particle Identification Detector
ITS	-	Inner Tracking System
LHC	-	Large Hadron Collider
LHCb	-	Large Hadron Collider beauty
LS2	-	Long Shutdown 2
MCH	-	Muon Chamber
MID	-	Muon Identifier
MTR	-	Muon Trigger
NRF	-	National Research Foundation
LABS	-	Laboratory for Accelerator-Based Science
FPGA	-	Field Programmable Gate Array
O^2	-	Online Offline
PHOS	-	Photon Spectrometer
PMD	-	Photon Multiplicity Detector
QGP	-	Quark-Gluon Plasma
SDD	-	Silicon Detector Drift
SPD	-	Silicon Pixel Detector
SSD	-	Silicon Strip Detector
TOF	-	Time Of Flight

TRD   -   Transition Radiation Detector

ZDC   -   Zero Degree Calorimeter

Chapter 1

Introduction

Since the early days of its employment in the 1960s, the distinctive qualities of Field Programmable Gate Arrays (FPGAs) such as high integration, flexibility, low power, and high bandwidth communication have allowed various new and critical approaches. FPGAs are the result of multiple generations of sophisticated technology, and they are often recognized as one of the major components utilized in the readout chain of detectors in high-energy physics experiments. The Muon Identifier, one of the sub-detector in the ALICE experiment, is taking full advantage of today's FPGAs by changing the way data are processed in its readout chain using a customized user logic firmware. This user logic is written in the VHDL programming language, which is used in ALICE's data acquisition due to its low sample times.

This chapter begins with background information and then delves through the topic at hand. The project's goals are established, and an overview of the strategy used to achieve these goals is provided. The hypothesis, as well as the constraints and key contributions, are listed.

1.1 Background

1.1.1 ALICE experiment

CERN [1] is the world's leading laboratory for scientific research located on the border of Switzerland and France. CERN houses the Large Hadron Collider (LHC) [2] which is about 100 meters below the surface and 27 kilometers in circumference. The LHC produces particle beams i.e. proton-proton, proton-lead, and lead-lead at ultra-relativistic energies to create, amongst others, a highly dense form of matter reminiscent of the early Universe a microsecond after the Big Bang. Spread along the LHC ring are four individual experiments positioned around the four collision points where the beams collide. As shown in Figure 1.1, one of these experiments is A Large Ion Collider Experiment (ALICE) [3].
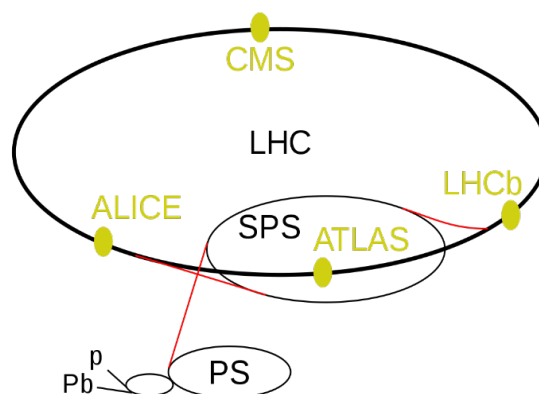
For few millions of seconds after the Big Bang, the universe consisted of a hot soup of elementary particles called quarks and gluons. A few microseconds later, the hot soup of particles known as the Quark-Gluon Plasma (QPG) began cooling to form protons and neutrons, the fundamental of matter. Over the past decades, scientists around the world are trying to re-create QPG by smashing beams of heavy particles together with enough energy to produce a temperature higher than the core center of the Sun. By keeping the temperature and the energy density high enough, scientists can obtain a new phase of matter where quarks and gluons are deconfined QGP. Such conditions can be created in high-energy heavy-ion collisions at the CERN LHC. ALICE is the ~~only~~ detector at the CERN LHC dedicated to the study of this strongly interacting matter, the QGP, and its proprieties.

1.1.2 ALICE Detector

To reconstruct and identify a myriad of particles created in the collisions, the ALICE detector shown in Figure 1.2, is using a set of 19 sub-detectors extended over a length of 26m and 16m in height and width, weighing over 10 000 tons. The sub-detectors provide information about the mass, velocity, and electric charge of the particles. Each sub-detector is designed to study different aspects of the particles created in the collisions.
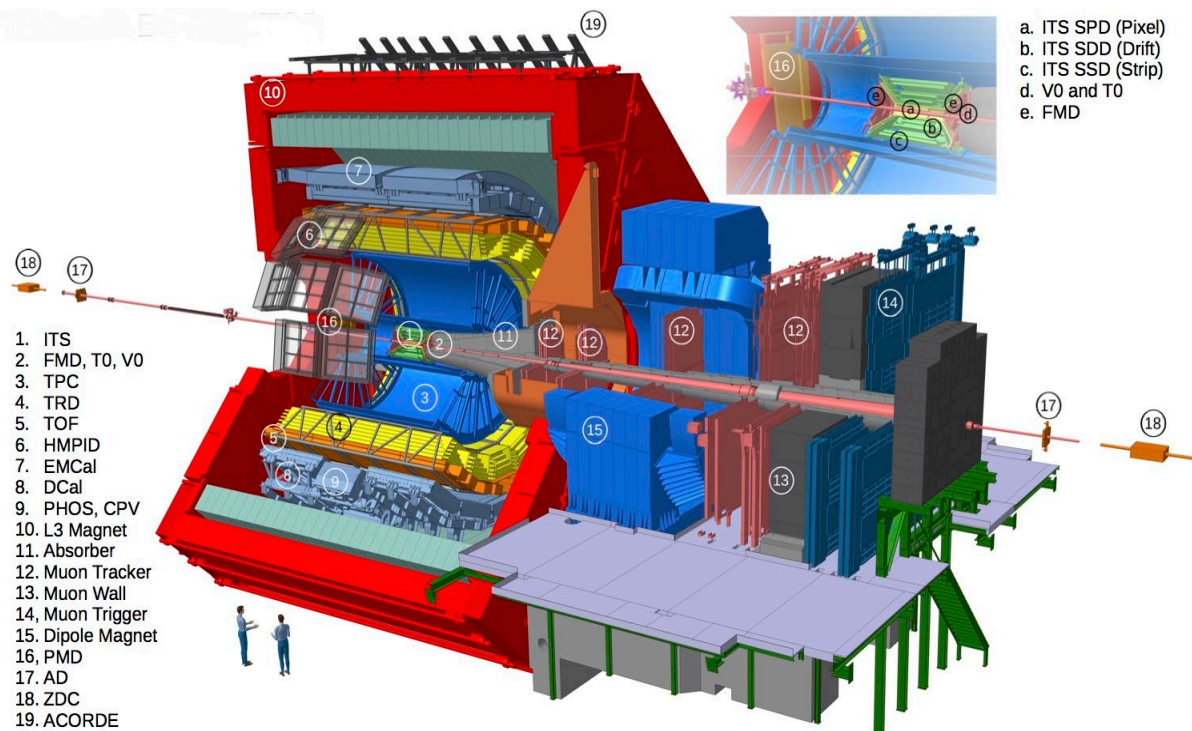

a. ITS SPD (Pixel)
b. ITS SDD (Drift)
c. ITS SSD (Strip)
d. V0 and T0
e. FMD

1. ITS
2. FMD, T0, V0
3. TPC
4. TRD
5. TOF
6. HMPID
7. EMCal
8. DCal
9. PHOS, CPV
10. L3 Magnet
11. Absorber
12. Muon Tracker
13. Muon Wall
14. Muon Trigger
15. Dipole Magnet
16. PMD
17. AD
18. ZDC
19. ACORDE

Figure 1.2: Schematic overview of the ALICE detector with its sub-detectors [5].

The ALICE detector consists of two main regions: the central barrel region and the forward region known as the Muon Spectrometer.

The central barrel is covered by a solenoid L3 magnet providing a field of 0.5 Tesla to the sub-detectors, and it contains the Inner Tracking System (ITS) composed of six layers of silicon detectors: Silicon Pixel Detector (SPD), Silicon Detector Drift (SDD), and Silicon Strip Detector (SSD). The ITS is enveloped by a circular Time Projection Chamber (TPC), three-particle identification arrays of Time of Flight (TOF), a ring imaging of Cherenkov High Momentum Particle Identification Detector (HMPID), and a Transition Radiation Detector (TRD). The surface layer contains the Electromagnetic Calorimeters (EMCal), and the Photon Spectrometer (PHOS). Small-scale sub-detectors used for global event identification and triggering such as the Zero Degree Calorimeter (ZDC), Photon Multiplicity Detector (PMD), Forward Multiplicity Detector (FMD), T0, and V0 are located away from the interaction point. On the three upper faces of the solenoid L3 magnet is A Cosmic Ray Detector (ACORDE). It consists of an array of plastic scintillator counters and together with the muon spectrometer, they provide accurate information about cosmic rays.

The Muon Spectrometer is designed to measure muon production from the decays of quarkonia, low mass vector mesons, heavy-flavor hadrons, and electroweak bosons [6]. The Muon Spectrometer has an angular acceptance of 171˚- 178˚, corresponding to the pseudorapidity region $-4.0 < \eta < -2.5$. The Muon Spectrometer covers a total length of $\simeq 17$ m and it is composed of the following components: front-absorbers to filter all particles except muons coming from the interaction point, a large dipole magnet, a high-resolution Muon Tracking Chambers (MCH), a 120 cm thick iron wall (Muon Filter), and a Muon Trigger (MTR).

The Muon Trigger is the former name given to the Muon Identifier before the upgrades. Further technical details concerning the muon trigger will be described in detail in the next sections as the work described in this thesis is only focused on this specific sub-detector.

1.1.4 Muon Trigger

The muon trigger system is equipped with a configurable threshold to provide trigger signals for selecting events of interest and discarding events with only low momentum muons ($p > 4$ GeV/c). As illustrated in Figure 1.5, the muon trigger is based on 72 single-gaps Resistive Plate Chamber (RPC) detectors, arranged in 2 stations of 2 chambers, each at a distance of about 16 m and 17 m from the interaction point respectively. Each RPC consists of two planes, a positively charged anode, and a negatively charged cathode, both made of very high resistivity plate plastic material and separated by 2 mm of a gas mixture of Ar, CH2F4, C4H10, and SF6. Once a charged particle such as a muon passes through the chamber, electrons are knocked out of the gas atoms. These electrons in turn hit other atoms causing a mass of electrons. The electrodes are transparent to the electrons, which are instead picked up by external metallic strips outside the chamber after a small but precise time delay. The pattern of hit strips gives a quick measure of the muon momentum, which is measured by the front-end electronics, known as A DUaL Threshold (ADULT) cards [7]. The signals from the ADULT cards are then propagated to the readout electronics based on three programmable circuits (local, regional and global) working in sequential mode at 40 MHz, to make immediate decisions about the validity of the data. The ADULT electronics were initially developed for streamer mode operation with a gas mixture for the LHC Run 1 (2010-2012). A few years later, a maxi-avalanche operation mode was introduced for the LHC Run 2 (2015-2018), where the signal amplitude was smaller than the streamer mode, but still compatible with the minimum threshold of 7 mV (voltage required to create a conducting a path between the RPC and the ADULT) set in the ADULT cards. The sub-detector planes are mounted on a mechanical frame that can be moved to allow access to the chambers for maintenance purposes.
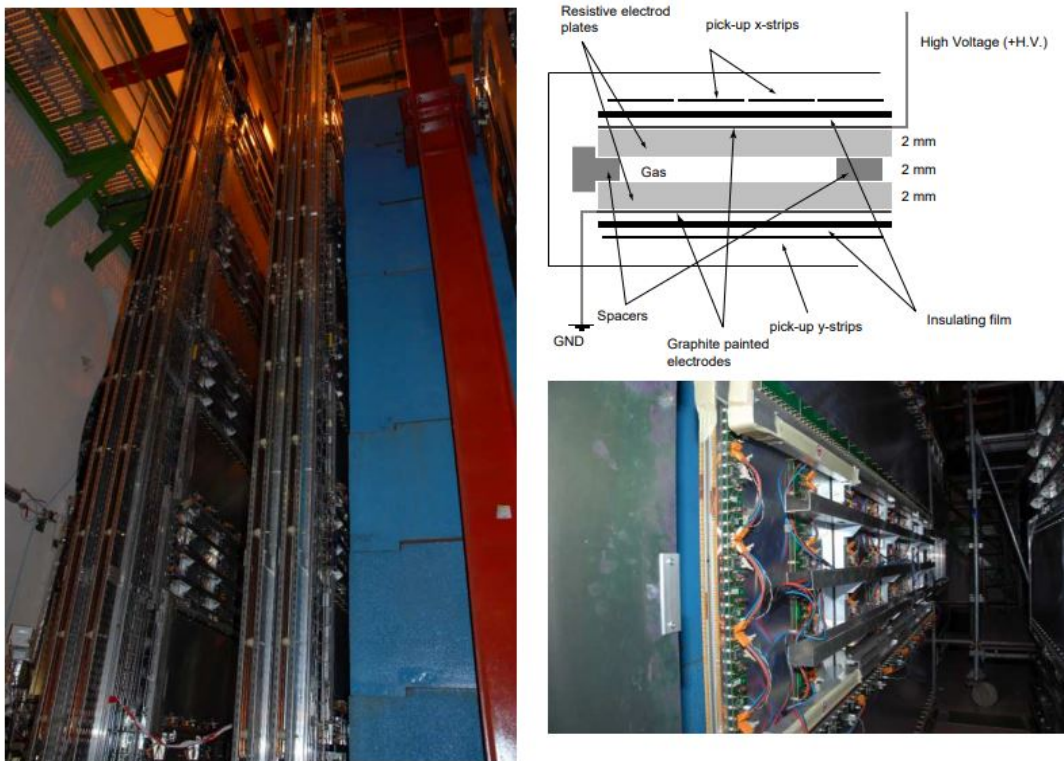
Figure 1.5: Left: View of the two trigger stations as they are positioned behind the muon filter. Right-top: schematic view of the cross-section of the RPC. Right-bottom: an independent RPC module with ADULT electronics [ ]

1.2 LHC Run 3

Based on data collected in Run 1 and 2 (~10 petabytes of raw data) [ ], ALICE is the leading heavy-ion experiment in the world and is quickly expanding the knowledge gathered in previous experiments all over the world. The LHC is currently going through three years of a planned second Long Shutdown called (LS2) which started at the end of 2018 to prepare for Run 3. In line with the LHC upgrade, the ALICE detector is undergoing a major upgrade. The upgrade addresses the challenge of reading out Lead–Lead collisions at the rate of 50 kHz, proton-proton, and proton–Lead at 200 kHz and higher. This will result in the inspection of a data volume of heavy-ion events collected during previous Runs. At the center of the ALICE upgrade strategy is a high-speed readout approach based on a Common Readout Unit (CRU). The CRU has been developed for detector data readout, concentration, reconstruction, multiplexing, and data decoding onto the online-offline (O²) computing system.

The LHC Run 3 was planned to start in the middle of 2021 onwards but has been postponed to March 2022 due to the global pandemic [8]. The peak luminosity of 6×10 cm² per second. Many of the proposed physics observables require a shift in the data-taking strategy, moving away from triggering a small subset of events to online processing and recording of all collisions delivered by the LHC. To achieve these goals, the ALICE detector is being upgraded in such a way that all interactions will be inspected with precision. The upgrade entails the replacement of some sub-detectors with new ones, exploring new technologies while most others including the muon trigger, are moving to new front-end electronics and readout systems.

1.2.1 The upgrade: Muon Trigger to Muon Identifier

For the past 10 years since the beginning of the LHC Run 1, the selection of single muon and di-muon events with a maximum trigger rate of 1 kHz has been provided by the Muon Trigger, however, to cope with the increased luminosity of the LHC during Run 3, this current trigger strategy is no longer sufficient. The upgrade trigger strategy [] does not require a muon trigger, since all events of interest will be read out upon the interaction trigger before online selections. For this reason as part of the upgrade, the existing MTR sub-detector will only play the role of providing the muon identification, hence it has been renamed to the MID.

1.3 Problem statement

Several issues arose during the transition of MTR to MID. These issues [9] were observed throughout a preliminary series of tests conducted on the MID readout chain at Subatech, Nantes (where the readout electronics is developed). The upgraded system showed limitations when running without data pre-analysis performed at the CRU firmware level. Among these limitations are large data rate, desynchronization of data, lack of hardware resources and, many other minor issues related to the data format transmitted to the O² computing system.

1.3.1 Large data rate

In the triggerless readout chain, all events are read out continuously. This results in a bandwidth of 3.2 Gbps generated by each data link of the chain. This large amount of data is a problem for the O² computing facility to conduct data processing concurrently without data compression at the CRU firmware level. The readout electronics data links are based on an 80-bit frame transmitted continuously at 40 MHz (25 ns), which corresponds to the LHC bunch crossing interval. The bunch crossing interval is the period between bunches of particles crossing each other in the LHC. In other words, it is the amount of time between potential collisions.

On the other hand, as previously mentioned, one of the primary goals of the ALICE sub-detectors upgrade is to read out lead-lead collisions at 50 kHz (20 μs), proton-proton, and proton-lead collisions at 200 kHz (5 μs). This indicates that out of 3.2 Gbps, just 4 Mbps during lead-lead collisions and 16 Mbps during proton-proton and proton-lead collisions are worth analyzing and might turn out to be valuable collision data. The remaining data is meaningless and must be suppressed. Holding these data in the memory results in inefficiency and waste of memory.

1.3.2 Desynchronization of data

The data obtained from all readout electronics occur simultaneously, at fixed periods, and is transmitted to the CRU over a wide spectrum of optical links. However, differing transmission delays result in the data from the various links losing synchronization when transmitted to the O² computing system and causes more problems further along the chain at the synchronous reconstruction level [].

1.3.3 Lack of hardware resources

The O² computing system is capable of handling the data rate from a single regional crate at the expense of 2 core processors. Attempting to use 1 core to decode a single regional crate leads to irreversible data loss. Hence, it takes 2 core processors to decode a single regional crate. However, the computer used in the readout chain contains 20 core processors [ ]. To decode data from the entire readout chain, that the computer would need 32 core processors, not to mention any additional cores required to perform further processing of the decoded data. As a result, processing data from the complete front-end system is unfeasible on a single machine. The architecture of the MID readout chain is described later in Chapter 2.

1.4 Research aim

The ALICE collaborators participating in the MID project are searching for new ways to process data. Many alternatives have been suggested, but most of them entail significant improvements in the existing readout chain and manpower such as changing the algorithm implemented in the O² processing to cope with the large data rate, acquiring additional CRUs, and core processor computers to process data from the entire readout electronics. A thorough analysis review revealed that the most efficient and cost-effective solution is to take advantage of the existing high-speed FPGA incorporated in the CRU by designing a customized user logic firmware to meet the requirements of the readout chain.

The user logic is a specific sub-detector component, that can be implemented into the CRU firmware through a specific compilation [ ]. It is developed by the sub-detector teams and can perform low-level data processing and other additional features before forwarding it to the O² computing facility for further analysis. This research aims to improve the way data are processed in the MID readout chain using a customized user logic firmware before the start of the LHC Run 3.

1.5 Objectives

The research aim stated above is achieved through the following objectives:

- Review and analyze different components of the readout chain
- Select the best user logic algorithm
- Identify and subsequently remove meaningless data
- Receive timing and trigger information
- Synchronize essential data before performing the correct analysis
- Reformat data transmitted from the readout electronics
- Transmit data in the order required by the O² computing facility
- Handle errors identified in the readout electronics data
- Successfully validate the user logic simulation tests
- Successfully validate the user logic hardware tests
- Make recommendations for future improvements

1.6 Hypothesis

There is a possibility of designing and developing a stable and reliable user logic firmware that can improve the way data is processed in the MID readout chain. This can be achieved by developing an algorithm based on systems requirements. However, the difference in protocol between various systems of the readout chain makes it complex and can be time-consuming. The main question to be considered is whether a user logic prototype can be designed and tested to meet the requirements of the MID readout chain on time before the start of the commissioning phase of the MID-sub-detector, and whether or not this prototype can be used to develop a realistic user logic capable of processing data from the entire readout chain, considering hardware and software restrictions of the approved FPGA.

1.7 Delineation

The thesis is limited to the design and development of the user logic firmware prototype capable of pre-analyzing data from 2 regional links of the MID readout chain. This research analyses in detail different systems used in the readout chain and improves the way data are processed in the CRU. The proposed scheme is developed after intensive research and a good understanding of the ALICE detector. Hence, the incorporation of the user logic component into the existing CRU firmware is done through conformance with established requirements and practice. Additionally, important technical decisions such as hardware, communication protocols, design tools, programming languages, and most relevant resource usage limit of the research in question were long established before the beginning of the research.

1.8 Collaboration and main contributions

In South Africa, the National Research Foundation (NRF) iThemba Laboratory for Accelerators Based-Science (LABS) is part of the ALICE Collaboration and contributes to the ALICE Muon Spectrometer upgrade, in particular the MID. In collaboration with the Cape Peninsula University of Technology (CPUT) and the University of Cape Town (UCT), NRF iThemba LABS is responsible for conducting research and developing the CRU user logic firmware for the MID readout chain, including setting up a testbench data acquisition readout chain and the maintenance thereof.

The user logic project started in early 2018, with early research conducted by Nathan Boyles, a former master's student from the Electrical Engineering department at UCT. In early 2019, Mr. Boyles delivered an early proof of concept of the user logic, which was completely discarded and identified as outdated by MID experts due to the rapid development of the ALICE CRU software and firmware projects. In mid-2019, I took over the responsibility of design, development, and prototype of user logic based on realistic data acquisition requirements and availability of relevant readout components. Together with Dr. C.Renard (expert in the readout electronics at Subatech in Nantes, France), the requirements to process data from 2 data links of the readout chain were established. To keep track of the rapid development of the CRU software and firmware, rigorous consultations and discussions took place scheduled with Dr. F.Costa (ALICE CRU software expert at CERN) and Dr. O.Bourrion (ALICE CRU firmware developer at the University of Grenoble, France). For what concerns the MID O^2 requirements, Dr. D.Stocco (MID O^2 expert at Subatech, France) was the main source of contact. His input was required since the outcome of this research may affect the way data will be handled at

the next phase of the data acquisition. As such, he was instrumental in setting up some additional requirements and constraints to facilitate the readability of the user logic output data.

 Overall, the design and development of the ALICE CRU user logic firmware prototype for the MID readout chain are provided by the Electrical Engineering department at CPUT with support from various collaborators using facilities provided by the NRF iThemba LABS and advanced technology.

1.9 Methodology

The research methods that are utilized for the development of this thesis are:

- **Literature review:** since in many cases the written literature is not available on the readout chain. Therefore, the information was gathered by reading technical specification papers, IEEE published journals, conferences, interviewing specialist engineers in the data acquisition chain, and through the World Wide Web.

- **Prototyping**: Intel Quartus Pro 18.1 is the main software environment recommended and used to design and develop the user logic. For this thesis, two different prototyping approaches are implemented. The rapid throwaway method involves exploring ideas by quickly developing a prototype based on preliminary requirements which are then revised through simulation test feedback. Once validated, the evolutionary approach is then introduced. This method uses a continuous, working prototype that is refined after each iteration of hardware test feedback.

- **Simulation tests:** ModelSim is the simulation software used to verify the functionality of the user logic algorithm by analyzing each component of the model. A more advanced simulation is performed by merging the CRU firmware simulation files as well as the MID readout electronics firmware simulation files into a single testbench for more efficient and accurate results.

- **Hardware tests**: a readout testbench facility available at iThemba LABS is developed for practical work. Expected tests for conformance include testing of the user logic prototype using a fully-functional MID readout testbench set-up capable of emulating the same events generated by the main ALICE MID detector readout chain at CERN.

- **Data collection:** simulation and hardware tests are conducted to collect real data coming in and out of the user logic firmware. A comparison between the input and output data is done to achieve an effective assessment of the user logic algorithm.

1.10 Thesis outline

Chapter 2

This chapter looks deeper into the MID readout chain and its most important components and protocols, particularly the CRU, which will serve as the interface between the on-detector electronics and the O² computing system.

Chapter 3

This chapter explains in detailed the CRU firmware. It also describes the busbar protection schemes that are currently in use and operation. The theory of overcurrent protection devices is also explained. The digital busbar protection schemes are also covered.

Chapter 4

tests the performance of the prototype of the conceptual design previously presented in relevant fields of metric for a project of this nature.

Chapter 5

The results obtained, the performance of the prototype, the key findings, and the thesis deliverables are summarized in this chapter. The recommendations for possible future work and the extension of the project are also discussed in this chapter.

Chapter 6

This thesis is concluded by a comparison of the project's defined goals and the results of the user logic prototype. Additionally, it addresses, the remaining work that needs to be completed. This includes features that are yet to be developed as well as potential recommendations.

Appendix A

This Appendix describes the software tool package used for IED configuration and all ABB 670 series function blocks that were used to build the reverse blocking protection scheme. These blocks are described in different categories which are based on their functions.

Appendix B

This Appendix describes the software tool package used for IED configuration and all ABB 670 series function blocks that were used to build the reverse blocking protection scheme. These blocks are described in different categories which are based on their functions.

Appendix C

This Appendix describes the software tool package used for IED configuration and all ABB 670 series function blocks that were used to build the reverse blocking protection scheme. These blocks are described in different categories which are based on their functions.

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