# Abstract

A Large Ion Collider Experiment (ALICE) at the Large Hadron Collider (LHC) at CERN is undergoing a major upgrade during which some of its sub-detectors are replaced with new ones and while others are equipped with new electronics to handle the expected higher lead-lead, proton-lead as well as proton-proton collision rates in the next running period (Run 3) foreseen to start in 2022. The upgrade requires, in part, new sub-detectors for the central system while other existing sub-detectors including those belonging to the Muon Spectrometer such as the Muon Trigger (MTR) which have been renamed to Muon Identifier (MID), will operate in continuous, trigger-less readout modes. At the center of the upgrade is a new approach based on the Common Readout Unit (CRU) developed to meet ALICE requirements. In particular, to share common interfaces, between 3 main sub-systems: the front-end electronics (FEE), the Online-Offline (O²) computing system, and the timing and trigger system (TTS).

Due to the increase in data quantity, as well as the high collision and acquisition rates, typical methodologies are impossible to employ without massive efforts to expand processing capacity. Since the required scaling of the O² computing system can not keep up with the MID increased data flow, a new acquisition and processing paradigm has to be established. The CRU is a PCI Express 3rd generation FPGA processor board with a specific sub-detector feature called user logic. This user logic is a customizable component that can be used to extend the capabilities of the CRU firmware by providing additional features such as zero suppression, synchronization, and so on to meet the needs of any sub-detector in the ALICE experiment.

This research project provides a new approach to process the MID data based on a user logic prototype. The key aims of this thesis are to plan, build, evaluate and validate the user logic component. Innovative methods have been used to reduce the bandwidth produced by the sub-detector readout electronics, as well as adaptations to facilitate data handling later in the processing chain. Research procedures, simulations, evaluation methods, and applied methods are used to build a consistent prototype design. A laboratory testbench at NRF iThemba LABs equipped with the MID readout chain is used to test and validate the user logic prototype. The research findings and deliverables of this thesis will be used for postgraduate studies of other students, research, as well as a preliminary solution for a more complex user logic firmware.

# Acronyms

ACORDE - A Cosmic Ray Detector

ADC - Analog-Digital Converter

ADULT - A DUaL Threshold

ALICE - A Large Ion Collider Experiment

ATLAS - A Toroidal LHC ApparatuS

CRU - Common Readout Unit

EMCal - Electromagnetic Calorimeters

FMD - Forward Multiplicity Detector

HMPID - High Momentum Particle Identification Detector

ITS - Inner Tracking System

LHC - Large Hadron Collider

LHCb - Large Hadron Collider beauty

LS2 - Long Shutdown 2

MCH - Muon Chamber

MID - Muon Identifier

MTR - Muon Trigger

NRF - National Research Foundation

LABS - Laboratory for Accelerator-Based Science

FPGA - Field Programmable Gate Array

O² - Online Offline

PHOS - Photon Spectrometer

PMD - Photon Multiplicity Detector

QGP - Quark-Gluon Plasma

SDD - Silicon Drift Detector

SPD - Silicon Pixel Detector

SSD - Silicon Strip Detector

TOF - Time Of Flight

TRD - Transition Radiation Detector

VHDL - VHSIC Hardware Description Language

ZDC - Zero Degree Calorimeter

**Chapter 1**

# Introduction

Since the early days of its first employment in the 1960s, the distinctive qualities of Field Programmable Gate Arrays (FPGAs) [1] such as integration, flexibility, low power, and high bandwidth communication have allowed various new and critical approaches. FPGAs are the result of multiple generations of sophisticated technology, and they are often recognized as one of the major components utilized in the data acquisition of the detectors in high-energy physics experiments.

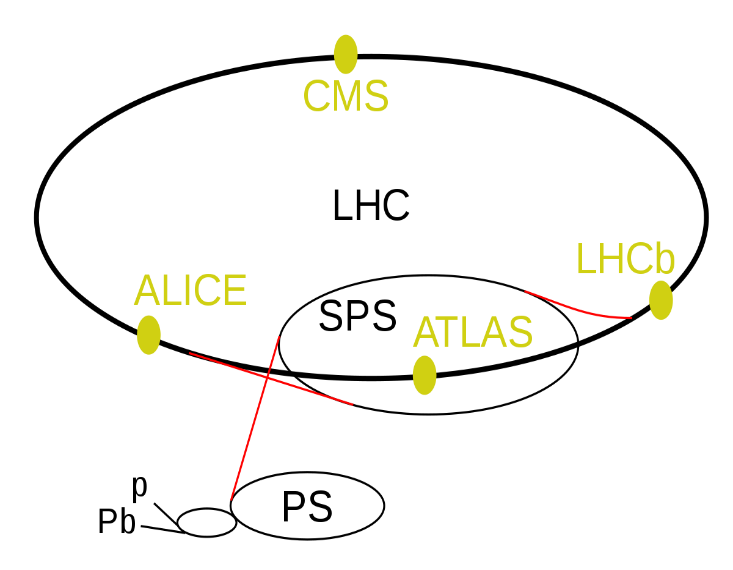
The ALICE detector at the Large Hadron Collider (LHC) at the European Organization for Nuclear Research (CERN) is undergoing a major upgrade during which some of its sub-detectors are replaced with new ones and while others are equipped with new electronics to cope with higher collision rates planned for the following years. The Muon Identifier (MID), one of the new sub-detector in ALICE is taking full advantage of today's FPGAs by changing the way data are processed in its readout chain using a customized user logic firmware. This user logic is written in the VHDL programming language and can implement multiple features tailored to the specific of the sub-detector.

This chapter begins with background information on the experiment and then introduces the ALICE detector. The project's goals are established, and an overview of the strategy used to achieve these goals is provided. The hypothesis, as well as the constraints and key contributions, are listed.

## 1.1 Background

### ALICE experiment

CERN [2] is the world’s leading laboratory for nuclear and particle physics research located on the border of Switzerland and France. CERN houses the LHC [3] which is about 100 meters below the surface and 27 kilometers in circumference. The LHC produces particle beams i.e. proton-proton (p-p), proton-lead (p-Pb), and lead-lead (Pb-Pb) at ultra-relativistic energies to create and study the characteristics of a highly dense form of matter reminiscent of the early Universe a microsecond after the Big Bang [4]. Spread along the LHC ring are four individual experiments positioned around the four collision points where the beams collide. As shown in Figure 1.1, one of these experiments is ALICE.



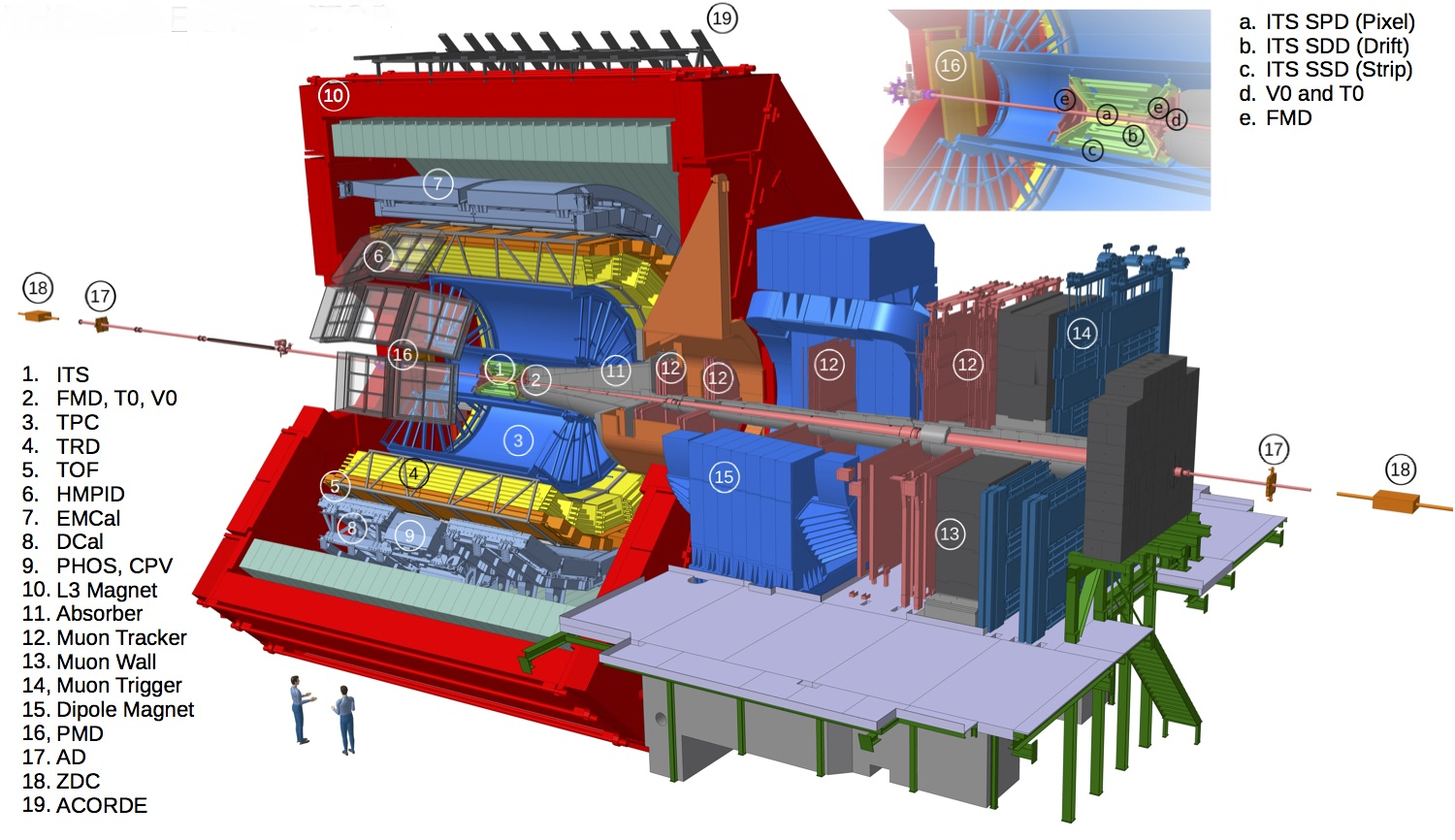
**Figure 1.1:** LHC ring with its four main experiments, ALICE, ATLAS, LHCb, and CMS as well as its super proton synchrotron (SPS), proton synchrotron (PS), and proton and lead accelerators [5].

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For a few millionths a second after the Big Bang, the universe consisted of a hot plasma of deconfined elementary particles called quarks and gluons. A few microseconds later, this hot plasma known as the quark-gluon plasma (QGP) cooled further down to form hadrons, amongst others protons and neutrons, the fundamental building blocks of atomic matter. The conditions of the QGP can be created in high-energy heavy-ion collisions at the CERN LHC. ALICE is the detector at the CERN LHC dedicated to the study of this strongly interacting matter, the QGP, and its properties after recording data in pp and p-Pb collisions.

### ALICE Detector

To reconstruct and identify a myriad of particles created in these collisions, the ALICE detector is shown in Figure 1.2, is using a set of 19 sub-detectors extended over a length of 26 m and 16 m in height and width, weighing over 10 000 tons. The sub-detectors encapsulated in a toroid magnet (L3) provide information about the mass, velocity, and electric charge of the particles. Each sub-detector is designed to study different aspects of the particles created in the collisions.



**Figure 1.2:** Schematic overview of the ALICE detector with its sub-detectors used during Run 2 [6].

The ALICE detector consists of two main regions: the central barrel region and the forward region known as the Muon Spectrometer.

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The central barrel detectors are surrounded by a solenoid L3 magnet providing a field of 0.5 Tesla. At the center of the central barrel and closest to the beamline is the Inner Tracking System (ITS) composed of six layers of silicon detectors: Silicon Pixel Detector (SPD), Silicon Drift Detector (SDD), and Silicon Strip Detector (SSD). The ITS is encompassed by a cylindrical Time Projection Chamber (TPC), three-particle identification arrays of Time of Flight (TOF), a ring imaging of Cherenkov High Momentum Particle Identification Detector (HMPID), and a Transition Radiation Detector (TRD). The surface layer contains the Electromagnetic Calorimeters (EMCal), and the Photon Spectrometer (PHOS). Small-scale sub-detectors used for global event identification and triggering such as the Zero Degree Calorimeter (ZDC), Photon Multiplicity Detector (PMD), Forward Multiplicity Detector (FMD), T0, and V0 are located on either side of the interaction point. On the three upper outside faces of the solenoid L3 magnet is A Cosmic Ray Detector (ACORDE). It consists of an array of plastic scintillator counters and provides accurate information about cosmic ray events.

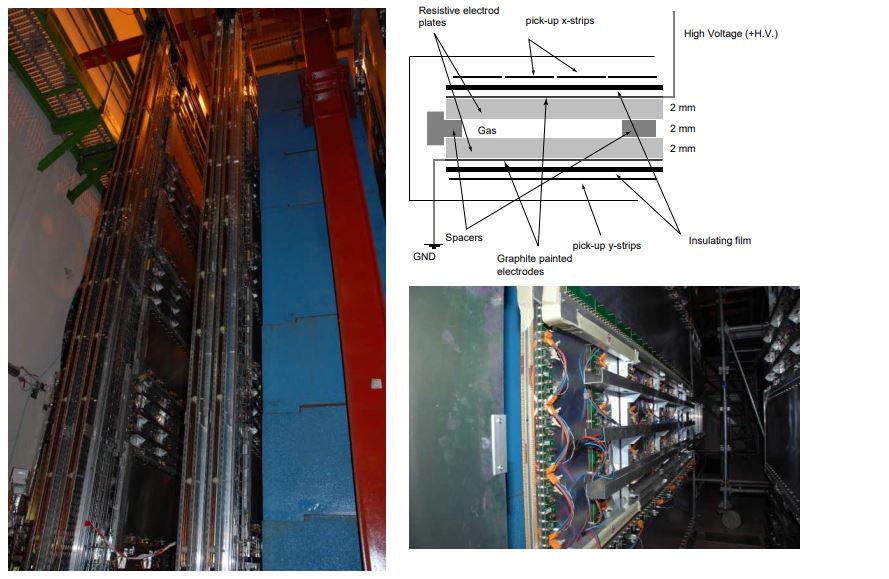
The Muon Spectrometer is designed to measure muon production from the decays of quarkonia, low mass vector mesons, heavy-flavor hadrons, and electroweak bosons [7]. The Muon Spectrometer has an angular acceptance of 171˚- 178˚, corresponding to the pseudorapidity region −4.0 < η < −2.5. The Muon Spectrometer covers a total length of ≃ 17 m and it is composed of the following components: front-absorbers to filter all particles except muons coming from the interaction point, a large dipole magnet, high-resolution Muon Tracking Chambers (MCH), a 120 cm thick iron wall (Muon Filter), and a Muon Trigger (MTR).

### 1.1.4 Muon Trigger

The MTR system is equipped with a configurable threshold to provide trigger signals for selecting events of interest and discarding events with only low momentum muons (*p*<4 GeV/*c*). As illustrated in Figure 1.5, the muon trigger is based on 72 single-gaps Resistive Plate Chamber (RPC) detectors, arranged in 2 stations of 2 chambers, each at a distance of about 16 m and 17 m from the interaction point, respectively. Each RPC consists of two planes, a positively charged anode, and a negatively charged cathode, both made of very high resistivity plate plastic material and separated by 2 mm of a gas mixture of Ar, CH2F4, C4H10, and SF6. Once a charged particle such as a muon passes through the chamber, it knocks electrons out of the gas atoms. These electrons in turn hit other atoms causing an avalanche of electrons. Since the electrodes are transparent to the electrons, these are instead picked up by external metallic strips after a small but precise time delay. The combination of hit strips firing gives a quick measure of the muon momentum, which are read-out by the front-end electronics, known as A DUaL Threshold (ADULT) cards [8]. The signals from the ADULT cards are then propagated to the readout electronics based on three programmable circuits (local, regional and global) working in sequential mode at 40 MHz, to make immediate decisions about the validity of the data. The ADULT electronics were initially developed for streamer mode operation with a gas mixture for the LHC Run 1 (2010-2012). A few years later, a maxi-avalanche operation mode was introduced for the LHC Run 2 (2015-2018), where the signal amplitude was smaller than in the streamer mode, but still compatible with the minimum threshold of 7 mV set in the ADULT cards. The sub-detector planes are mounted on a mechanical frame on rail support that can be moved to allow access to the chambers for maintenance purposes.

The Muon Trigger will be called Muon Identifier (MID) after the upgrade for Run 3. Technical details concerning the new MID readout chain are described in chapter 2, as the work described in this thesis is solely focused on this specific sub-detector.

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**Figure 1.5:** Left: View of the two trigger stations positioned behind the muon filter. Right-top: schematic view of the cross-section of the RPC. Right-bottom: an independent RPC module with ADULT electronics

## 1.2 LHC Run 3

Based on data collected in Run 1 and 2 (~10 petabytes of raw data), ALICE is the leading heavy-ion experiment in the world and is quickly expanding the knowledge gathered in previous experiments all over the world. The LHC is currently going through three years of a planned second Long Shutdown called (LS2) which started at the end of 2018 to prepare for Run 3. In line with the LHC upgrade, the ALICE detector is undergoing a major upgrade. This upgrade addresses the challenge of reading out lead-lead collisions at the rate of 50 kHz, proton-proton, and proton-lead at 200 kHz and higher. At the center of the ALICE’s upgrade strategy is a high-speed readout approach based on a Common Readout Unit (CRU). The CRU has been developed for detector data readout, concentration, reconstruction, multiplexing, and data decoding onto the online-offline (O²) computing system.

Many of the proposed physics observables require a change in the data-taking strategy, moving away from triggering a small subset of events to continuous online processing and recording of all events. To achieve these goals, the ALICE detector is being upgraded in such a way that all interactions will be scrutinized with precision. The upgrade entails the replacement of some sub-detectors with new ones, making use of new technologies while most others are equipping their detectors with new electronic systems.

The LHC Run 3 was planned to start in the middle of 2021 onwards but has been postponed to March 2022 due to the global pandemic [9].

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### 1.2.1 The upgrade: Muon Trigger to Muon Identifier

For the past 10 years since the beginning of the LHC Run 1, the selection of single muon and di-muon events with a maximum trigger rate of 1 kHz was provided by the MTR. However, to cope with the increased luminosity of the LHC during Run 3, this current trigger strategy is no longer sufficient. The upgrade trigger strategy described in [10] does not require a muon trigger, since all events of interest will be read out upon the interaction trigger before online selections. For this reason, as part of the upgrade, the new MID will play the role of providing the muon identification.

## 1.3 Problem statement

Several issues concerning the readout arose during the transition from MTR to MID. These issues [11] were observed throughout a preliminary series of tests conducted on the MID readout chain at Subatech, Nantes in France (where the readout electronics are developed). The upgraded system showed limitations when running without data pre-analysis performed at the CRU firmware level. Among these limitations are large data rate, desynchronization of data, lack of hardware resources and, many other minor issues related to the data format transmitted to the O² computing system. All these limitations had to be addressed urgently.

### 1.3.1 Large data rate

In the triggerless readout chain, all events are read out continuously. This results in a bandwidth of 3.2 Gbps generated by each data link of the chain. This large amount of data is a problem for the O² computing facility to conduct data processing concurrently without data compression already at the CRU firmware level. The readout electronics data links are based on an 80-bit frame transmitted continuously at 40 MHz (25 ns), which corresponds to the LHC bunch crossing interval. The bunch crossing interval is the period between bunches of particles crossing each other in the LHC. In other words, it is the amount of time between colliding bunches.

On the other hand, as previously mentioned, one of the primary goals of the ALICE detector upgrade is to read out lead-lead collisions at 50 kHz (20 µs), proton-proton, and proton-lead collisions at 200 kHz (5 µs). This indicates that out of 3.2 Gbps, just 4 Mbps during lead-lead collisions and 16 Mbps during proton-proton and proton-lead collisions are worth analyzing and might turn out to be valuable collision data. The remaining data are meaningless and must be suppressed. Retaining these data in the memory results in inefficiency and waste of memory.

### 1.3.2 Desynchronization of data

The data obtained from all readout electronics occur simultaneously, at fixed periods, and are transmitted to the CRU over a wide set of optical links. However, differing transmission delays result in the data from the various links losing synchronization when transmitted to the O² computing system. Therefore, cause more problems further along the chain at the synchronous and reconstruction levels.

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### 1.3.3 Lack of hardware resources

The O² computing system is capable of handling the data rate from a single regional crate at the expense of 2 core processors. Attempting to use 1 core to decode a single regional crate leads to irreversible data loss. Hence, it takes 2 core processors to decode a single regional crate. However, the computer [12] used in the readout chain contains 20 core processors. To decode data from the entire readout chain, that the computer would need 32 core processors, not to mention any additional cores required to perform further processing of the decoded data. As a result, processing data from the complete front-end system is unfeasible on a single machine. The architecture of the MID readout chain is described in Chapter 2.

## 1.4 Research aim

The ALICE collaborators participating in the MID project are searching for new ways to process raw data. Many alternatives have been suggested, but most of them entail significant improvements in the existing readout chain. Some of the improvements require changing the algorithm implemented in the O² processing to cope with the large data rate, acquiring additional CRUs, and core processor computers to process data from the entire readout electronics. A thorough analysis review revealed that the most efficient and cost-effective solution is to take advantage of the existing high-speed FPGA incorporated in the CRU by designing a customized user logic firmware to meet the requirements of the readout chain.

The user logic is a specific sub-detector component, that can be implemented in the CRU firmware through a specific compilation. It is developed by the sub-detector teams and can perform low-level data processing and other additional features before forwarding data to the O² computing facility for further analysis. This research aims to improve the way data are processed in the MID readout chain using a customized user logic firmware before the start of the LHC Run 3.

## 1.5 Objectives

The research aim stated above is achieved through the following objectives:

* Review and analyze different components of the readout chain
* Select the best user logic algorithm
* Identify and subsequently remove meaningless data
* Receive timing and trigger information
* Synchronize essential data before performing the correct analysis
* Reformat data transmitted from the readout electronics
* Transmit data in the order required by the O² computing facility
* Handle errors identified in the readout electronics data
* Successfully validate the user logic simulation tests
* Successfully validate the user logic hardware tests
* Make recommendations for future improvements

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## 1.6 Hypothesis

This study offers the possibility of designing and developing a stable and reliable user logic firmware that can improve the way data are processed in the MID readout chain. This can be achieved by developing an algorithm based on systems requirements. However, the difference in protocol between various systems of the readout chain makes it complex and can be time-consuming. The main questions to be considered are whether a user logic prototype can be designed and tested to meet the requirements of the MID readout chain on time before the start of the commissioning phase of the MID-sub-detector, and whether or not this prototype can be used to develop a realistic user logic capable of processing data from the entire readout chain, considering hardware and software restrictions of the approved FPGA.

## 1.7 Delineation

This thesis is limited to the design and development of the user logic firmware prototype capable of pre-analyzing data from 2 regional links of the MID readout chain. This research analyses in detail different systems used in the readout chain and improves the way data are processed in the CRU. The proposed scheme is developed after intensive research and a good understanding of the ALICE detector. Hence, the incorporation of the user logic component into the existing CRU firmware is done through conformance with established requirements and practice. Additionally, important technical decisions such as hardware, communication protocols, design tools, programming languages, and most relevant resource usage limit of the research in question have been established before the beginning of the research.

## 1.8 Collaboration and main contributions

In South Africa, the National Research Foundation (NRF) iThemba Laboratory for Accelerators Based-Science (LABS) is part of the ALICE Collaboration and contributes to the ALICE Muon Spectrometer upgrade, in particular the MID. In collaboration with the Cape Peninsula University of Technology (CPUT) and the University of Cape Town (UCT), NRF iThemba LABS is responsible for conducting research and developing the CRU user logic firmware for the MID readout chain, including setting up a testbench data acquisition readout chain and the maintenance thereof.

The user logic project started in early 2018, with early research described in this paper [13]. Due to the rapid evolution of the ALICE CRU software and firmware projects, a complete modification to the initial project was necessary. In 2020, a new design and development of the user logic based on realistic data acquisition requirements and availability of relevant readout components led to this study. Together with Dr. C.Renard (expert in the readout electronics at Subatech in Nantes, France), the requirements to process data from 2 data links of the readout chain were established. To keep track of the rapid evolution of the CRU software and firmware, rigorous consultations and discussions took place with Dr. F.Costa (ALICE CRU software expert at CERN) and Dr. O.Bourrion (ALICE CRU firmware developer at the University of Grenoble, France). For what concerns the MID O² requirements, Dr. D.Stocco (MID O² expert at Subatech, France) was the main contact and source of information. His input was required since the outcome of this research may affect the way data will be handled at the next phase of the data acquisition chain. As such, he was instrumental in setting up some additional requirements and constraints to facilitate the readability of the user logic output data.

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Overall, the design and development of the ALICE CRU user logic firmware prototype for the MID readout chain are provided by the Electrical Engineering department at CPUT with support from various collaborators using facilities provided by the NRF iThemba LABS and advanced technology.

## 1.9 Methodology

The research methods that are utilized for the development of this thesis are:

* **Literature review:** since in many cases the written literature is not available on the readout chain. The information was gathered by reading technical specification papers, IEEE published journals, conferences, interviewing specialist engineers in the data acquisition chain, and through the World Wide Web.
* **Prototyping**: Intel Quartus Pro 18.1 [14] is the main software environment recommended and used to design and develop the user logic. For this thesis, two different prototyping approaches are implemented. The rapid throwaway method involves exploring ideas by quickly developing a prototype based on preliminary requirements which are then revised through simulation test feedback. Once validated, the evolutionary approach is then introduced. This method uses a continuous, working prototype that is refined after each iteration of hardware test feedback.
* **Simulation tests:** ModelSim [15] is the simulation software used to verify the functionality of the user logic algorithm by analyzing each component of the model. A more advanced simulation is performed by merging the CRU firmware simulation files as well as the MID readout electronics firmware simulation files into a single testbench for more efficient and accurate results.
* **Hardware tests**: a readout testbench facility available at iThemba LABS is developed for practical work. Expected tests for conformance include testing of the user logic prototype using a fully-functional MID readout testbench set-up capable of emulating the same events generated by the main ALICE MID detector readout chain at CERN.
* **Data collection:** simulation and hardware tests are conducted to collect real data coming in and out of the user logic firmware. A comparison between the input and output data is done to achieve an effective assessment of the user logic algorithm.

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## 1.10 Thesis outline

**Chapter 2**

This chapter looks deeper into the MID readout chain and its most important components and protocols, particularly the CRU, which will serve as the interface between the on-detector electronics and the O² computing system.

**Chapter 3**

This chapter explains in detailed the CRU firmware. It also describes the busbar protection schemes that are currently in use and operation. The theory of overcurrent protection devices is also explained. The digital busbar protection schemes are also covered.

**Chapter 4**

tests the performance of the prototype of the conceptual design previously presented in relevant fields of metric for a project of this nature.

**Chapter 5**

The results obtained, the performance of the prototype, the key findings, and the thesis deliverables are summarized in this chapter. The recommendations for possible future work and the extension of the project are also discussed in this chapter.

**Chapter 6**

This thesis is concluded by a comparison of the project's defined goals and the results of the user logic prototype. Additionally, it addresses, the remaining work that needs to be completed. This includes features that are yet to be developed as well as potential recommendations.

**Appendix A**

This Appendix describes the software tool package used for IED configuration and all ABB 670 series function blocks that were used to build the reverse blocking protection scheme. These blocks are described in different categories which are based on their functions.

**Appendix B**

This Appendix describes the software tool package used for IED configuration and all ABB 670 series function blocks that were used to build the reverse blocking protection scheme. These blocks are described in different categories which are based on their functions.

**Appendix C**

This Appendix describes the software tool package used for IED configuration and all ABB 670 series function blocks that were used to build the reverse blocking protection scheme. These blocks are described in different categories which are based on their functions.

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