**Chapter 2**

# Muon identifier

We have devices with lower power, more accurate and efficient ADCs, and faster digital electronics. This section reviews the existing electronics and presents the design requirements for the new system.

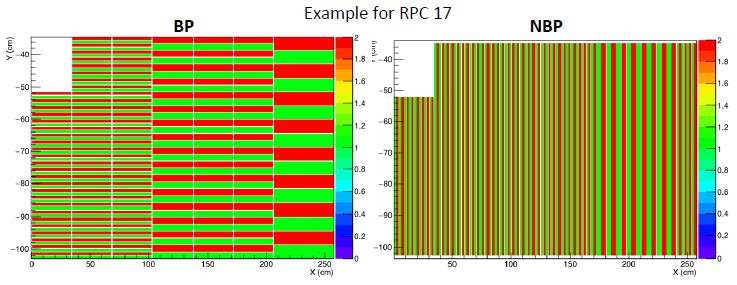
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| 2 | Readout chain |

## 2.1 Overview

The transition from MTR to MID during the LS2 entails, the replacement of the RPC ADULT electronics by a new ASICS named the Front-End Electronics Rapid Integrated Circuit (FEERIC) [ ]. Unlike ADULT, FEERIC amplifies the analog signals from the RPCs. The RPCs will be operated in avalanche mode resulting in a substantial reduction of the charge produced in the gas and thus limiting aging effects. Furthermore, to cope with the given readout rates, both the local and regional readout cards have been redesigned. Since the triggering functionalities are abandoned, a more streamlined approach has been introduced. The hardware implementation of the regional and local card is almost identical, minimizing the design and development effort by re-using the same hardware and altering the FPGA firmware. The global crate has been replaced by a regional crate equipped with a J2 backplane bus card which acts as an interface between the regional and local cards.

## 2.2 RPC detectors

In the ALICE cavern, three distinct forms of RPC are installed. They refer to long, short, and cut forms, respectively. The beam pipe is accommodated by the short cut forms. The present RPCs are constructed with 2 mm wide gas gaps, 2 mm thick High-Pressure Laminate (HPL or bakelite) resistive electrodes, and polyamide insulation layers. The readout strips are made of copper and have three different pitch options: 1, 2, or 4 cm. Both RPCs have one collection of readout strips on each hand. The strips on either side of the RPCs are orthogonal to one another. In comparison to the dipole motion on charged-particle tracks, the vertical strips that have (y) hits are referred to as non-bending and the horizontal strips that have (x) hits are referred to as bending.



**Figure 2.1**: RPC strip patterns

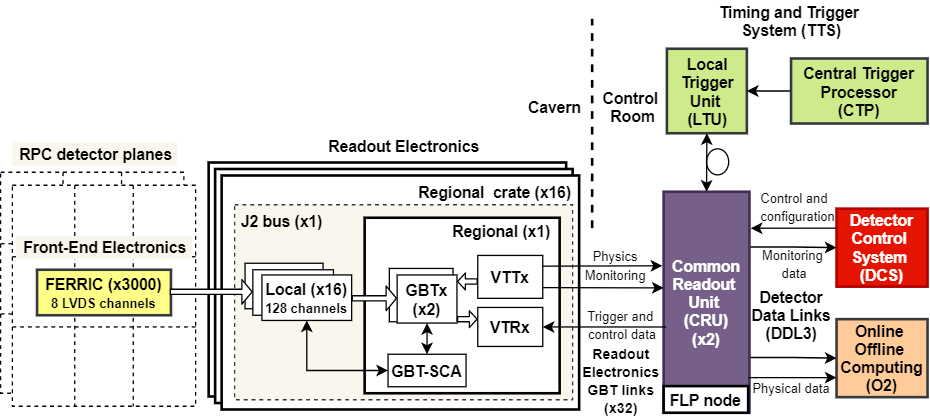
Scientists predict an improvement in RPC hits in Pb-Pb collisions to exceed the highest counting rate of about 10 Hz/cm2 up to 90 Hz/cm2 [ ] which is marginally similar to the maximum rated capacity of the sub-detector in maxi-avalanche mode [ ]. This rise would also hasten the aging of the gas gaps, which will hit the end of their projected lifespan long before the end of Run 3, necessitating the replacement of certain gas gaps and other affected components.

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| 2 | Readout chain |

These updates are distributed among three institutions. The Puricelli factory in Costa Masnaga (Italy) is responsible for redesigning the bakelite resistive electrodes, which feature a smoother surface for the bakelite used on the presently installed RPCs, the General Tecnica in Colli (Italy) is responsible for manufacturing the gas gaps for the new RPCs and, the National Institute for Nuclear Physics (INFN) in Torino (Italy) is responsible for checking and testing the performance of the new RPCs with cosmic rays. The installation of the new RPCs in the cavern is expected to start from July 2021, with the intent of installing 2 RPCs per day. In case of failure to meet this deadline, the MID will operate with the existing RPCs during Run 3 until the new RPCs are ready.

## 2.3 Readout chain

In total, the readout chain consists of 21 000 strips attached to 72 RPCs and spread over multiple front-end electronics cards equipped with one or two FEERIC ASICs. The signals from the FEERICs are propagated to the readout electronics, acting as the readout interface and in charge of the first stage of the trigger decision. The readout electronics are mounted on the upper gangways where the radiation is low. The beam collisions will produce a lot of radiation in the area around ALICE, therefore the readout electronics cards are equipped with radiation hardening to operate properly. The CRUs combine and multiplex data from multiple readout electronics cards as well as timing and trigger information from the Timing and Trigger system (TTS) before transmission to the O² computing facility for processing and storage in the next layer of the readout chain. The CRUs are mounted in computers housed in the intermediary computer room, called the counting room, away from the ALICE cavern and thus do not require radiation hardening, as is the case for the readout electronics. These computers can be reached over the network from the main Detector Control System (DCS). The DCS manages the readout chain by sending commands and monitoring the system. Experiment data are moved from the FLP node to the O² computing system for processing and storage. A block diagram of the readout chain is shown in Figure 2.2.



**Figure 2.2**: MID readout chain architecture

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### 2.3.1 Front-End Electronics for the RPCs

The FEERIC is an 8-channel ASIC that uses low-cost AMS 0:35mm CMOS technology developed by the Laboratory of Physics Clermont-Ferrand (LPC Clermont-Ferrand). It is made up of a trans-impedance amplifier stage, a zero-crossing discriminator to limit time walk effects, and a one-shot to prevent retriggering during 100 ns and LVDS drivers. Table 2.1 summarizes the main specifications, and requirements of the FEERIC ASIC. Fig.2.3 below depicts FEERIC's functional single-channel block diagram.

**Table 2.1**: Requirements of the FEERIC ASIC

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| feature | value or type |
| pulse polarity | positive or negative |
| # of channels | 8 |
| power consumption per channel | < 100 mW |
| input impedance | < 50 W |
| dynamic range | 20 fC < q < 3 pC |
| time resolution | < 1 ns |
| time walk | < 2 ns |
| one-shot | 100 ns |
| output format | LVDS |
| signal shape | square pulse 23±3 ns |

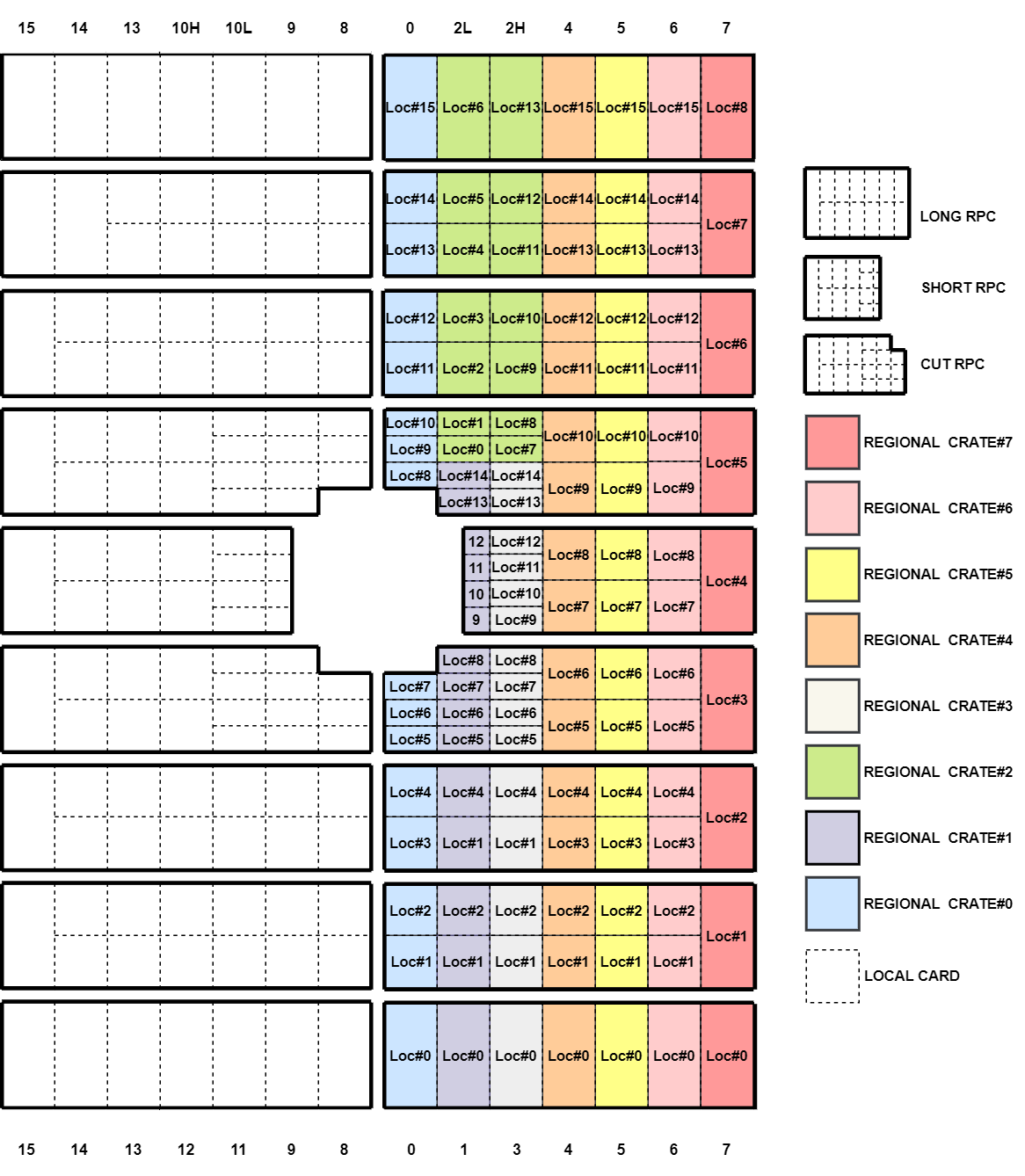
In contrast to the ADULT card thresholds, which were formerly set using an analog voltage spread of just one threshold value per RPC, the FEERIC card thresholds would be set wirelessly. Their values will be assigned to each card, allowing one to fine-tune the threshold based on the local RPC efficiency while minimizing operating high voltage. The technology selected to accomplish this task is the ZIGBEE protocol. It is a wireless technology established as an open universal norm to meet the special requirements of low-cost, low-power wireless IoT networks based on the IEEE 802.15.4 physical radio interface and works in unlicensed bands such as 2.4 GHz. The ZEGBEE is incorporated on the Atmel SAMD21 microcontroller and the program is based on Arduino libraries (I2C, SD cards, and Xbee module). This is then put onto a printed circuit board called the Xbee cards. The master cards are linked to the DCS PC using ethernet, and the ZIGBEE (wireless) protocol is used to communicate from master to nodes.

As previously mentioned, the charge delivered within the gas gaps must be lowered to minimize aging and improve rate capabilities. This is achieved by operating RPCs with the same gas mixture but at a lower gain, in conjunction with new FEERIC ASICs which perform amplification of the analog signal before discrimination. So far, (2384 + 336 spares) FEERIC cards and 26 Xbee cards have been manufactured and installed in the ALICE cavern. The installation and commissioning of all FEERIC and Xbee cards concluded in July 2019 [ ].

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## 2.3 Readout electronics

As shown in Fig 2.3, the readout electronics are divided into 16 vertical regions (8 on the left and 8 on the right side of the plane). Each vertical region is read out by a single regional crate. Each regional crate contains a backplane bus card called a J2 card, which connects to a single regional card and up to 16 local cards.



**Figure 2.3**: Geometry of the readout electronics

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### 2.3.1 Local and Regional card

For each LHC clock tick, the local card receives binary data from LVDS channels, which indicates whether the corresponding channel has been struck or not. The local card is embedded with the Intel MAX 10 FPGA and its firmware performs the following functions:

* Remotely configure and mask noisy FEERIC channels
* Read or read/write the internal DCS registers using the I²C protocol
* Remotely reset and configure the position of the local card in the crate
* Compensate the different transmission delays (per step of 3.12 ns) from different cables coming from the FEERIC cards.
* Prepare the informative part of an event and send a data byte (0x00 if no events of interests happen) to the regional card using one 320 Mbit/s serial electrical link
* Provide a local tracklet signal corresponding to a track crossing in any of the four chambers

The regional card receives the local information via 16 serial electrical links, assembles the raw events in their final format, and adds timing and trigger information. Similar to the local card, the regional card is also embedded with the Intel MAX 10 FPGA and unlike the local card, it is equipped with two bi-directional 3.2 Gbit/s GBT links to send the data to the CRU.

Fig. 2.5 shows a block diagram of the local and regional hardware implementation.

### 2.3.2 J2 backplane bus card

The J2 bus card serves as an interface between the regional crate and the local/regional cards in terms of power and serves as an interface between the local and regional in terms of signal transfer. It is equipped with a 4-bit dip switch for assigning a specific identification to the regional crate, as well as 3 LEDs for monitoring the status of the voltages (2.5V, 3.3V, 5V, GND) supplied to the regional and local cards.

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| *Coding of*  *SOx, EOx, RESET*  *events in LOCAL* | *Bits* |  | *Coding of*  *PHY, ORB*  *events in LOCAL* | *Bits* |  | *Coding of*  *self-triggered DATA*  *event in LOCAL* | *Bits* |
| START BIT (always '1')  CARD TYPE (always '1'=LOCAL)  LOCAL BUSY ('0'=OK; '1'=FIFO full)  LOCAL DECISION (tracklet)  ACTIVE ('0'=OFF; '1'=ON)  REJECTING ('0'=OFF; '1'=ON)  MASKED ('0'=OFF; '1'=ON)  OVERWRITED ('0'=OFF; '1'=ON) | 1  1  1  1  1  1  1  1  1 | START BIT (always '1')  CARD TYPE (always '1'=LOCAL)  LOCAL BUSY ('0'=OK; '1'=FIFO full)  LOCAL DECISION (tracklet)  ACTIVE ('0'=OFF; '1'=ON)  REJECTING ('0'=OFF; '1'=ON)  MASKED ('0'=OFF; '1'=ON)  OVERWRITED ('0'=OFF; '1'=ON) | 1  1  1  1  1  1  1  1  1 | START BIT (always '1')  CARD TYPE (always '1'=LOCAL)  LOCAL BUSY ('0'=OK; '1'=FIFO full)  LOCAL DECISION (tracklet)  ACTIVE (always '1'=ON)  REJECTING (always '0'=OFF;)  MASKED ('0'=OFF; '1'=ON)  OVERWRITED ('0'=OFF; '1'=ON) | 1  1  1  1  1  1  1  1  1 |
| SOx  EOx  PAUSE (always '0')  RESUME (always '0')  CALIBRATE (ignored)  PHY (ignored)  RESET  ORB | 1  1  1  1  1  1  1  1 | SOx (always '0')  EOx (always '0')  PAUSE (always '0')  RESUME (always '0')  CALIBRATE (always '0')  PHY  RESET (always '0')  ORB | 1  1  1  1  1  1  1  1 | Always '0' | 8 |
| LOCAL bunch counter | 16 | LOCAL bunch counter | 16 | LOCAL bunch counter | 16 |
| LOCAL board position in Crate (0-15) | 4 | LOCAL board position in Crate (0-15) |  | LOCAL board position in Crate (0-15) |  |
| Status: "0xF" | 4 | Always '0' |  | Data: detector plane(s) (1 bit / plane) |  |
| Status: Mask registers  [(X4, Y4), (X3, Y3), (X2, Y2), (X1, Y1)] | 32\*4 | N/A | 0 | Data: Only masked strip pattern(s)  [(X4, Y4), (X3, Y3), (X2, Y2), (X1, Y1)] | 32\*i |
| Total number of bits |  | Total number of bits | 40 | Total number of bits | 8\*bc |
| Bunches needed to send |  | Bunches needed to send | 5 | Bunches needed to send | 9 - 21 |

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| *Coding of*  *SOx, EOx, RESET*  *events in REGIONAL* | *Bits* |  | *Coding of*  *PHY, ORB*  *events in REGIONAL* | *Bits* |  | *Coding of*  *self-triggered DATA*  *event in REGIONAL* | *Bits* |
| START BIT (always '1')  CARD TYPE (always '1'=LOCAL)  LOCAL BUSY ('0'=OK; '1'=FIFO full)  LOCAL DECISION (tracklet)  ACTIVE ('0'=OFF; '1'=ON)  REJECTING ('0'=OFF; '1'=ON)  MASKED ('0'=OFF; '1'=ON)  OVERWRITED ('0'=OFF; '1'=ON) | 1  1  1  1  1  1  1  1  1 | START BIT (always '1')  CARD TYPE (always '1'=LOCAL)  LOCAL BUSY ('0'=OK; '1'=FIFO full)  LOCAL DECISION (tracklet)  ACTIVE ('0'=OFF; '1'=ON)  REJECTING ('0'=OFF; '1'=ON)  MASKED ('0'=OFF; '1'=ON)  OVERWRITED ('0'=OFF; '1'=ON) | 1  1  1  1  1  1  1  1  1 | START BIT (always '1')  CARD TYPE (always '1'=LOCAL)  LOCAL BUSY ('0'=OK; '1'=FIFO full)  LOCAL DECISION (tracklet)  ACTIVE (always '1'=ON)  REJECTING (always '0'=OFF;)  MASKED ('0'=OFF; '1'=ON)  OVERWRITED ('0'=OFF; '1'=ON) | 1  1  1  1  1  1  1  1  1 |
| SOx  EOx  PAUSE (always '0')  RESUME (always '0')  CALIBRATE (ignored)  PHY (ignored)  RESET  ORB | 1  1  1  1  1  1  1  1 | SOx (always '0')  EOx (always '0')  PAUSE (always '0')  RESUME (always '0')  CALIBRATE (always '0')  PHY  RESET (always '0')  ORB | 1  1  1  1  1  1  1  1 | Always '0' | 8 |
| REGIONAL bunch counter | 16 | REGIONAL bunch counter | 16 | REGIONAL bunch counter | 16 |
| REGIONAL crate position (0-15) | 4 | REGIONAL position crate (0-15) | 4 | REGIONAL crate position (0-15) | 4 |
| Status: "0xF" | 4 | Always '0' | 4 | Data: detector plane(s) (1 bit / plane) | 4 |
| Total number of bits | 40 | Total number of bits | 40 | Total number of bits | 40 |
| Bunches needed to send | 5 | Bunches needed to send | 5 | Bunches needed to send | 5 |

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### 2.3.3 Event data format

Events are stored in the local card multi-event buffer at each trigger. The range of the acceptable trigger latency is 0.5-9.6 ns. The multi-event buffer in the local card is larger than the size of one software event (registered at a very low rate) which includes, in addition to the standard physics event information, the counters. The maximum size of a software event, obtained in case of calibration events with the front-end test (FET) generator for which zero suppression is not efficient, because all strips are fired, is 50 words of 32 bits. It corresponds to a depth of 10 physics events (maximum 5 words of 32 bits). The implementation of 2 GBTs per regional card leaves the option of a complete VFE data transfer (5.12 Gbit/s), at 40 MHz without zero suppression, from the local cards directly to the CRUs (typically one CRU per regional area in this case). This solution corresponds to a continuous readout, however, with an increased cost due to the higher number of optical GBT links to the CRUs. The expected data flow in pp and PbPb is given in Tab. 7.4. It includes a preliminary evaluation of event separators and headers which contribute significantly to the event size. The total data flow in PbPb at 100 kHz amounts to 320 MB/s. The readout dead time is expected to be negligible with a single DDL3 link at 10 Gbit/s. Anyhow a busy mechanism will be implemented.

## 2.4 GBT protocol

The Gigabit Transceiver (GBT) architecture is an optical serial data link developed at CERN, designed for use in the LHC, which requires high bandwidth as well as radiation hardening[12]. It is frame-based, with one 120-bit frame transmitted continuously at an interval of 25 ns. This results in a raw serial line rate of 4.8 Gb/s. 25 nm corresponds to the LHC bunch crossing interval. The bunch crossing interval is the time between bunches of particles crossing each other in the LHC. In other words, it is the time between potential collisions.

The GBT link is implemented in the ITS readout chain in two ways. Radiation hardened ASIC called GBTx is used on the readout unit. This ASIC can accept data in parallel as input, serialize and encode the data, and output it to a laser transmitter, and opposite for the downlink. The laser transmitter used is a custom unit also designed at CERN to be radiation hardened. On the common readout unit, the GBT link controller is implemented as a module on the FPGA. The GBT protocol specifies three different frame modes; the standard GBT frame mode, the wide frame mode, and the 8B/10B frame mode. ITS will use the standard GBT frame, illustrated in figure 9. This frame starts with a 4-bit long header. The header can be either 0b0101, which signals that the frame contains valid data, or 0b0110, which signals the opposite, for example, if the transmitter is idle, or the frame contains non-data information, such as SingleWord Transactions (SWT). Then follow 4 bits for slow control information, of which the first 2 bits are for Internal Control (IC), strictly reserved for control of the GBTx ASIC. The last 2 bits for slow control are for External Control (EC). Next follows the main data payload of 80 bits. The data and EC fields are not pre-assigned and can be used for different purposes such as Data Acquisition (DAQ), Timing and Trigger Control (TTC), or experiment control, depending on requirements. The last 32 bits are used for error correction. This leaves 84-bits per frame, or 3.36 Gb/s, of usable bandwidth, of which 3.2 Gb/s is dedicated to data. Before transmitting the frame, the data, EC, and IC fields are fed through a scrambling algorithm in which DC balances them. Then, a Reed-Solomon encoder generates the 32 error correcting bits based on the scrambled data in addition to the header. The receiver does the opposite; first decoding and checking the error correction bits, then de-scrambling the data before the IC, EC and data fields can be read. This is illustrated in figure 10.

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The 4-bit header is used to track frames and synchronize the receiver to the transmitter. The header is not affected by the scrambling so that it can be easily detected. When a GBT receiver is powered up, it enters a frame-lock acquisition mode in which it searches for valid headers. Once a configurable amount of frames with valid headers have been detected in succession, it considers the link established and enters frame-tracking mode. In this mode, it receives data and operates normally, while keeping track of invalid headers. Once a configurable amount of frames in succession is found to be invalid, it considers the synchronization lost and re-enters the acquisition mode. Typically multiple invalid frames are needed to trigger this, so that occasional random single event upsets aren’t enough to cause the link to fall out of synchronization. The data field (80-bit) of the GBT frame is used to transmit the data. GBT frames are differentiated into control frames and data frames, with the header specifying data valid for the latter only. Control frames start with a 4-bit identifying header. Four headers are defined: IDLE, SOP (Start Of Packet), EOP (End Of Packet), and SWT. IDLE frames contain no information. SOP and EOP, as the names suggest, mark the start and end of packets of data from the detectors. They contain various metadata relating to the packets such as length and tags.

Single Word Transactions frames can contain arbitrary data used for special control or data transfers. In the GBT downlink, this will normally be the only type of GBT frame. In the uplink, SWT frames may only be sent in between data frames, in other words between EOP and SOP control frames. In the ITS readout electronics, SWT frames are for example used to access the register bus on the readout unit main FPGA.

### 2.4.1 Slow Control

Part of the GBT link is the slow control system. The 2 bytes in the EC field of the GBT frame payload is forwarded to a dedicated ASIC for slow control called GBTSCA. This chip is part of the readout unit board as mentioned. On the CRU main FPGA, the SCA communication is implemented as part of the GBT VHDL module. The GBT-SCA ASIC contains several communication modules, including a range of GPIO, ADC and DAC pins, as well as I²C, SPI and JTAG masters[13]. These modules are connected to various components on the board such as the FPGAs. Communication with the GBT-SCA is done using the High Level Data Link Control (HDLC) serial protocol. This protocol is command based. Rather than reading and writing directly to registers, transactions specify a command ID, a transaction ID and data if the command requires it. Command IDs determine what the GBT-SCA chip will do, for example writing or reading registers or executing operations. Every command transaction returns a package with the same transaction ID. The return packet contain status info and returned data if there is any. The IC slow control field is used for accessing the GBTx registers, for configuration and monitoring. This field can also control the laser transceivers through a master communication module on the GBTx chip, accessible through its registers.

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## 2.5 Timing and trigger system

### 2.5.1 Central Trigger Processing

### 2.5.2 Local Trigger Unit

## 2.6 Common readout unit

## 2.7 Detector control system

The MID readout process is monitored and controlled by the ALICE Detector Control System (DCS). The DCS system accesses the readout electronics via the FLP and CRUs through a network connection.

One of the protocols considered for the communication between the CRU and DCS is called ALF (On the CRU side) and FRED (On the DCS side). This protocol is based on Distributed Information Management System (DIM). DIM is a communication system for distributed/mixed environments, originally developed for one of the experiments of the Large Electron–Positron Collider, an earlier particle accelerator at CERN[14]. It provides a network transparent inter-process communication layer. The FLP host computer runs a DIM server, which acts as a bridge between the DIM network and the CRU driver, allowing DCS to communicate with the CRU from the control center without physical access to the CRU host computer.

The DCS data is extracted from the data stream and sent to ALF (Alice Low Level Front-end) interface, which publishes the data to the upper layers of the software. ALF can also receive commands and converts them to data words to be sent to the front-end electronics. To keep the ALF detector neutral, its functionality is restricted to the basic I/O operations. In the current implementation, the ALF can read/write registers implemented on the front-end modules and publish the data using a DIM service. The data published by ALF could be single values, or blocks of data prepared by the electronics modules.

## 2.8 Online Offline computing system

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## 2.9 References