**Chapter 2**

# Muon identifier readout chain

As discussed in the previous chapter, the approach taken by ALICE is to read out all Pb-Pb events at an interaction rate of 50 kHz. The objective behind the upgrades is to significantly improve vertexing and tracking capabilities at low transverse momentum. In line with the ALICE upgrades, the MID readout chain is also being upgraded to support continuous readout operation after the LS2. This upgrade entails:

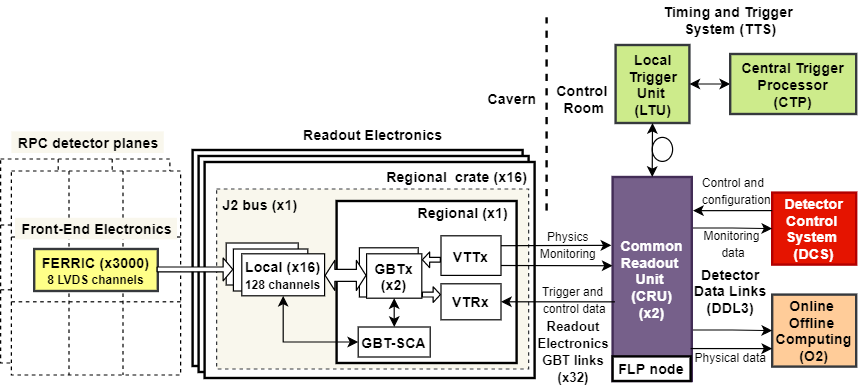
* New RPCs;
* New front-end electronics;
* New readout electronics

This chapter deals with the description of the MID readout chain and is organized as follows. Section 2.1 gives a brief overview of the readout chain. The upgrades of the RPCs is described in section 2.2, while the front-end and readout electronics upgrades are discussed in sections 2.3 and 2.4. The CRU is the heart of the readout chain, and its hardware architecture is discussed in section 2.5. The timing and trigger, online-offline computing, and detector control systems are discussed accordingly in the following sections.

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## 2.1 Overview

The readout chain block diagram is shown in Figure 2.1. The readout chain consists of 21 000 strips connected to 72 RPC detectors spread over multiple Front-End Electronic Rapid Integrated Circuit (FEERIC) cards equipped with one or two customized Application Specific Integrated Circuits (ASICs) [1]. The strip pattern signals from the FEERICs are propagated to the readout electronics using high-speed Low-voltage Differential Signaling (LVDS) channels. The readout electronics act as the readout interface and are in charge of the first stage of the trigger decision. They are mounted on the upper gangways inside the cavern a little further away from the detector stations, where the radiation is low. Since the colliding beams will produce a lot of radiation in the area around the ALICE detector in the cavern, the readout electronics regional cards are equipped with Gigabit Transceiver (GBT) radiation hardening to operate under these conditions. The CRUs are the key components of the chain, they combine and multiplex data from multiple readout electronic cards as well as timing and trigger information generated from the Central Trigger Processor (CTP) via the Local Trigger Unit (LTU) before transmitting the data to the O² computing facility for processing and storage. The CRUs are mounted in computers housed in the intermediary computer room, called the counting room, away from the ALICE cavern and thus do not require radiation hardening, as is the case for the readout electronics. These computers can be reached over the network from the main Detector Control System (DCS). The DCS manages the readout chain by sending commands and monitoring the system. Experimental data are moved from the First Level Processor (FLP) node to the O² computing system for processing and storage.

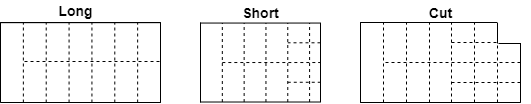


**Figure 2.1**: A schematic deciption of the MID readout chain architecture

## 2.2 RPC detectors

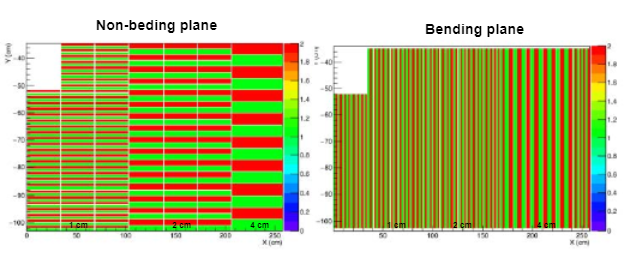
In the ALICE cavern, three distinct forms of RPC are installed. They refer to long, short, and cut forms, respectively (Fig.2.2). The beam pipe is accommodated by the short-cut forms. The composition of the current RPCs was discussed in section 1.1.4. Their pick-up strips are made of copper and have three different pitch options: 1, 2, or 4 cm. The RPCs have one collection of pick-up strips on each hand.

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**Figure 2.2**: Three forms of RPCs found in the ALICE cavern

The strips on either side of the RPCs are orthogonal to one another. In comparison to the dipole motion on charged-particle tracks, the vertical strips that have (y) hits are referred to as non-bending plane and the horizontal strips that have (x) hits are referred to as bending plane as shown in Figure 2.3.



**Figure 2.3**: RPC non-bemding and bending strip patterns

As described in [2], the amount of RPC hits in Pb-Pb collisions is expected to exceed the highest counting rate of about 10 Hz/cm² up to 90 Hz/ cm². This is marginally similar to the maximum rated capacity of the detector in the maxi-avalanche mode during the LHC Run 2. This rise would also hasten the aging of the gas gaps, which will hit the end of their projected lifespan long before the end of Run 3, necessitating the replacement of certain gas gaps and other affected components.

These upgrades are distributed among three institutions. The Puricelli factory in Costa Masnaga (Italy) is responsible for redesigning the bakelite resistive electrodes, which feature a smoother surface for the bakelite used on the presently installed RPCs, the General Tecnica in Colli (Italy) is responsible for manufacturing the gas gaps for the new RPCs and, the National Institute for Nuclear Physics (INFN) in Torino (Italy) is responsible for checking and testing the performance of the new RPCs with cosmic rays. The installation of the new RPCs in the cavern is expected to start from July 2021, with the intent of installing 2 RPCs per day. In case of failure to meet this deadline, the MID will operate with the existing RPCs during Run 3 until the new RPCs are ready.

## 2.3 Front-End electronics

The RPC ADULT electronics have been replaced by the new FEERIC and unlike the ADULT, it performs amplification of analog signals from the RPCs. The FEERIC is an 8-channel ASIC, which uses low-cost AMS 0:35mm CMOS technology developed by the Laboratory of Physics Clermont-Ferrand. It is made up of a trans-impedance amplifier stage, a zero-crossing discriminator to limit time walk effects, and a one-shot to prevent retriggering during 100 ns and LVDS drivers. Table 2.1 summarizes the main specifications, and requirements of the FEERIC ASIC. In contrast to the ADULT card thresholds, which were set using an analog voltage distribution of just one threshold value per RPC, the FEERIC card thresholds would be set wirelessly during the LHC Run 3. Their values will be assigned to fine-tune the threshold based on the local RPC efficiency while minimizing operating high voltage.

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The technology selected to accomplish this task is the ZIGBEE protocol [3]. It is a wireless technology established as an open universal norm to meet the special requirements of ultra-low-cost, low-power wireless IoT networks based on the IEEE 802.15.4 physical radio and works in unlicensed bands such as 2.4 GHz. The ZEGBEE is incorporated on the Atmel SAMD21 microcontroller [4] and the program is based on Arduino libraries (I2C, SD cards, and Xbee module). This is then put onto a printed circuit board called the Xbee cards. The master cards are connected to the DCS PC using ethernet, and the ZIGBEE (wireless) protocol is used to communicate from master to nodes.

**Table 2.1**: Requirements of the FEERIC ASIC [1]

|  |  |
| --- | --- |
| **Feature** | **Value or type** |
| pulse polarity | positive or negative |
| # of channels | 8 |
| power consumption per channel | < 100 mW |
| input impedance | < 50 W |
| dynamic range | 20 fC < q < 3 pC |
| time resolution | < 1 ns |
| time walk | < 2 ns |
| one-shot | 100 ns |
| output format | LVDS |
| signal shape | square pulse 23±3 ns |

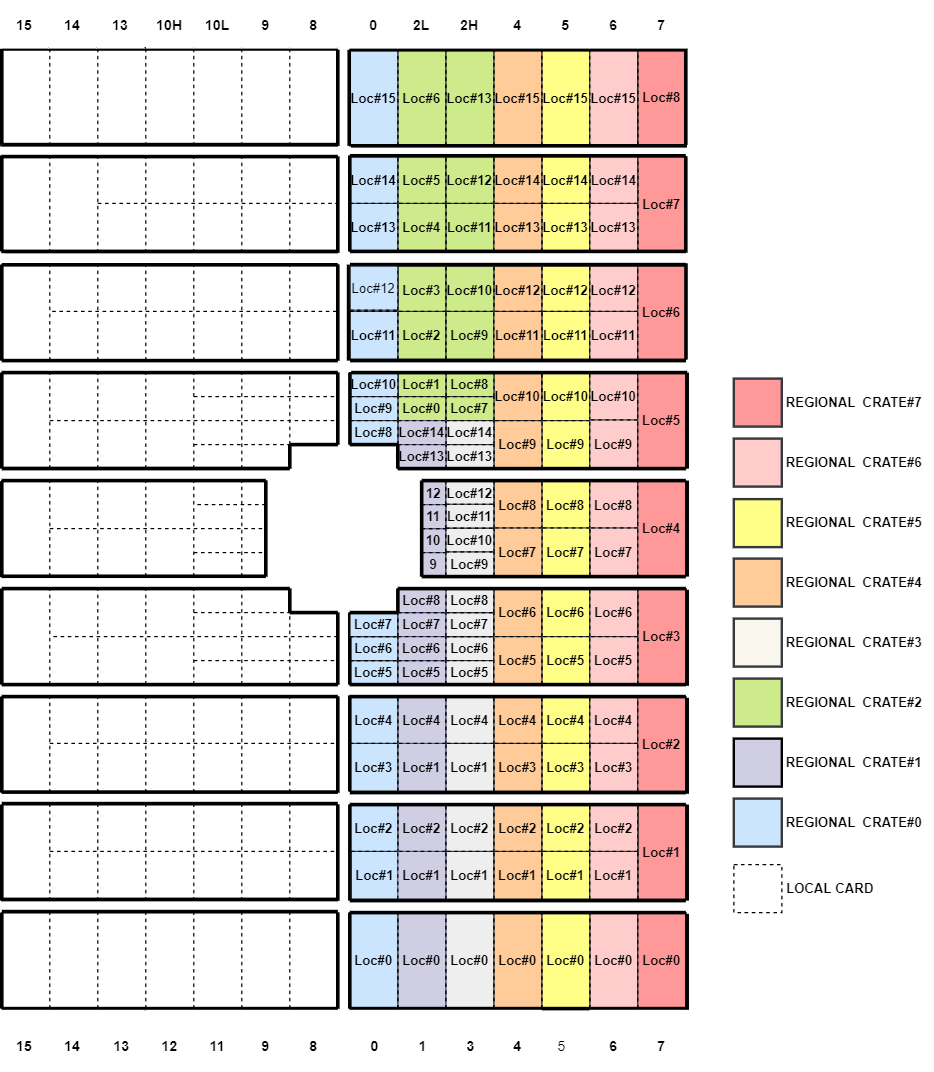
As previously mentioned, the charge delivered within the gas gaps must be lowered to minimize aging and improve rate capabilities. This is achieved by operating RPCs with the same gas mixture but at a lower gain, in conjunction with the FEERICs, which perform amplification of the analog signal before discrimination. Hitherto 2384 + 336 spares FEERIC cards and 26 Xbee cards have been manufactured and installed in the ALICE cavern. The installation and commissioning of all FEERIC and Xbee cards concluded in July 2019.

## 2.4 Readout electronics

To cope with the new readout rates, the local and regional readout cards have been redesigned. Since the triggering functionalities are abandoned, a more streamlined approach has been introduced. The hardware implementation of the regional and local card is almost identical, minimizing the design and development effort by re-using the same hardware and altering the FPGA firmware. The global crate has been replaced by a new regional crate.

As shown in Figure 2.3, the readout electronics are divided into 16 vertical regions (8 on the left and 8 on the right side of the plane). Each vertical region is read out by a single regional crate. Each contains a backplane bus card called the J2 card, which connects to a single regional card and up to 16 local cards.

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**Figure 2.3**: Geometry of the readout electronic

### 2.4.1 Local card

For every bunch crossing, the local card receives binary data from LVDS channels, which indicates whether the corresponding channel has been struck or not. The local card is equipped with 16 LVDS input connectors (32 pins, for both the BP and NBP). It is embedded with the Intel MAX 10 FPGA (10M50DCF484C7G) [5] its firmware is described here [6].

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### 2.4.2 J2 bus card

The J2 bus card serves as an interface between the regional crate and the local/regional cards in terms of power, and it also serves as an interface between the local and regional cards in terms of data transfer. The J2 bus card has a 4-bit dip switch for assigning a specific identification to the regional crate, as well as three LEDs for monitoring the voltages (2.5V, 3.3V, and 5V) supplied to the regional and local cards.

### 2.4.3 Regional card

The regional card collects data from up to 16 local cards using the GBT protocol, which is discussed in the next section. Similar to the local card, the regional card is incorporated with the same Intel MAX 10 FPGA. However, unlike the local card, it is equipped with two bi-directional GBT optical links allowing transmission and reception of data to/from the CRU. The implementation of 2 GBT optical links per regional card enables complete regional crate data transfer. The firmware implemented in the regional card FPGA is a slightly modified version of the local card firmware, which is also described in [6].

### Event data formats

Events are stored in the local and regional card multi-buffers for each trigger. The multi-event buffer in the local card carries strip patterns, therefore it is larger than the regional card. The event data formats of the local card and regional card are shown in Tab.2.2 and Tab.2.3 accordingly.

**Table 2.2**: Local event format [6]

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| *Coding of*  *SOx, EOx, RESET, CALIBRATE*  *Event in LOCAL* | *Bits* |  | *Coding of*  *PHY, ORB*  *Event in LOCAL* | *Bits* |  | *Coding of*  *self-triggered DATA*  *Event in LOCAL* | *Bits* |
| START BIT (always '1')  CARD TYPE (always '1'=LOCAL)  LOCAL BUSY ('0'=OK; '1'=FIFO full)  LOCAL DECISION (tracklet)  ACTIVE ('0'=OFF; '1'=ON)  REJECTING ('0'=OFF; '1'=ON)  MASKED ('0'=OFF; '1'=ON)  OVERWRITED ('0'=OFF; '1'=ON) | 1  1  1  1  1  1  1  1  1 | START BIT (always '1')  CARD TYPE (always '1'=LOCAL)  LOCAL BUSY ('0'=OK; '1'=FIFO full)  LOCAL DECISION (tracklet)  ACTIVE ('0'=OFF; '1'=ON)  REJECTING ('0'=OFF; '1'=ON)  MASKED ('0'=OFF; '1'=ON)  OVERWRITED ('0'=OFF; '1'=ON) | 1  1  1  1  1  1  1  1  1 | START BIT (always '1')  CARD TYPE (always '1'=LOCAL)  LOCAL BUSY ('0'=OK; '1'=FIFO full)  LOCAL DECISION (tracklet)  ACTIVE (always '1'=ON)  REJECTING (always '0'=OFF;)  MASKED ('0'=OFF; '1'=ON)  OVERWRITED ('0'=OFF; '1'=ON) | 1  1  1  1  1  1  1  1  1 |
| SOx  EOx  PAUSE (always '0')  RESUME (always '0')  CALIBRATE  PHY (ignored)  RESET  ORB | 1  1  1  1  1  1  1  1 | SOx (always '0')  EOx (always '0')  PAUSE (always '0')  RESUME (always '0')  CALIBRATE (always '0')  PHY  RESET (always '0')  ORB | 1  1  1  1  1  1  1  1 | Always '0' | 8 |
| LOCAL bunch counter | 16 | LOCAL bunch counter | 16 | LOCAL bunch counter | 16 |
| LOCAL board position in Crate (0-15) | 4 | LOCAL board position in Crate (0-15) |  | LOCAL board position in Crate (0-15) |  |
| Status: "0xF" | 4 | Always '0' |  | Data: detector plane(s) (1 bit / plane) |  |
| Status: Mask registers (SOx=’1’|EOx=’1’)  Data: all strip patterns (not masked)  [(X4, Y4), (X3, Y3), (X2, Y2), (X1, Y1)] | 32\*4 | N/A | 0 | Data: Only masked strip pattern(s)  [(X4, Y4), (X3, Y3), (X2, Y2), (X1, Y1)] | 32\*i |
| Total number of bits | 168 | Total number of bits | 40 | Total number of bits | 8\*bc |
| Bunches needed to send | 21 | Bunches needed to send | 5 | Bunches needed to send | 9 - 21 |

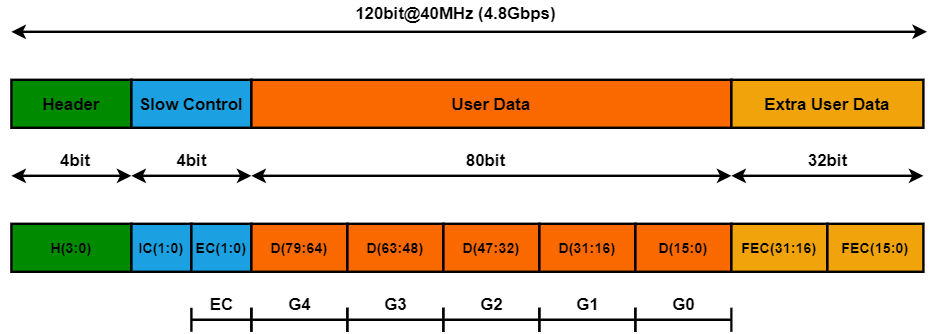
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**Table 2.3**: Regional event format [6]

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| *Coding of SOx, EOx, RESET, CALIBRATE Event in REGIONAL* | *Bits* |  | *Coding of PHY, ORB Event in REGIONAL* | *Bits* |  | *Coding of self-triggered DATA Event in REGIONAL* | *Bits* |
| START BIT (always '1')  CARD TYPE (always '1'=LOCAL)  LOCAL BUSY ('0'=OK; '1'=FIFO full)  LOCAL DECISION (tracklet)  ACTIVE ('0'=OFF; '1'=ON)  REJECTING ('0'=OFF; '1'=ON)  MASKED ('0'=OFF; '1'=ON)  OVERWRITED ('0'=OFF; '1'=ON) | 1  1  1  1  1  1  1  1  1 | START BIT (always '1')  CARD TYPE (always '1'=LOCAL)  LOCAL BUSY ('0'=OK; '1'=FIFO full)  LOCAL DECISION (tracklet)  ACTIVE ('0'=OFF; '1'=ON)  REJECTING ('0'=OFF; '1'=ON)  MASKED ('0'=OFF; '1'=ON)  OVERWRITED ('0'=OFF; '1'=ON) | 1  1  1  1  1  1  1  1  1 | START BIT (always '1')  CARD TYPE (always '1'=LOCAL)  LOCAL BUSY ('0'=OK; '1'=FIFO full)  LOCAL DECISION (tracklet)  ACTIVE (always '1'=ON)  REJECTING (always '0'=OFF;)  MASKED ('0'=OFF; '1'=ON)  OVERWRITED ('0'=OFF; '1'=ON) | 1  1  1  1  1  1  1  1  1 |
| SOx  EOx  PAUSE (always '0')  RESUME (always '0')  CALIBRATE  PHY (ignored)  RESET  ORB | 1  1  1  1  1  1  1  1 | SOx (always '0')  EOx (always '0')  PAUSE (always '0')  RESUME (always '0')  CALIBRATE (always '0')  PHY  RESET (always '0')  ORB | 1  1  1  1  1  1  1  1 | Always '0' | 8 |
| REGIONAL bunch counter | 16 | REGIONAL bunch counter | 16 | REGIONAL bunch counter | 16 |
| REGIONAL crate position (0-15) | 4 | REGIONAL position crate (0-15) | 4 | REGIONAL crate position (0-15) | 4 |
| Status: Mask registers (SOx=’1’| EOx=’1’)  Data: All tracklet inputs (not masked) | 4 | Always '0' | 4 | Data: detector plane(s) (1 bit / plane) | 4 |
| Total number of bits | 40 | Total number of bits | 40 | Total number of bits | 40 |
| Bunches needed to send | 5 | Bunches needed to send | 5 | Bunches needed to send | 5 |

### Gigabit Transceiver protocol

The GBT protocol architecture was created at CERN, for use in the LHC, which requires high bandwidth as well as radiation protection [7]. Embedded in the regional cards is a radiation-hardened ASIC known as GBTx (Fig.2.6). This ASIC contains a high-speed serializer and deserializer that takes data and then transmits them through a laser transmitter, as well as the reverse for the downlink. The laser transmitter utilized is a special component manufactured at CERN. The GBT optical link controller is implemented as a module in the CRU firmware. The GBT protocol operates in 3 different frame modes: standard GBT frame, wide frame, and 8B/10B frame. Figure 2.4 depicts the standard GBT frame mode used in the MID readout chain.

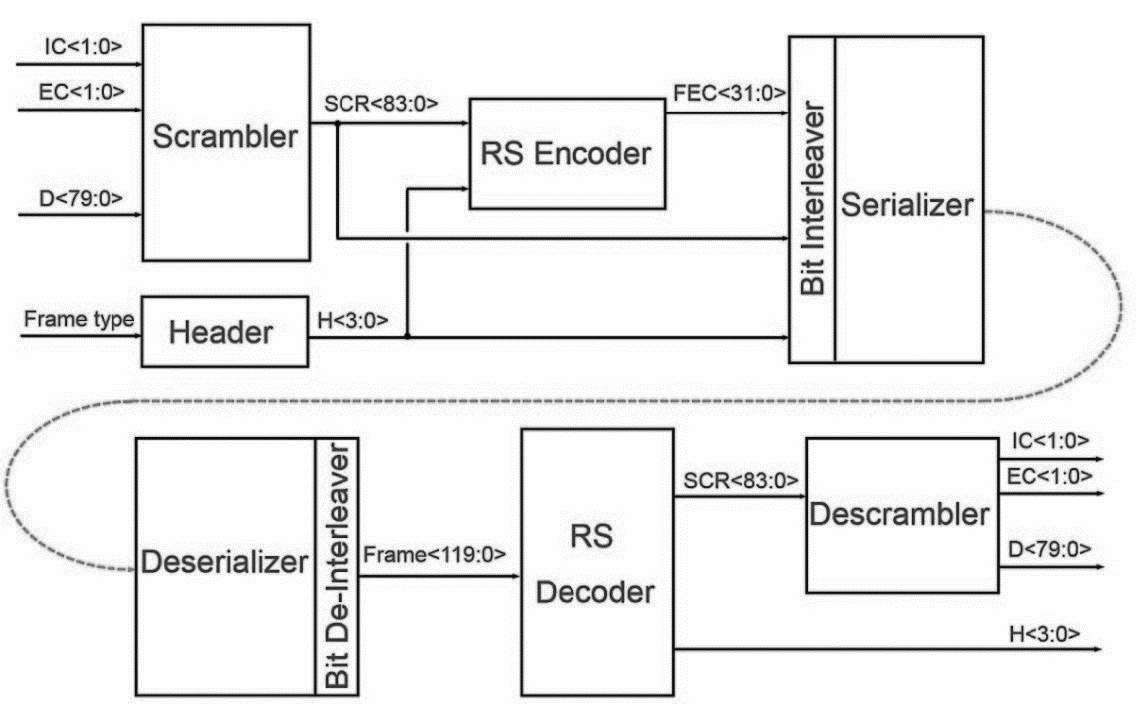


**Figure 2.4**: Block diagram of the standard GBT mode encoding and decoding. Adapted from [7]

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The standard GBT frame is continuously transmitted during a single LHC bunch crossing. It starts with a 4-bit header field, which is necessary for frame-level synchronization of the data stream. Recognizing multiple valid headers implies a proper frame-locking. The opposite implies that the frame synchronization has failed and the frame synchronization cycle must be initialized. The header field can either provide a value “0x5” (data state), which indicates that the frame includes legitimate data, or “0x6” (idle state), which indicates that the frame does not include valid data. Next is, a 4-bit used for slow control, the first two of which are for Internal Control (IC), which is reserved for controlling the GBTx ASIC. The last two slow control bits are for External Control (EC). The payload data and EC fields are not pre-assigned and are utilized for a variety of functions, including Data Acquisition (DAQ), Timing and Trigger Control (TTC), and experiment control, depending on the needs of the MID. The last 32 bits are utilized for forwarding Error Correction (FEC). The remaining 84-bit, which includes the EC, having an associated bandwidth of 3.36 Gb/s, of which 3.2 Gb/s is allocated to the payload data.

Before serialization, the data, EC, and IC fields are put through a scrambling process that concatenates them. In addition to the header, a Reed-Solomon (RS) encoder creates the 32-bit FEC based on the scrambled data. The deserializer does the opposite. Both scenarios are represented in Figure 2.5.



**Figure 2.5**: Block diagram of the standard Mode GBT encoding and decoding. Adapted from [7]

The header is used to track frames and synchronize the receiver with the sender. The header is not affected by the scrambling therefore, it is easily detectable. When a GBT receiver is powered up, it enters a frame-lock initialization mode in which it searches for valid headers. After detecting a configurable number of frames with valid headers, it considers that the connection has been established and enters the frame tracking mode, in which it receives data and runs normally while searching for invalid headers.

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Once it is determined that a configurable number of consecutive frames is invalid, the synchronization is considered lost and the initialization mode is re-entered. This usually requires multiple invalid frames, so an accidental violation of a single random frame is not enough to cause channel synchronization. The data field (80 bits) of the GBT frame is used for data transmission. GBT frames are divided into control frames, data frames, and the header contains data valid only for the latter. The frame starts with a 4-bit identification header. Four headers are defined: IDLE, Start of Packet (SOP), End of Packet (EOP), and the Single Word Transaction (SWT). The IDLE frame does not contain any information. SOP and EOP, as the name suggests, mark the beginning and end of the detector data packet, which contains various packet-related metadata. The SWT frame contains any data used for a specific control or data transmission. On the GBT uplink, SWT frames are transmitted between data frames, that is, between EOP and SOP control frames. In the MID read chain, the SWT frame is used to access the register bus on the regional card.

The 2 bytes in the EC payload of the GBT frame are routed to a special slow control ASIC called GBT-SCA [8]. As mentioned above, the chip is part of the regional card. The communications between the CRU and SCA are implemented in the CRU firmware architecture described in Chapter 3. The GBT-SCA ASIC has a large number of communication modules, including various GPIO, ADC, and DAC pins, as well as I²C, SPI, and JTAG master control. The communication between the regional FPGA and GBT-SCA is carried out through the high-level serial link control (HDLC) protocol. The protocol is based on commands. In contrast to the direct reading and writing of registers, the transaction contains the command ID, transaction ID, and data required by the command. The command ID indicates what the GBT-SCA chip will do, such as read or write registers or perform operations. Each command transaction returns a batch with the same transaction ID. The return package contains status information and returned data. The slow control IC is used for GBTx register access, configuration, and monitoring. This field can also control the laser transceivers that use the main communication modules on the GBTx chip, which can be accessed through its registers.

**Electrical-links**

The GBTx chips on the regional cards communicate with up to 8 local card FPGAs using the standard GBT frame mode. It consists of connecting the GBTx and the regional FPGAs through duplex electrical serial lines (e-links). Each GBT bi-directional optical link of the readout chain is made up of 10 serial e-links (8 local e-links + 2 internal regional e-links).

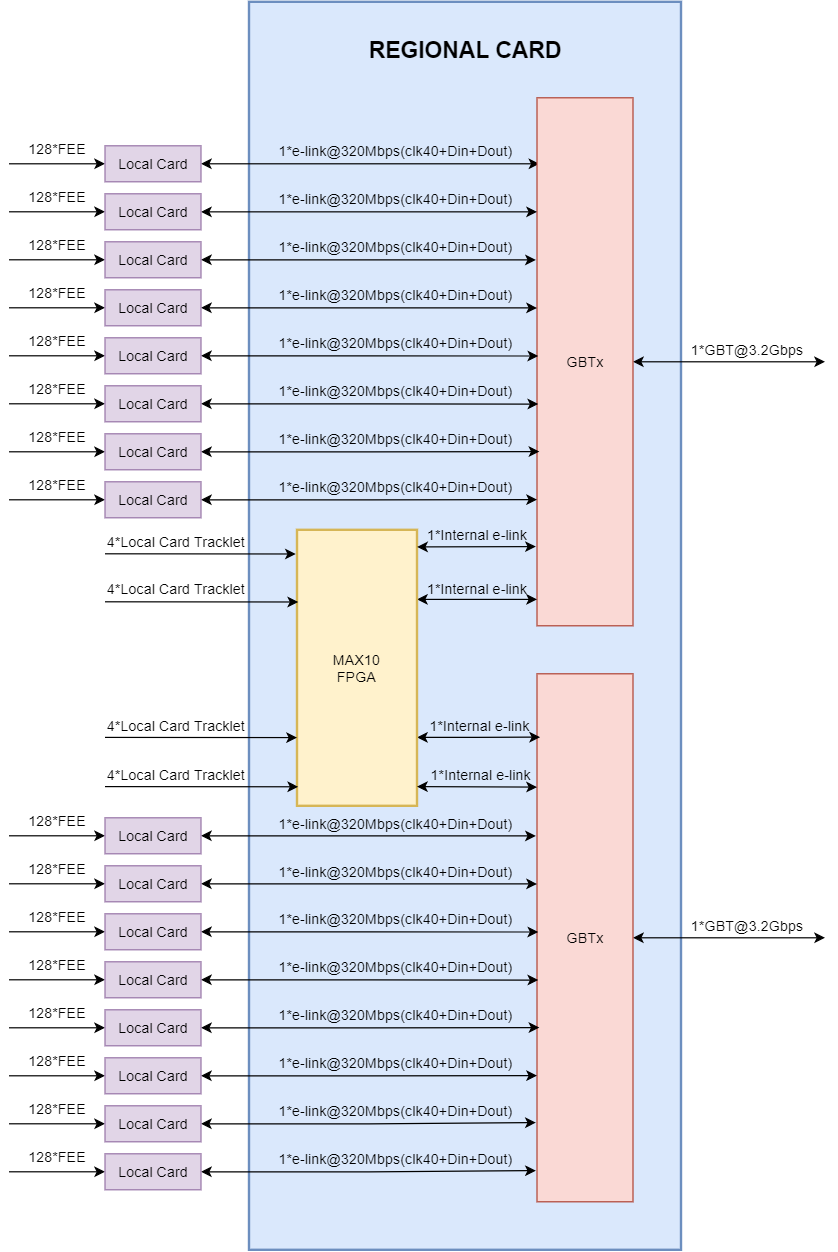
Each of these e-links consists of three signal lines (differential pairs):

* Differential Clock line (dClk+/dClk-): Clock driven by GBTx to the local/regional FPGA
* Differential Downlink data output (dOut+/dOut-): Data from GBTx to the local/regional FPGA
* Differential Uplink data input (dIn+/dIn-): Data line from the local/regional FPGA to GBTx

The MID readout chain is configured to operate at the maximum e-links data rate of 320 Mb/s, with a maximum of 2 e-links per group. As mentioned earlier, each e-link is composed of one differential clock line (dClk+/dClk-), one differential downlink output (dOut+/dOut-), and one differential uplink input (dIn+/dIn-). Thus, the maximum number of differential e-link signals per group is 3 x 2 = 6, equivalent to 6 signal pins per group. Overall, a total of 6 x 5 = 30 configuration pins are dedicated to the e-links. To provide the greatest possible signal quality and transmission reliability, the physical e-link connections are assumed to be differential transmission lines with a differential impedance of 100 Ω and a suitable termination line at the receiver end.

Figure 2.6 represents the e-links configuration between the GBTx chip and the readout electronics.

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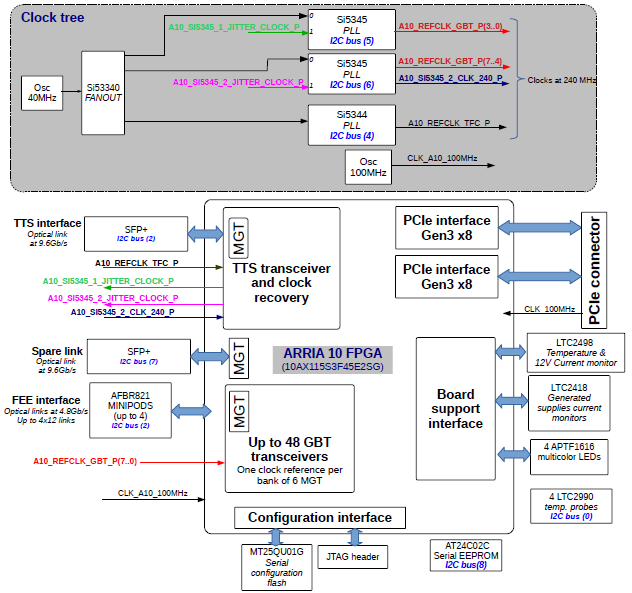


**Figure 2.6**: E-links configuration between the GBTx chip and the readout electronics.

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| 2 | Readout chain |

## Common readout unit

The ALICE CRU hardware architecture is shown in Figure 2.7. Besides the PCIe interface, which utilizes a built-in 100 MHz crystal oscillator, the clock tree is designed to utilize a single reference clock for all CRU communication links. The CRU card can either be used independently with a built-in 40MHz crystal oscillator or with a recovered clock retrieved from the TTS optical link. On the other hand, the TTS transceiver requires a constant 240 MHz reference frequency before initialization, which is generated locally with the help of a Phase-Locked Loop (PLL) SI5344. The clock recovered from the FPGA is transferred to a high-performance SI5345 PLL for jitter attenuation after it has successfully been locked to the incoming stream. The clocks extracted from the SI5345 PLL are then utilized to run the FPGA logic. The SI5345 PLL uses I²C communication to switch between local and recovered TTS clock modes. The clock generated from the built-in 100 MHz crystal oscillator is utilized to run many other features of the FPGA, including initialization and hardware monitoring.



**Figure 2.7**: A functional overview of the hardware, highlighting the functions used in the CRU [9].

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The CRU card is embedded with an Intel ARRIA10 FPGA (10AX115S3F45E2G) [10]. It is equipped with two Small Form-factor Pluggable (SFP+) connections. One is used for TTS connection, and the other is used as a backup. The connections from/to the readout electronics are ensured by up to 4x12-channel bi-directional 10.3125 Gb/s optical transceivers (mini-pods) [11]. These two mini-pods can connect to up to 24 GBT links. However, for what concerns the MID, 32 GBT links are necessary to transfer data from the complete readout electronics. Hence, 2 CRU cards are utilized, each connected to 16 GBT links.

The CRU is equipped with a PCIe edge connector on the rear end, that provides a dual gen3 x8 PCIe interface. This interface is synchronized with a 250MHz reference frequency provided through the connector. The FPGA is also linked to board support functions such as temperature and current sensors, as well as an EEPROM with a unique identifier assigned by the manufacturer during board construction. I²C and SPI are used to communicate with various peripheral devices. There is also the option to control tri-color LEDs, which is essential for easily locating a single machine in a server farm for maintenance purposes. Finally, the FPGA can be programmed using either a JTAG connector, which is useful for software debugging in the laboratory or a Quad SPI flash. The latter can be remotely modified over the PCIe interface, allowing for on-site updates.

## Trigger architecture

The ALICE trigger architecture is an amalgamation of multi-link technologies based on several protocol standards. It has been optimized to function in coherence with the surrounding blocks of the detectors, allowing the complete readout chain to operate synchronously and efficiently. The ALICE trigger architecture relies on the Trigger and Timing distribution System (TTS) ability to efficiently distribute the critical Timing and Trigger Control (TTC) information from the CTP to the readout electronics via the LTU and CRUs with constant latency over bi-directional TTC 10G-Passive Optical Network (PON) links. This allows the MID to be read out in continuous and triggered readout mode operations.

### 2.6.1 Central Trigger Processing

The CTP in the trigger architecture controls global trigger decisions and supervises the generation of trigger requests by integrating inputs from a set of trigger contributing detectors [12]. It is critical to recognize unusual occurrences and record them for later analysis. The CTP also generates periodic heartbeat (HB) triggers and customized software triggers for both continuous and triggered operations. It interacts with up to 24 LTUs, one of which is dedicated to MID.

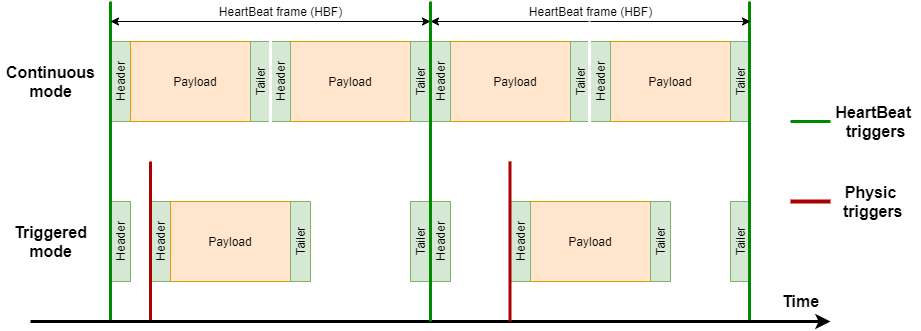
### 2.6.2 Local Trigger Unit

The LTU serves as an interface between the CTP and CRUs. It provides a clock, orbit, and external trigger inputs as well as allows monitoring and control using ethernet bus protocols. The LTU is a 6U VME-type board equipped with a Xilinx Kintect FPGA with 2 GB of DDR4 memory [13]. It has two running modes (global and stand-alone). In global mode, the LTU acts as a transparent interface between the CTP and the CRU. It converts signals and provides some online monitoring. Contrary, in the stand-alone mode, the LTU emulates the CTP protocol, allowing the MID team to perform tests, and calibration activities independently of the CTP, at remote sites, when the CTP is either unavailable or not necessary.

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### 2.6.3 Heartbeat

The heartbeat trigger is scheduled by the CTP to run with the highest possible priority and with a fixed period (89.4us). The heartbeat trigger is used by the readout electronics and CRU to verify whether its bunch crossing, orbit, and trigger counters are still synchronized. The amount of data collected between two HB triggers is called HeartBeat Frame (HBF). This HBF is generated by the CRU and used by O² systems for data segmentation, fault finding, and recovery procedures. The readout electronics cards in the MID readout chain are modified to handle this combination of physics and heartbeat triggers. Each regional/local card autonomously tags the data using the copy of the LHC Orbit and the bunch crossing id (BCID). For continuous mode, the payload data are sent as a continuous flow of successive frames each preceded with a header containing the time-based tagging. The triggered mode operates in the same way as the continuous mode with a few variations, it only sends a payload data block preceded with a header upon reception of physics triggers. Figure 2.8 shows how the physics and heartbeat triggers are used for the continuous and triggered readout modes.



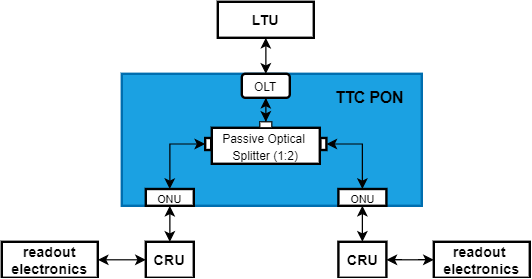
**Figure 2.8**: Continuous and triggered mode trigger configuration

### TTC 10G-PON

The TTC 10G-PON is a point-to-multipoint network architecture that uses optical splitters to enable an Optical Line Terminal (OLT) to interact with several Optical Network Units (ONUs). The TTC 10G-PON technology, as illustrated in Figure 2.9, allows the TTC message to be split among multiple CRUs of the readout chain using a single link. The TTC-PON downstream (CTP to CRU) and upstream (CRU-CTP) messages are described below.

* The TTC-PON downstream message is based on a 240-bit word transmitted synchronously with the LHC clock from CTP to the CRUs. The PON internally uses 40-bit, leaving 200-bits available for the sub-detectors use. The complete message is summarised in Table 2.4. The trigger type information is described in Table 2.5.
* Upon reception of an HB trigger, each CRU of the readout chain transmits the TTC-PON upstream message of 56 bits to the CTP, alternatively called HB acknowledge message (HBam). The HBam carries information about the CRU status illustrated in Table 2.6. The CTP collects the HBam from all CRUs acknowledging that data have been successfully collected.

|  |  |
| --- | --- |
| 2 | Readout chain |



**Figure 2.8:** TTC-PON architecture

**Table 2.4**: PON downstream message

|  |  |  |
| --- | --- | --- |
| **No. of Bit** | **Name** | **Description** |
| <31:0> | TType | Trigger Types data |
| <11:0> | BCID | Bunch crossing identification |
| <31:0> | Orbit | Orbit counter |
| <0:0> | TTValid | Trigger Type data valid |
| <7:0> | HBM header | Heartbeat message header |
| <31:0> | 1st ORBIT of TF/HBMTF | Heartbeat message time frame |
| <0:0> | HBMValid | Heartbeat meassage valid |

**Table 2.5**: Trigger Types

|  |  |  |
| --- | --- | --- |
| **Bit** | **Name** | **Description** |
| 0 | Orbit | Orbit flag |
| 1 | HB | HeartBeat flag |
| 2 | HBr | HeartBeat reject flag |
| 3 | HC | Health Check |
| 4 | PhT | Physics Trigger |
| 5 | PP | Pre Pulse Calibration |
| 6 | Cal | Calibration trigger |
| 7 | SOT | Start of Continuous |
| 8 | EOT | End of Continuous |
| 9 | SOC | Start of Triggered Data |
| 10 | EOC | End of Triggered Data |
| 11 | TF | Time Frame |
| … | … | Spare |
| 29 | TPCSync | TPC synchronization |
| 30 | TPCReset | TPC reset |
| 31 | TOF | TOF special trigger |

|  |  |
| --- | --- |
| 2 | Readout chain |

**Table 2.4**: PON upstream message

|  |  |  |
| --- | --- | --- |
| **No. of Bit** | **Name** | **Description** |
| <31:0> | HB id | Heartbeat identification |
| <9:0> | CRU id | CRU identification |
| <0:0> | CRU ack | CRU acknowledge bit |
| <1:0> | CRU status | CRU buffer status |
| <11:0> | Spare | Spare bits |

### MID trigger types

The TTC-PON trigger types contain usefull information to accommodate various sub-detector and not all triggers are used by the MID.

are compressed to be of HB triggers are envisaged, HB-accept (HBa) and HB-reject (HBr) depending on the status of CRUs. The HBa and HBr triggers will contain the HBid and a bit to signify whether it is an HBa or HBr. After receiving an HB trigger, each CRU will transmit an HB acknowledge message to the CTP, via their LTU. The payload of the message is defined in [8], table 7. The CTP will collect the HB acknowledge of all CRUs, within a time-frame of 8 Orbits and form an HB map.

**Table 2.4**: MID custom trigger format

|  |  |  |  |
| --- | --- | --- | --- |
| **MID**  **trigger type** | **CTP**  **trigger type** | **CRU message to**  **Readout electronics** | **FEE**  **trigger code** |
| SOx  (Start Of Run) | 9: SOC  7: SOT | Update internal ORBIT, BCID, bunch counter  Transmit command to all e-links  Reset event buffers  Start assembling events  Start sending events | 0x80 |
| EOx  (End Of Run) | 10: EOC  8: EOT | update internal Orbit, BCID & bunch counters  Transmit command to all e-links  Assemble last events  Send last events | 0x40 |
| TF  (TimeFrame) | 11: TF | Transmit command to all e-links | 0x20 |
| RUNNING  (Run status) | 14: RS | Transmit command to all e-links | 0x10 |
| CALIBRATE | 6: CAL | Update internal Orbit, BCID & bunch counters  Transmit command to all e-links | 0x08 |
| PHY | 4: PhT | Update internal Orbit, BCID & bunch counters  Transmit command to all e-links | 0x04 |
| RESET | 12: FEErst | Update internal Orbit, BCID & bunch counters  Transmit command to all e-links  Stop assembling events  Stop sending events | 0x02 |
| ORBIT | 0: ORBIT | Update internal Orbit, BCID & bunch counters  Reset internal MID's bunch counter  Transmit command to all e-links | 0x01 |

|  |  |
| --- | --- |
| 2 | Readout chain |

## 2.7 Online-Offline computing farm

The O² computer farm is composed of the First Level Processors (FLP) and Event Processing Nodes (EPN).

The ALICE reconstruction strategy consists of 2 phases: a first synchronous online reconstruction stage during data-taking enabling detector calibration, and a posterior calibrated asynchronous reconstruction stage.

The global architecture of the online system as presented in the upgrade LoI

### 2.7.1 First Level Processor

The FLP (DELL POWEREDGE R740) exchanges information with the FEE via the CRU, it can host a maximum of two CRUs. The FLP communicates with the EPN through a 100 Gb InfiniBand network.

### 2.7.2 Event Processing Node

|  |  |
| --- | --- |
| 2 | Readout chain |

## 2.8 Detector control system

The readout electronics are monitored and controlled by the ALICE DCS. The DCS system accesses the readout electronics via the FLP and CRUs through a network connection. The main protocol considered for communication between the CRU and DCS is called Alice Low-Level Front-end (ALF) on the CRU side and Front-End Device (FRED) on the DCS side. In the current readout chain implementation, the ALF can read/write registers implemented on the readout electronics cards modules and publish the data using a Distributed Information Management System (DIM) service.

The DIM is a communication system for distributed/mixed environments, originally developed for one of the experiments of the Large Electron-Positron Collider, an earlier particle accelerator at CERN. It provides a network transparent inter-process communication layer. The FLP host computer runs a DIM server, which acts as a bridge between the DIM network and the CRU driver, allowing DCS to communicate with the CRU from the control center without physical access to the CRU host computer.

|  |  |
| --- | --- |
| 2 | Readout chain |

## 2.9 References