**Chapter 2**

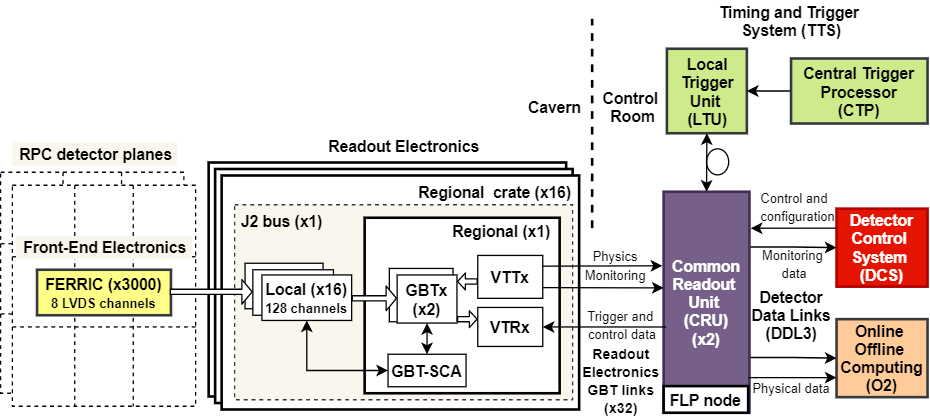
# Muon identifier readout chain

The transition from MTR to MID during the LS2 entails,

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| 2 | Readout chain |

## 2.1 Overview

The readout chain block diagram is shown in Fig. 2.1. The readout chain consists of 21 000 strips connected to 72 RPC detectors spread over multiple front-end electronics cards equipped with one or two FEERIC ASICs [ ]. The strip pattern signals from the FEERICs are propagated to the readout electronics, acting as the readout interface and in charge of the first stage of the trigger decision. The readout electronics are mounted on the upper gangways a little further away from the stations, where the radiation is low. The beam collisions will produce a lot of radiation in the area around ALICE in the cavern, therefore the readout electronics regional cards are equipped with Gigabit Transceiver (GBT) radiation hardening to operate properly. The CRUs combine and multiplex data from multiple readout electronics cards as well as timing and trigger information from the Timing and Trigger system (TTS) before transmission to the O² computing facility for processing and storage in the next layer of the readout chain. The CRUs are mounted in computers housed in the intermediary computer room, called the counting room, away from the ALICE cavern and thus do not require radiation hardening, as is the case for the readout electronics. These computers can be reached over the network from the main Detector Control System (DCS). The DCS manages the readout chain by sending commands and monitoring the system. Experimental data are moved from the FLP node to the O² computing system for processing and storage.



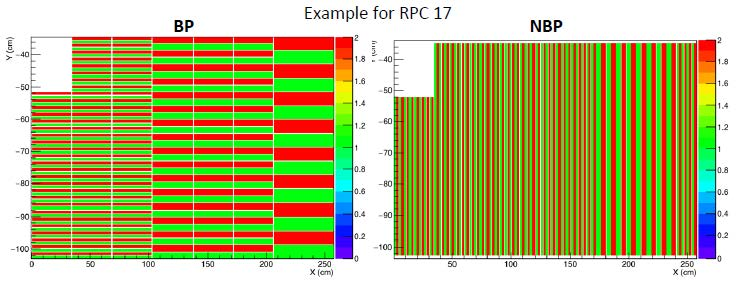
**Figure 2.1**: MID readout chain architecture

## 2.2 RPC detectors

In the ALICE cavern, three distinct forms of RPC are installed. They refer to long, short, and cut forms, respectively (Fig.2.3). The beam pipe is accommodated by the short-cut forms. The current RPCs are constructed with 2 mm wide gas gaps, 2 mm thick High-Pressure Laminate (HPL or bakelite) resistive electrodes, and polyamide insulation layers. The readout strips are made of copper and have three different pitch options: 1, 2, or 4 cm. Both RPCs have one collection of readout strips on each hand. The strips on either side of the RPCs are orthogonal to one another. In comparison to the dipole motion

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| 2 | Readout chain |

on charged-particle tracks, the vertical strips that have (y) hits are referred to as non-bending and the horizontal strips that have (x) hits are referred to as bending.



**Figure 2.2**: RPC strip patterns

Scientists predict an improvement in RPC hits in lead-lead collisions to exceed the highest counting rate of about 10 Hz/cm² up to 90 Hz/ cm², which is marginally similar to the maximum rated capacity of the sub-detector in the maxi-avalanche mode described in [ ]. This rise would also hasten the aging of the gas gaps, which will hit the end of their projected lifespan long before the end of Run 3, necessitating the replacement of certain gas gaps and other affected components.

These upgrades are distributed among three institutions. The Puricelli factory in Costa Masnaga (Italy) is responsible for redesigning the bakelite resistive electrodes, which feature a smoother surface for the bakelite used on the presently installed RPCs, the General Tecnica in Colli (Italy) is responsible for manufacturing the gas gaps for the new RPCs and, the National Institute for Nuclear Physics (INFN) in Torino (Italy) is responsible for checking and testing the performance of the new RPCs with cosmic rays. The installation of the new RPCs in the cavern is expected to start from July 2021, with the intent of installing 2 RPCs per day. In case of failure to meet this deadline, the MID will operate with the existing RPCs during Run 3 until the new RPCs are ready.

## 2.3 Front-End electronics

The RPC ADULT electronics have been replaced by a new ASICS named the Front-End Electronics Rapid Integrated Circuit (FEERIC) [ ] and unlike the ADULT, it amplifies the analog signals from the RPCs. The FEERIC is an 8-channel ASIC that uses low-cost AMS 0:35mm CMOS technology developed by the Laboratory of Physics Clermont-Ferrand. It is made up of a trans-impedance amplifier stage, a zero-crossing discriminator to limit time walk effects, and a one-shot to prevent retriggering during 100 ns and LVDS drivers. Table 2.1 summarizes the main specifications, and requirements of the FEERIC ASIC. In contrast to the ADULT card thresholds, which were set using an analog voltage distribution of just one threshold value per RPC, the FEERIC card thresholds would be set wirelessly during Run 3. Their values will be assigned to each card, allowing one to fine-tune the

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threshold based on the local RPC efficiency while minimizing operating high voltage. The technology selected to accomplish this task is the ZIGBEE protocol. It is a wireless technology established as an open universal norm to meet the special requirements of low-cost, low-power wireless IoT networks based on the IEEE 802.15.4 physical radio interface and works in unlicensed bands such as 2.4 GHz. The ZEGBEE is incorporated on the Atmel SAMD21 microcontroller and the program is based on Arduino libraries (I2C, SD cards, and Xbee module). This is then put onto a printed circuit board called the Xbee cards. The master cards are linked to the DCS PC using ethernet, and the ZIGBEE (wireless) protocol is used to communicate from master to nodes.

**Table 2.1**: Requirements of the FEERIC ASIC [ ]

|  |  |
| --- | --- |
| feature | value or type |
| pulse polarity | positive or negative |
| # of channels | 8 |
| power consumption per channel | < 100 mW |
| input impedance | < 50 W |
| dynamic range | 20 fC < q < 3 pC |
| time resolution | < 1 ns |
| time walk | < 2 ns |
| one-shot | 100 ns |
| output format | LVDS |
| signal shape | square pulse 23±3 ns |

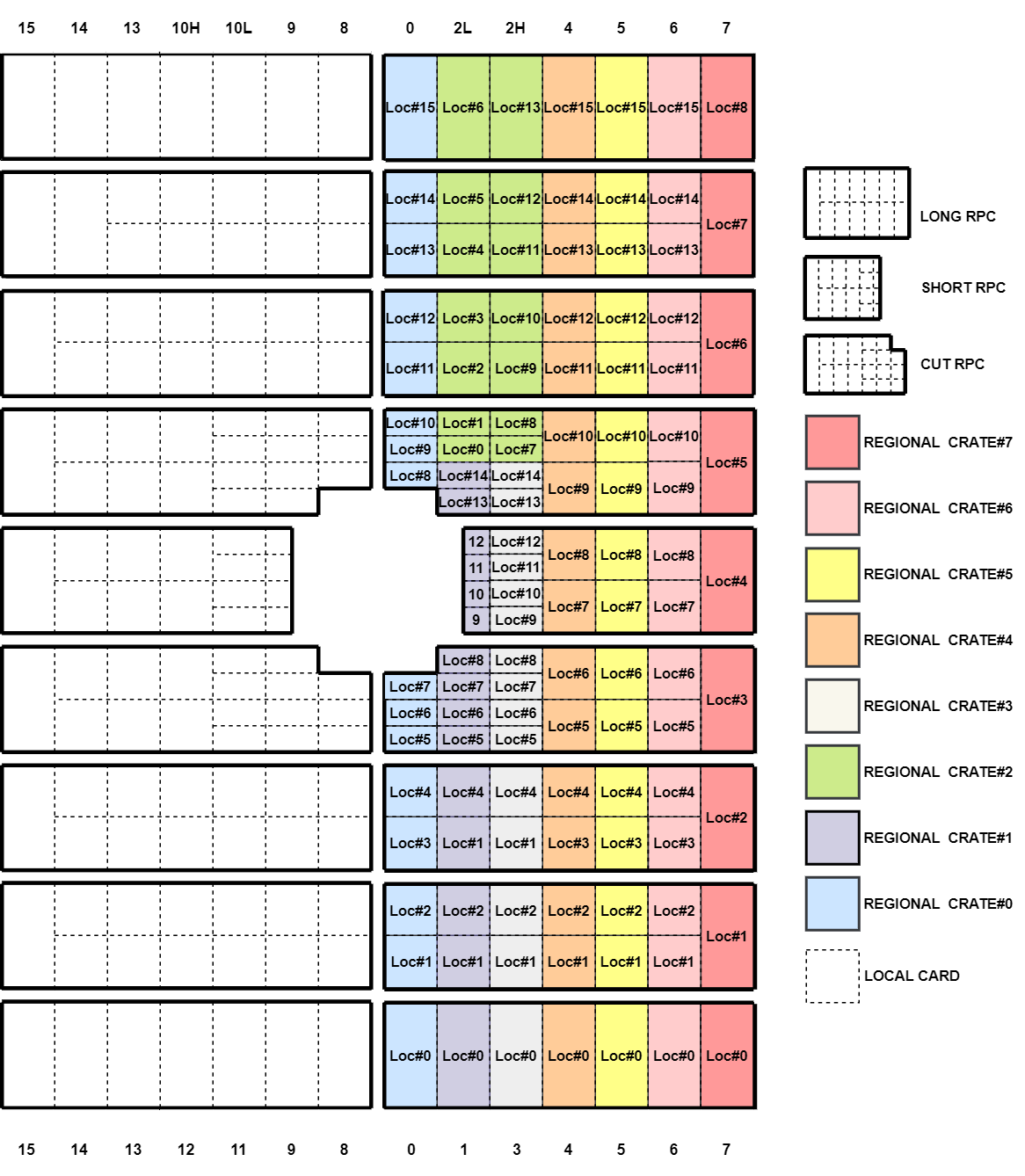
As previously mentioned, the charge delivered within the gas gaps must be lowered to minimize aging and improve rate capabilities. This is achieved by operating RPCs with the same gas mixture but at a lower gain, in conjunction with new FEERIC ASICs which perform amplification of the analog signal before discrimination. So far, 2384 + 336 spares FEERIC cards and 26 Xbee cards have been manufactured and installed in the ALICE cavern. The installation and commissioning of all FEERIC and Xbee cards concluded in July 2019 [ ].

## 2.4 Readout electronics

To cope with the new readout rates, the local and regional readout cards have been redesigned. Since the triggering functionalities are abandoned, a more streamlined approach has been introduced. The hardware implementation of the regional and local card is almost identical, minimizing the design and development effort by re-using the same hardware and altering the FPGA firmware. The global crate has been replaced by a new regional crate.

As shown in Fig 2.3, the readout electronics are divided into 16 vertical regions (8 on the left and 8 on the right side of the plane). Each vertical region is read out by a single regional crate. Each contains a backplane bus card called the J2 card, which connects to a single regional card and up to 16 local cards.

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**Figure 2.3**: Geometry of the readout electronic

### 2.4.1 Local card

For every bunch crossing, the local card receives binary data from LVDS channels, which indicates whether the corresponding channel has been struck or not. The local card is equipped with 16 LVDS input connectors (32 pins, for both the BP and NBP ). It is embedded with the Intel MAX 10 FPGA (10M50DCF484C7G). Its FPGA firmware is described here []

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### 2.4.2 J2 bus card

The J2 bus card serves as an interface between the regional crate and the local/regional cards in terms of power, and it also serves as an interface between the local and regional cards in terms of data transfer. The J2 bus card has a 4-bit dip switch for assigning a specific identification to the regional crate, as well as three LEDs for monitoring the voltages (2.5V, 3.3V, and 5V) supplied to the regional and local cards.

### 2.4.3 Regional card

The regional card collects data from up to 16 local cards using the GBT protocol, which is discussed in the next section. Similar to the local card, the regional card is incorporated with the same Intel MAX 10 FPGA. However, unlike the local card, it is equipped with two bi-directional GBT optical links allowing transmission and reception of data to/from the CRU. The implementation of 2 GBT optical links per regional card enables complete regional crate data transfer. The firmware implemented in the regional card FPGA is a slightly modified version of the local card firmware, which is also described in [].

### Event data formats

Events are stored in the local and regional card multi-buffers for each trigger. The multi-event buffer in the local card carries strip patterns, therefore it is larger than the regional card. The event data formats of the local card and regional card are shown in Tab.2.2 and Tab.2.3 accordingly.

**Table 2.2**: Local event format [ ]

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| *Coding of*  *SOx, EOx, RESET, CALIBRATE*  *Event in LOCAL* | *Bits* |  | *Coding of*  *PHY, ORB*  *Event in LOCAL* | *Bits* |  | *Coding of*  *self-triggered DATA*  *Event in LOCAL* | *Bits* |
| START BIT (always '1')  CARD TYPE (always '1'=LOCAL)  LOCAL BUSY ('0'=OK; '1'=FIFO full)  LOCAL DECISION (tracklet)  ACTIVE ('0'=OFF; '1'=ON)  REJECTING ('0'=OFF; '1'=ON)  MASKED ('0'=OFF; '1'=ON)  OVERWRITED ('0'=OFF; '1'=ON) | 1  1  1  1  1  1  1  1  1 | START BIT (always '1')  CARD TYPE (always '1'=LOCAL)  LOCAL BUSY ('0'=OK; '1'=FIFO full)  LOCAL DECISION (tracklet)  ACTIVE ('0'=OFF; '1'=ON)  REJECTING ('0'=OFF; '1'=ON)  MASKED ('0'=OFF; '1'=ON)  OVERWRITED ('0'=OFF; '1'=ON) | 1  1  1  1  1  1  1  1  1 | START BIT (always '1')  CARD TYPE (always '1'=LOCAL)  LOCAL BUSY ('0'=OK; '1'=FIFO full)  LOCAL DECISION (tracklet)  ACTIVE (always '1'=ON)  REJECTING (always '0'=OFF;)  MASKED ('0'=OFF; '1'=ON)  OVERWRITED ('0'=OFF; '1'=ON) | 1  1  1  1  1  1  1  1  1 |
| SOx  EOx  PAUSE (always '0')  RESUME (always '0')  CALIBRATE  PHY (ignored)  RESET  ORB | 1  1  1  1  1  1  1  1 | SOx (always '0')  EOx (always '0')  PAUSE (always '0')  RESUME (always '0')  CALIBRATE (always '0')  PHY  RESET (always '0')  ORB | 1  1  1  1  1  1  1  1 | Always '0' | 8 |
| LOCAL bunch counter | 16 | LOCAL bunch counter | 16 | LOCAL bunch counter | 16 |
| LOCAL board position in Crate (0-15) | 4 | LOCAL board position in Crate (0-15) |  | LOCAL board position in Crate (0-15) |  |
| Status: "0xF" | 4 | Always '0' |  | Data: detector plane(s) (1 bit / plane) |  |
| Status: Mask registers (SOx=’1’|EOx=’1’)  Data: all strip patterns (not masked)  [(X4, Y4), (X3, Y3), (X2, Y2), (X1, Y1)] | 32\*4 | N/A | 0 | Data: Only masked strip pattern(s)  [(X4, Y4), (X3, Y3), (X2, Y2), (X1, Y1)] | 32\*i |
| Total number of bits |  | Total number of bits | 40 | Total number of bits | 8\*bc |
| Bunches needed to send |  | Bunches needed to send | 5 | Bunches needed to send | 9 - 21 |

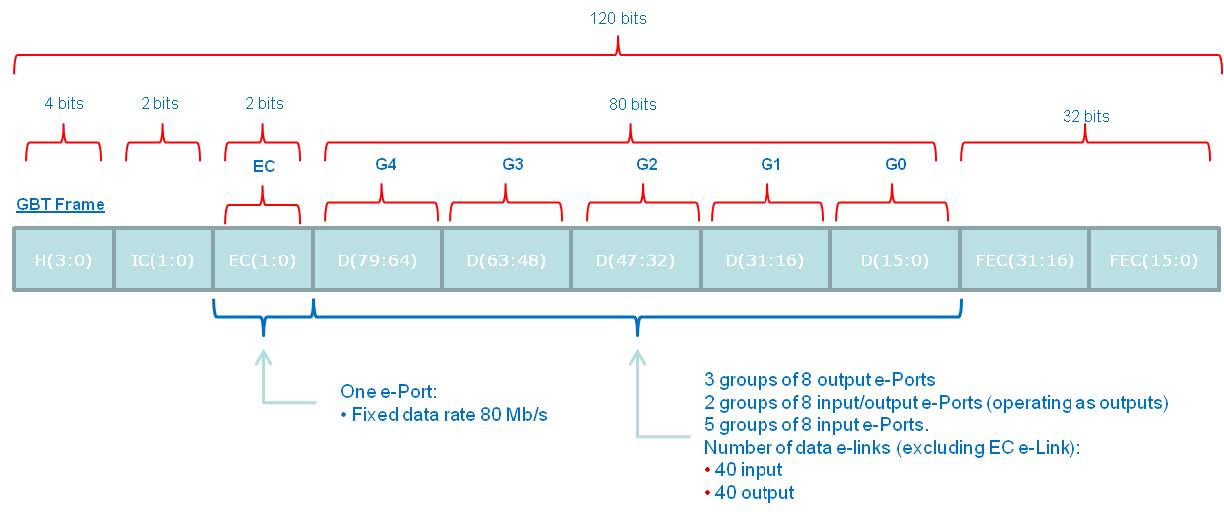
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**Table 2.3**: Regional event format [ ]

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| *Coding of*  *SOx, EOx, RESET, CALIBRATE*  *Event in REGIONAL* | *Bits* |  | *Coding of*  *PHY, ORB*  *Event in REGIONAL* | *Bits* |  | *Coding of*  *self-triggered DATA*  *Event in REGIONAL* | *Bits* |
| START BIT (always '1')  CARD TYPE (always '1'=LOCAL)  LOCAL BUSY ('0'=OK; '1'=FIFO full)  LOCAL DECISION (tracklet)  ACTIVE ('0'=OFF; '1'=ON)  REJECTING ('0'=OFF; '1'=ON)  MASKED ('0'=OFF; '1'=ON)  OVERWRITED ('0'=OFF; '1'=ON) | 1  1  1  1  1  1  1  1  1 | START BIT (always '1')  CARD TYPE (always '1'=LOCAL)  LOCAL BUSY ('0'=OK; '1'=FIFO full)  LOCAL DECISION (tracklet)  ACTIVE ('0'=OFF; '1'=ON)  REJECTING ('0'=OFF; '1'=ON)  MASKED ('0'=OFF; '1'=ON)  OVERWRITED ('0'=OFF; '1'=ON) | 1  1  1  1  1  1  1  1  1 | START BIT (always '1')  CARD TYPE (always '1'=LOCAL)  LOCAL BUSY ('0'=OK; '1'=FIFO full)  LOCAL DECISION (tracklet)  ACTIVE (always '1'=ON)  REJECTING (always '0'=OFF;)  MASKED ('0'=OFF; '1'=ON)  OVERWRITED ('0'=OFF; '1'=ON) | 1  1  1  1  1  1  1  1  1 |
| SOx  EOx  PAUSE (always '0')  RESUME (always '0')  CALIBRATE  PHY (ignored)  RESET  ORB | 1  1  1  1  1  1  1  1 | SOx (always '0')  EOx (always '0')  PAUSE (always '0')  RESUME (always '0')  CALIBRATE (always '0')  PHY  RESET (always '0')  ORB | 1  1  1  1  1  1  1  1 | Always '0' | 8 |
| REGIONAL bunch counter | 16 | REGIONAL bunch counter | 16 | REGIONAL bunch counter | 16 |
| REGIONAL crate position (0-15) | 4 | REGIONAL position crate (0-15) | 4 | REGIONAL crate position (0-15) | 4 |
| Status: Mask registers (SOx=’1’| EOx=’1’)  Data: All tracklet inputs (not masked) | 4 | Always '0' | 4 | Data: detector plane(s) (1 bit / plane) | 4 |
| Total number of bits | 40 | Total number of bits | 40 | Total number of bits | 40 |
| Bunches needed to send | 5 | Bunches needed to send | 5 | Bunches needed to send | 5 |

### Gigabit Transceiver protocol

The GBT protocol architecture was created at CERN, for use in the LHC, which required high bandwidth as well as radiation protection [ ]. Embedded in the regional cards is a radiation-hardened ASIC known as GBTx (Fig.2.4). This ASIC contains a high-speed serializer and deserializer that takes data and then transmits them through a laser transmitter, as well as the reverse for the downlink. The laser transmitter utilized is a special component manufactured at CERN. The GBT optical link controller is implemented as a module in the CRU firmware as described later in Chapter 4. The GBT protocol operates in 3 different frame modes: standard GBT frame mode, wide frame mode, and 8B/10B frame mode. Fig.2.5 depicts the standard GBT frame mode used in the MID readout chain.

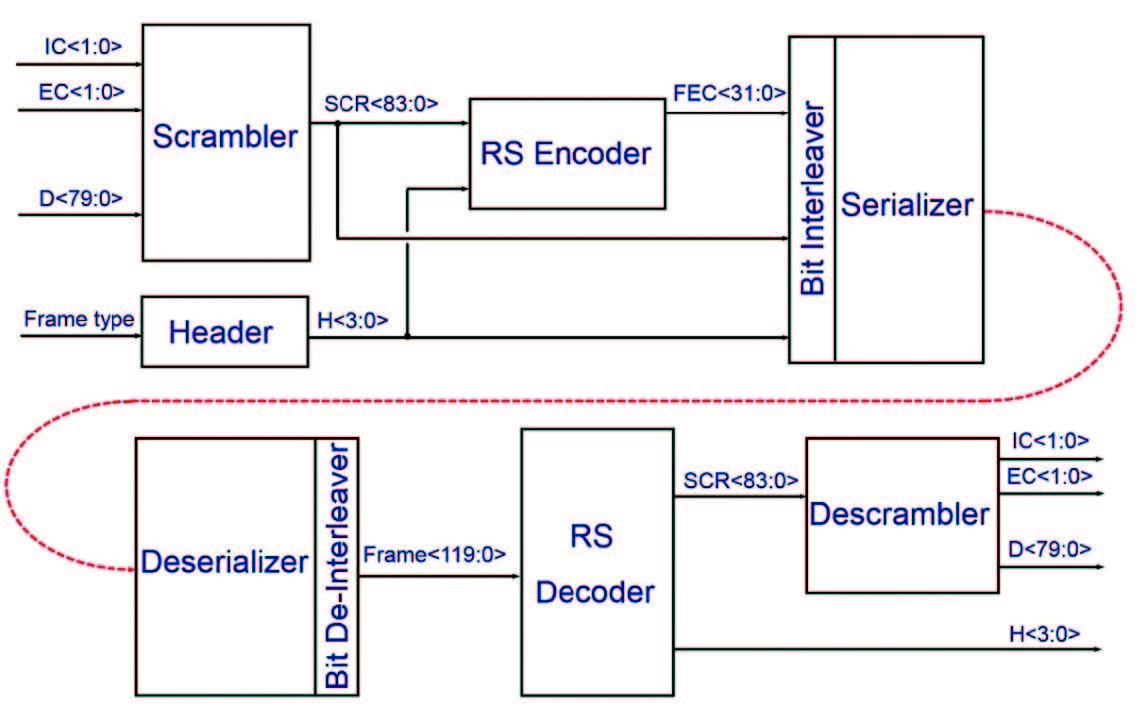


**Figure 2.4**: Block diagram of the standard mode GBT encoding and decoding. (to be changed later)

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| 2 | Readout chain |

The GBT frame shown above is continuously transmitted during a single LHC bunch crossing. It starts with a 4-bit header field, which is necessary for frame-level synchronization of the data stream. Recognizing multiple valid headers implies a proper frame-locking. The opposite implies that the frame synchronization has failed and the frame synchronization cycle must be initialized. The header field can either provide a value “0b0101” (data state), which indicates that the frame includes legitimate data, or “0b0110” (idle state), which indicates that the frame does not include valid data. Next is, a 4-bit used for slow control, the first two of which are for Internal Control (IC), which is reserved for controlling the GBTx ASIC. The last two slow control bits are for External Control (EC). The payload data and EC fields are not pre-assigned and are utilized for a variety of functions, including Data Acquisition (DAQ), Timing and Trigger Control (TTC), and experiment control, depending on the needs of the MID. The last 32 bits are utilized for forwarding Error Correction (FEC). The remaining 84-bit, which includes the EC, having an associated bandwidth of 3.36 Gb/s, of which 3.2 Gb/s is allocated to the payload data.

Before serialization, the data, EC, and IC fields are put through a scrambling process that balances them. In addition to the header, a Reed-Solomon (RS) encoder creates the 32-bit FEC based on the scrambled data. The deserializer does the opposite. Both scenarios are represented in Fig. 2.5.



**Figure 2.5**: Block diagram of the standard Mode GBT encoding and decoding. Adapted from [36]

The header is used to track frames and synchronize the receiver with the sender. The header is not affected by the scrambling therefore, it is easily detectable. When a GBT receiver is powered up, it enters a frame-lock initialization mode in which it searches for valid headers. After detecting a configurable number of frames with valid headers, it considers that the connection has been established and enters the frame tracking mode, in which it receives data and runs normally while searching for invalid headers.

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Once it is determined that a configurable number of consecutive frames is invalid, the synchronization is considered lost and the initialization mode is re-entered. This usually requires multiple invalid frames, so an accidental violation of a single random frame is not enough to cause channel synchronization. The data field (80 bits) of the GBT frame is used for data transmission. GBT frames are divided into control frames, data frames, and the header contains data valid only for the latter. The frame starts with a 4-bit identification header. Four headers are defined: IDLE, Start of Packet (SOP), End of Packet (EOP), and the Single Word Transaction (SWT). The IDLE frame does not contain any information. SOP and EOP, as the name suggests, mark the beginning and end of the detector data packet, which contains various packet-related metadata. The SWT frame contains any data used for a specific control or data transmission. On the GBT uplink, SWT frames are transmitted between data frames, that is, between EOP and SOP control frames. In the MID read chain, the SWT frame is used to access the register bus on the regional card.

The 2 bytes in the EC payload of the GBT frame are routed to a special slow control ASIC called GBT-SCA. As mentioned above, the chip is part of the regional card. The communications between the CRU and SCA are implemented in the CRU firmware architecture described in Chapter 3. The GBT-SCA ASIC has a large number of communication modules, including various GPIO, ADC, and DAC pins, as well as I²C, SPI, and JTAG master control [ ]. The communication between the regional FPGA and GBT-SCA is carried out through the high-level serial link control (HDLC) protocol. The protocol is based on commands. In contrast to the direct reading and writing of registers, the transaction contains the command ID, transaction ID, and data required by the command. The command ID indicates what the GBT-SCA chip will do, such as read or write registers or perform operations. Each command transaction returns a batch with the same transaction ID. The return package contains status information and returned data. The slow control IC is used for GBTx register access, configuration, and monitoring. This field can also control the laser transceivers that use the main communication modules on the GBTx chip, which can be accessed through its registers.

**E-links**

The GBTX chips on the regional cards communicate with the local cards using the standard GBT frame mode architecture. It consists of connecting the GBTX and the regional and regional FPGAs through duplex electrical serial lines (e-links). Each GBT bi-directional optical link of the readout chain is made up of 10 serial e-links (8 local e-links + 2 internal regional e-links).

Each of these e-links consists of three signal lines (differential pairs):

* Differential Clock line (dClk+/dClk-): Clock driven by GBTX to the local/regional FPGA
* Differential Downlink data output (dOut+/dOut-): Data from GBTX to the local/regional FPGA
* Differential Uplink data input (dIn+/dIn-): Data line from the local/regional FPGA to GBTX

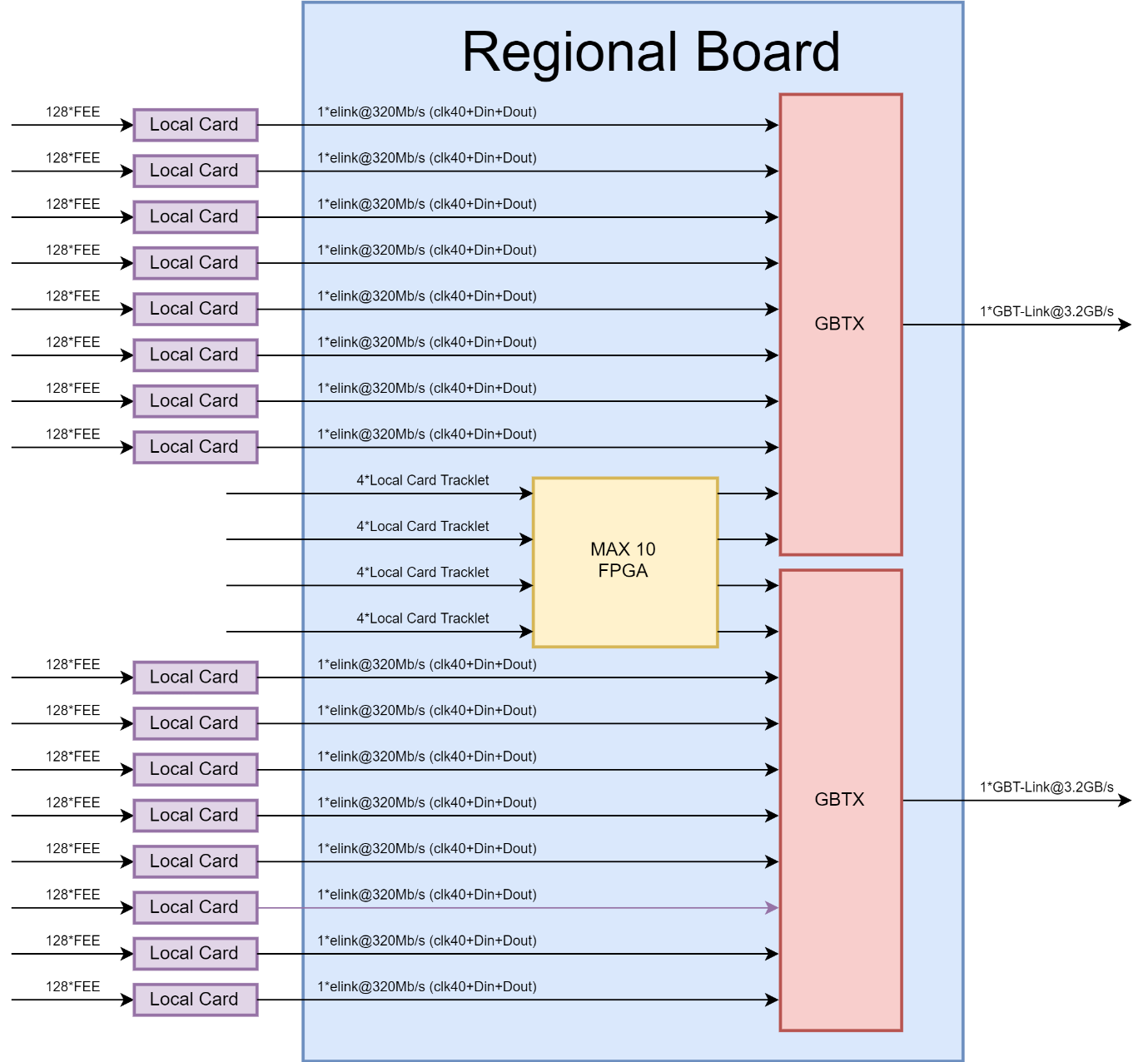
Fig. 2.6 represents the standard GBT frame mode topology between the GBTX chip and the readout electronics using e-links.

The maximum data rate in the e-links is 320 Mb/s, with a maximum of 2 e-links per group. As mentioned earlier, each e-link is composed of one differential clock line (dClk+/dClk-), one differential downlink output (dOut+/dOut-), and one differential uplink input (dIn+/dIn-). Thus, the maximum number of differential e-link signals per group is 3 x 2 = 6, equivalent to 6 signal pins per group. Overall, a total of 6 x 5 = 30 configuration pins are dedicated to the e-links.

To provide the greatest possible signal quality and transmission reliability, the physical e-link connections are assumed to be differential transmission lines with a differential impedance of 100 Ω and a suitable termination line at the receiver end.

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The e-link receivers have built-in 100 Ω terminations that can be disabled if necessary. The e-link signal drivers and receivers that are not being utilized in the readout chain are shut off to minimize the power consumption (I/O power is a significant part of the total GBTx power consumption).

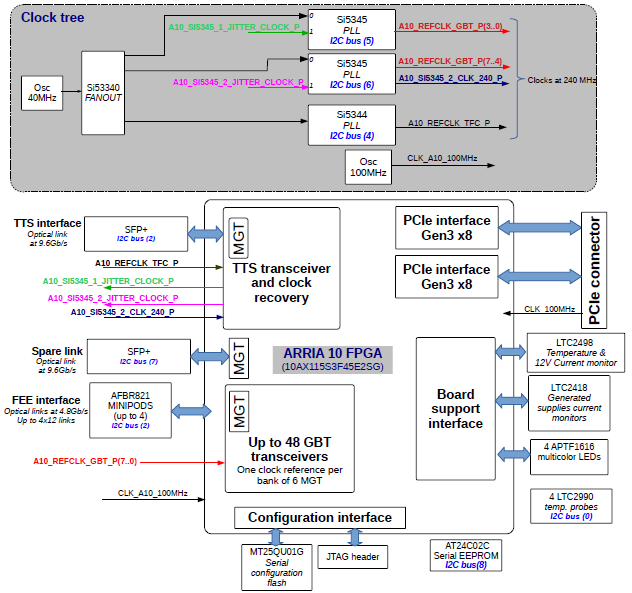


**Figure 2.6**: Geometry of the readout electronics (to be changed later)

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## Common readout unit

The ALICE CRU hardware architecture described in [ ] is shown in Fig. 2.7. Besides the PCIe interface, which utilizes a built-in 100 MHz crystal oscillator, the clock tree is designed to utilize a single reference clock for all CRU communication links. The CRU board can either be used independently with a built-in 40MHz crystal oscillator or with a recovered clock retrieved from the TTS optical link. On the other hand, the TTS transceiver requires a constant 240 MHz reference frequency before initialization, which is generated locally with the help of a Phase-Locked Loop (PLL) SI5344. The clock recovered from the FPGA is transferred to a high-performance SI5345 PLL for jitter attenuation after it has successfully been locked to the incoming stream. The cleaned clocks are then utilized to run the FPGA logic. The SI5345 PLL uses I²C communication to switch between local and recovered clock modes. The clock generated from the built-in 100 MHz crystal oscillator is utilized to run many features of the FPGA, including initialization and hardware monitoring.



**Figure 2.7**: a functional overview of the hardware, highlighting the functions used in the CRU.

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| 2 | Readout chain |

CRU is integrated in Intel ARRIA10 FPGA (10AX115S3F45E2G). It is equipped with two Small Form-factor Pluggable (SFP+) connections. Only one of the two SFP modules is used for TTS connection, and the other is used as a backup. The connections from/to the readout electronics are ensured by up to 4x12-channel bi-directional 10.3125 Gb/s optical transceivers (mini-pods)[ ]. These two mini-pods can connect to up to 24 GBT links. However, for what concerns the MID, 32 GBT links are required to transfer data from the complete readout electronics. Hence, 2 CRUs are utilized, each connected to 16 GBT links.

The CRU is connected to a PCIe edge connector on the rear end and provides a dual gen3 x8 PCIe interface. This interface is synchronized with a 250MHz reference frequency provided through the connector. The FPGA is also linked to board support functions such as temperature and current sensors, as well as an EEPROM with a unique identifier assigned by the manufacturer during board construction. I²C and SPI are used to communicate with various peripheral devices. There is also the option to control multi-color LEDs, which is essential for easily locating a single machine in a server farm for maintenance purposes. Finally, the FPGA can be programmed using either a JTAG connector, which is useful for software debugging in the laboratory or a Quad SPI flash []. The latter can be remotely modified over the PCIe interface, allowing for on-site updates.

## Timing and trigger architecture

### 2.6.1 Central Trigger Processing

For the triggered ALICE operation, the CTP system produces trigger signals (LM, L0, L1) with several latencies derived from the input trigger signals provided by the trigger detectors [ ]. For both the continuous and triggered operation the CTP produce the periodic heartbeat (HB) trigger and specific software triggers. All trigger types provided by the CTP are sent via the LTUs and the TTS to the detector read-out systems. The CTP system will assemble and evaluate the HB acknowledge messages sent from the CRUs to the CTP which will include the HB ID so that the CTP can assemble a complete HB map. This HB map represents the HBF data transmission and CRU buffer occupancy status of all the CRUs for each HBF. This HB map will be part of the CTP read-out to the O2 system. The implementation does not require additional hardware, as the acknowledge message is sent via the bi-directional high bandwidth timing and trigger distribution (TTS) link from the CRU to the CTP. It needs to be defined whether for some detectors the granularity of the HB acknowledge message needs to be increased to more than one bit per CRU. In case the HB map evaluation gives a too high number of incomplete HBF the CTP can act automatically or manually as described in Section 3.

### 2.6.2 Local Trigger Unit

The Local Trigger Unit combines the functions of transmission of trigger signals and emulation of the CTP for use in detector development. The LTU sends trigger signals to sub-detectors via the GBT or the TTC protocol. For the GBT there will be ten separate bi-directional GBT links that can also be used for upstream BUSY collection. In the TTC case, the LTU optical links will provide the optical signal according to TTC protocol, and BUSY is propagated by dedicated LVDS cables. In addition, there will be provision for a clock, orbit, and external trigger inputs. Monitoring and control will be provided by a 1Gb/s optical Ethernet link using the bus protocol.

## 2.7 Online Offline computing farm

The O2 facility is a computer farm composed of the First Level Processors (FLP) and Event Processing Nodes (EPN).

### 2.8.1 First Level Processor

The FLP (DELL POWEREDGE R740) [] exchanges information with the FEE via the CRU, it can host a maximum of three CRUs. The FLP communicates with the EPN through a 100 Gb InfiniBand network.

### 2.8.2 Event Processing Node

## 2.8 Detector control system

The MID readout processes are monitored and controlled by the ALICE DCS. The DCS system accesses the readout electronics via the FLP and CRUs through a network connection.

One of the protocols considered for the communication between the CRU and DCS is called ALF (On the CRU side) and FRED (On the DCS side). This protocol is based on Distributed Information Management System (DIM). DIM is a communication system for distributed/mixed environments, originally developed for one of the experiments of the Large Electron-Positron Collider, an earlier particle accelerator at CERN[14]. It provides a network transparent inter-process communication layer. The FLP host computer runs a DIM server, which acts as a bridge between the DIM network and the CRU driver, allowing DCS to communicate with the CRU from the control center without physical access to the CRU host computer.

The DCS data is extracted from the data stream and sent to the ALF (Alice Low-Level Front-end) interface, which publishes the data to the upper layers of the software. ALF can also receive commands and converts them to data words to be sent to the front-end electronics. To keep the ALF detector neutral, its functionality is restricted to the basic I/O operations. In the current implementation, the ALF can read/write registers implemented on the front-end modules and publish the data using a DIM service. The data published by ALF could be single values or blocks of data prepared by the electronics modules.

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| 2 | Readout chain |

## 2.9 References