**Chapter 3**

# CRU common firmware

The upgrade of the electronics allows one to increase the data to a value of about two orders of magnitude larger than the one that ALICE experienced during LHC RUN1 and RUN2. As mentioned above, one of the main goals of the new data campaign is the study of rare probes down to low transverse momenta, a region where the large background makes the triggering techniques very inefficient or even impossible in many situations. Such increase of data size, combined with the high collision and acquisition rates, makes standard approaches difficult to apply without enormous (technical and economical) efforts for the upgrade of computing capabilities. Since the required scaling of computing infrastructure cannot cope with the data throughput increase, a new acquisition and processing paradigm had to be developed. The basic idea is to reduce the data size as early as possible in the stream that goes from the sub-detector to the storage and reconstruction (Fig. 4.1). This goal can be achieved adding pre-processing and reconstruction layers close to the detector acquisition logic. For example, some detectors will be equipped with a zero-suppression algorithm to reduce the volume of data without losing useful information. Such fast reconstruction will be performed synchronously with the data acquisition and will be based on preliminary calibration and alignment information. Thanks to this fast and partial reconstruction the amount of stored data will be reduced. This procedure will replace the hardware trigger, allowing one to perform precise selections focused on getting the maximum signal for rare and otherwise non-triggerable observables.

This chapter gives a more in-depth description of the design and development of the user logic firmware.

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| 2 | MID readout chain |

**Data extraction**

Data transmitted from the readout electronics are forwarded to the user logic via the CRU common firmware. The transmission of data from the CRU and the user logic is done using the GBT interface. The

This interface works at 240MHz

Support at the same time (user configurable via avalon bus) the wide bus, the GBT format and raw format. It is a dynamic switching.

It is scalable. A design can links from 0 to 48 GBT links. The position of the GBT links can be controlled.

Decoder

Control

Monitoring

**Data reformat**

E-Link multiplexer

Packetizer

Quantifier

**Data transmission**

Transmitter

Header

**GBT user logic multiplexer**