**Chapter 4**

# Design and development

The basic idea is to reduce the data size as early as possible in the stream that goes from the sub-detector to the storage and reconstruction (Fig. 4.1). This goal can be achieved by adding pre-processing and reconstruction layers close to the detector acquisition logic. For example, some detectors will be equipped with a zero-suppression algorithm to reduce the volume of data without losing useful information. Such fast reconstruction will be performed synchronously with the data acquisition and will be based on preliminary calibration and alignment information. Thanks to this fast and partial reconstruction the amount of stored data will be reduced. This procedure will replace the hardware trigger, allowing one to perform precise selections focused on getting the maximum signal for rare and otherwise non-triggerable observables. This chapter gives a more in-depth description of the design and development of the user logic firmware.

The major objective is to minimize data size as early in the stream as feasible, from the sub-detector through storage and reconstruction. This may be accomplished by incorporating pre-processing and reconstruction layers close to the sub-detector acquisition logic. Some detectors, for example, will be outfitted with a zero-suppression algorithm to minimize data volume while retaining important information. This kind of quick reconstruction will take place in tandem with data capture and will be based on preliminary calibration and alignment information. The quantity of data retained will be decreased as a result of this quick and partial rebuilding. This technique will take the place of the hardware trigger, allowing for precise choices aimed at obtaining the highest signal for uncommon and otherwise non-triggerable observables. This chapter goes into further detail about the design and development of the user logic firmware.

The nominal DMA throughput provides a sufficient margin to collect data from the most demanding detector in ALICE, the MID. Each of the CRUs receives data from 16 GBT links as input for a total throughput of roughly 89.6 Gb/s. Unfortunately, the data must be aligned to a 32-bit word boundary, and therefore the actual throughput is 102.4 Gb/s. The incoming data are compressed by the MID user logic before being delivered to the DMA engine. The expected output of the TPC user logic is 20 Gb/s.

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| 2 | MID readout chain |