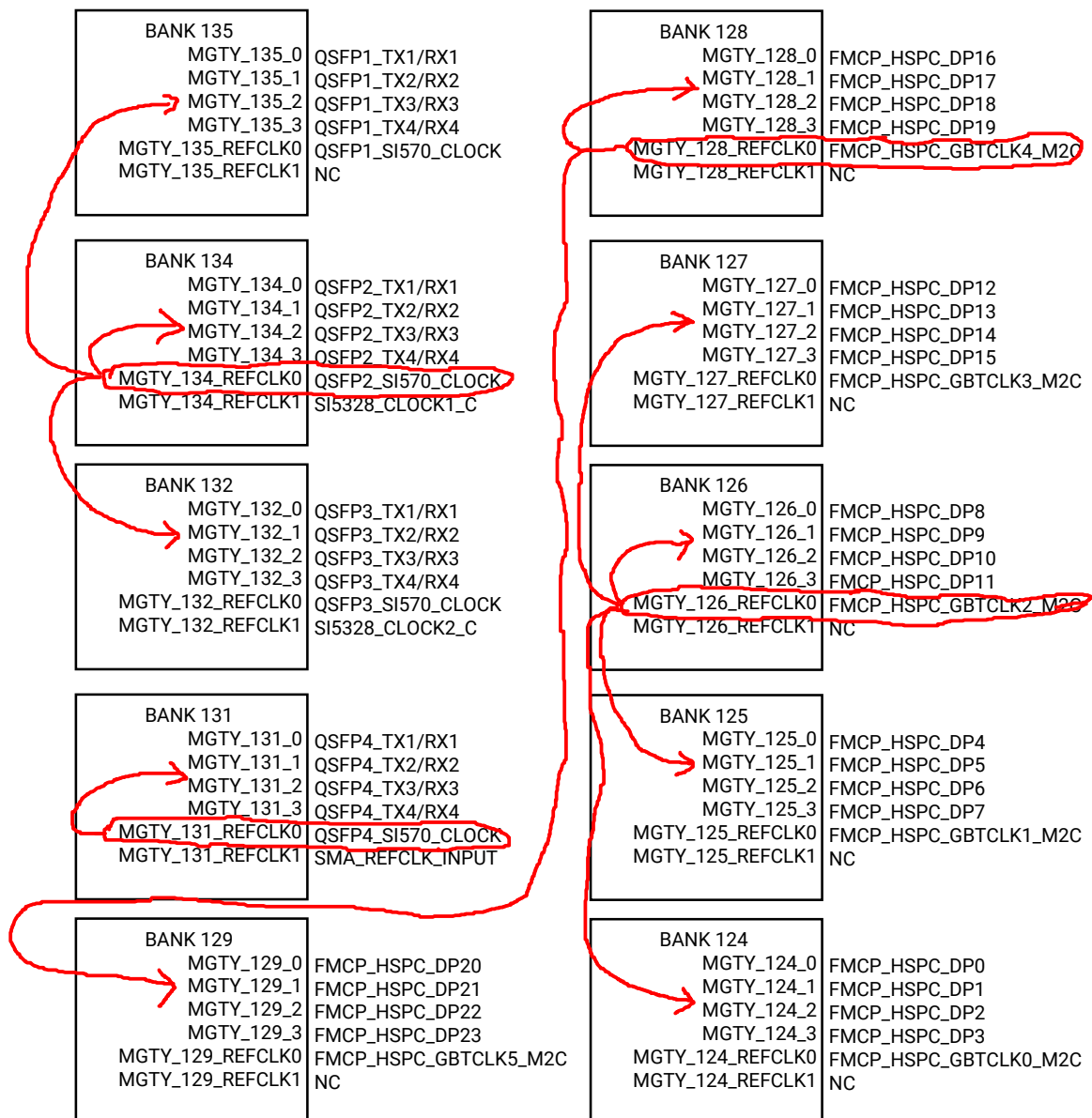


— = RX clock source (needs si570)
— = TX clock source (needs si528 jitter cleaner)

- Four GTY transceivers allocated to FMCP_HSPC_DP[0:3]

The XCVU37P right-side GTY transceiver interface assignments are shown in the following figure.

Figure 20: XCVU37P Right-side GTY Transceiver Assignments



X21650-092618

Right-side GTY Transceiver Connectivity

The following tables list the connectivity of the ten XCVU37P FPGA U1 right-side GTY transceivers.