USING THE Si5328 IN ITU G.8262-COMPLIANT SYNCHRONOUS ETHERNET APPLICATIONS

1. Introduction—The Si5328 and G.8262

The Si5328 is a Synchronous Ethernet (SyncE) PLL providing any-frequency translation and jitter attenuation for GbE, 10GbE, 40GbE, and 100GbE Carrier Ethernet switches and routers. The PLL loop filter is integrated on-chip as part of the Si5328's DSPLL architecture, and the device supports G.813 EEC Option 1 and EEC Option 2 loop bandwidth requirements (<0.1 Hz to 10 Hz). When used in conjunction with a Stratum 3 TCXO, the Si5328 meets all frequency accuracy, jitter, wander, and holdover requirements listed in G.8262. This application note provides recommendations and guidelines for the TCXO.

The following documents provide additional support and can be downloaded from the Skyworks Solutions web site.

- Si5328 Data Sheet, Rev 1.0 or higher
- Si53xx Reference Manual, Rev 1.2 or higher
- AN775: Si5328 ITU-T G.8262 SyncE Compliance Test Report
- Si5328-EVB User's Guide

The following is a link to the Timing section of the Skyworks Solutions website:

https://www.skyworksinc.com/en/Products/Timing

2. Reference Oscillator Selection Criteria

Table 1 lists potential sources for 40 MHz TCXOs that can be used in conjunction with the Si5328. These TCXOs have been tested and/or reviewed by Skyworks Solutions. Since system requirements may vary, designers should consult with their oscillator suppliers to ensure that the oscillator meets their system requirements and G.8262 standards compliance. Note that the Si5328 evaluation board uses a Rakon 40 MHz model RTX7050A TCXO. Frequencies other than 40 MHz can also be supported. See the Si53xx Reference Manual, Rev 1.2 or higher, for more details. For more information, please contact Skyworks Solutions.

Table 1. 40 MHz TCXO Sources

Manufacturer	Description/Part Number	URL
AVX/Kyocera	KT7050B-400000 KW33T	http://global.kyocera.com/prdct/electro/product/timing/tcxo.html
Rakon	RTX7050A, 509768	http://www.rakon.com/products/families/tcxo
Rakon	RPT7050A, E6213LF	http://www.rakon.com/products/families/tcxo
Vectron	VT-803-0020-40M0000000	http://www.vectron.com/products/tcxo/vt-803.htm

3. Oscillator PCB Layout Guidelines

The Si5328 accepts a clipped sine wave, CMOS, or differential reference clock on the XA/XB interface. Most clipped sine wave and CMOS TCXOs have insufficient drive strength to drive a 100 Ω or 50 Ω load. For this reason, place the TCXO as close to the Si5328 as possible to minimize PCB trace length. In addition, ensure that both the Si5328 and the TCXO are both connected directly to the ground plane. A clipped sine wave is preferable to CMOS signaling because the clipped sine wave signal does not need to be attenuated before being connected to the Si5328 XA pin. Figure 1 shows the recommended method of connecting a clipped sine wave TCXO to the Si5328. Because the Si5328 provides dc bias at the XA and XB pins, the ~800 mV peak-peak swing can be input directly into the XA interface of the Si5328 once it has been ac-coupled. Because the signal is single-ended, the XB input is ac-coupled to ground. Figure 2 illustrates the recommended method of connecting a CMOS rail-to-rail output to the XA/XB inputs of the Si5328. The resistor network attenuates the rail-to-rail output swing to ensure that the maximum input voltage swing at the XA pin is less than 1.2 V pk-pk. The signal is ac-coupled before connecting it to the Si5328 XA input.

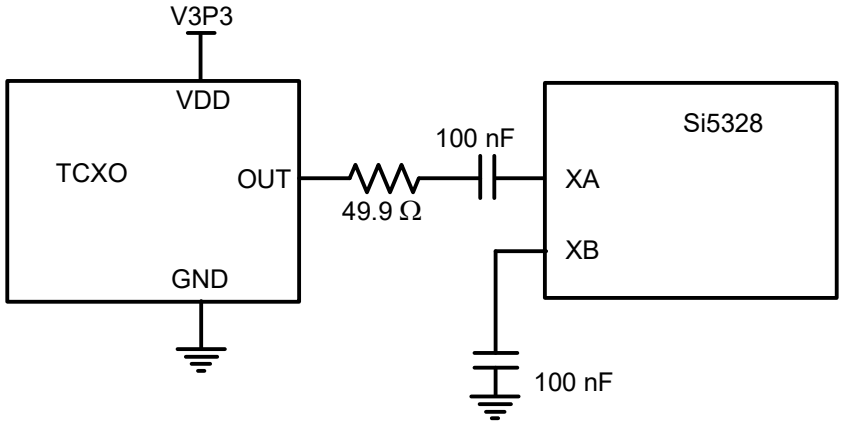

Figure 1. Clipped Sine Wave TCXO Output

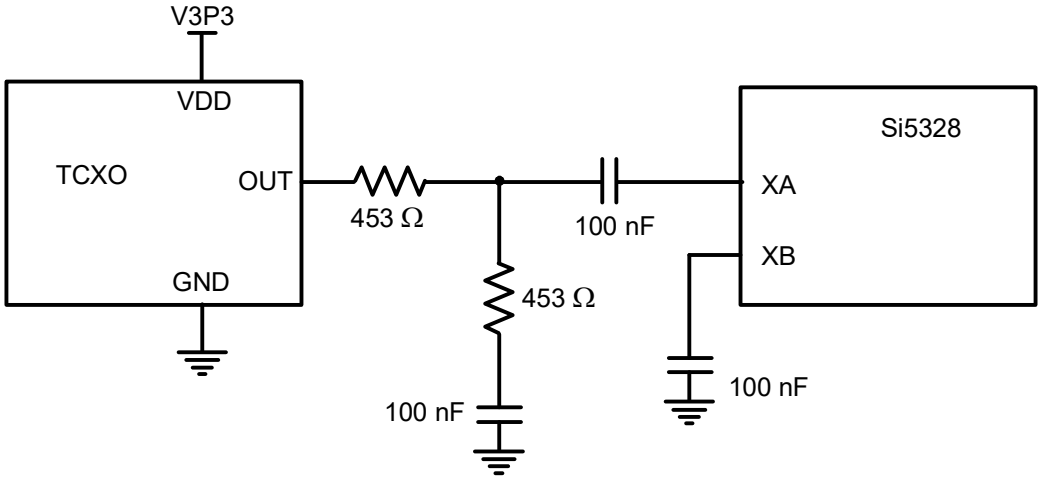

Figure 2. CMOS TCXO Output

4. G.8262 Compliance Testing

The Si5328 has been fully tested for compliance with G.8262 requirements. Table 2 summarizes the list of G.8262 requirements that pertain to SyncE PLLs, such as the Si5328. Jitter generation and jitter transfer are largely determined by the SyncE PLL. Wander generation and wander transfer are determined by a combination of the SyncE PLL and the TCXO. Wander transfer measurements also highlight the loop bandwidth of the PLL and its associated jitter peaking (<0.2 dB). Holdover performance is largely determined by the TCXO's frequency drift and short-term (24 hours) stability.

Note that some measurements must be taken over long periods of time (e.g. holdover). It is advisable to operate the test equipment with an uninterruptible power supply (UPS) because it isolates the equipment from powerline surges and glitches and ensures that short power interruptions do not force tests to be rerun from the beginning. See “AN775: Si5328 ITU-T G.8262 Synchronous Ethernet Compliance Test Report” for more details.

Table 2. G.8262 Sections by Measurement

Requirement	G.8262 Section
Frequency Accuracy	6
MTIE	8.1
TDEV	8.1
Wander Generation	8.1
Jitter Generation	8.3
Wander Transfer	10
PLL Loop Bandwidth (Peaking)	10
Long Term Phase Transient Response (Holdover)	11.2

5. TCXO Cover

In order to meet G.8262 stability and accuracy requirements, the overall stability and accuracy of the TCXO must be ±4.6 ppm over the temperature range of interest. Poor temperature stability will result in increased time deviation (TDEV) and maximum time interval error (MTIE) measurements. Because temperature stability is such an important issue, it is recommended that the TCXO be covered so that it is away from drafts and air flow from sources such as fans. An example of such a cover is Rakon part number PCV00015AA1. Figure 3 shows typical TDEV measurements taken with a TCXO cover, without a cover in still air, and without a cover with airflow. The units for both axes are in seconds.

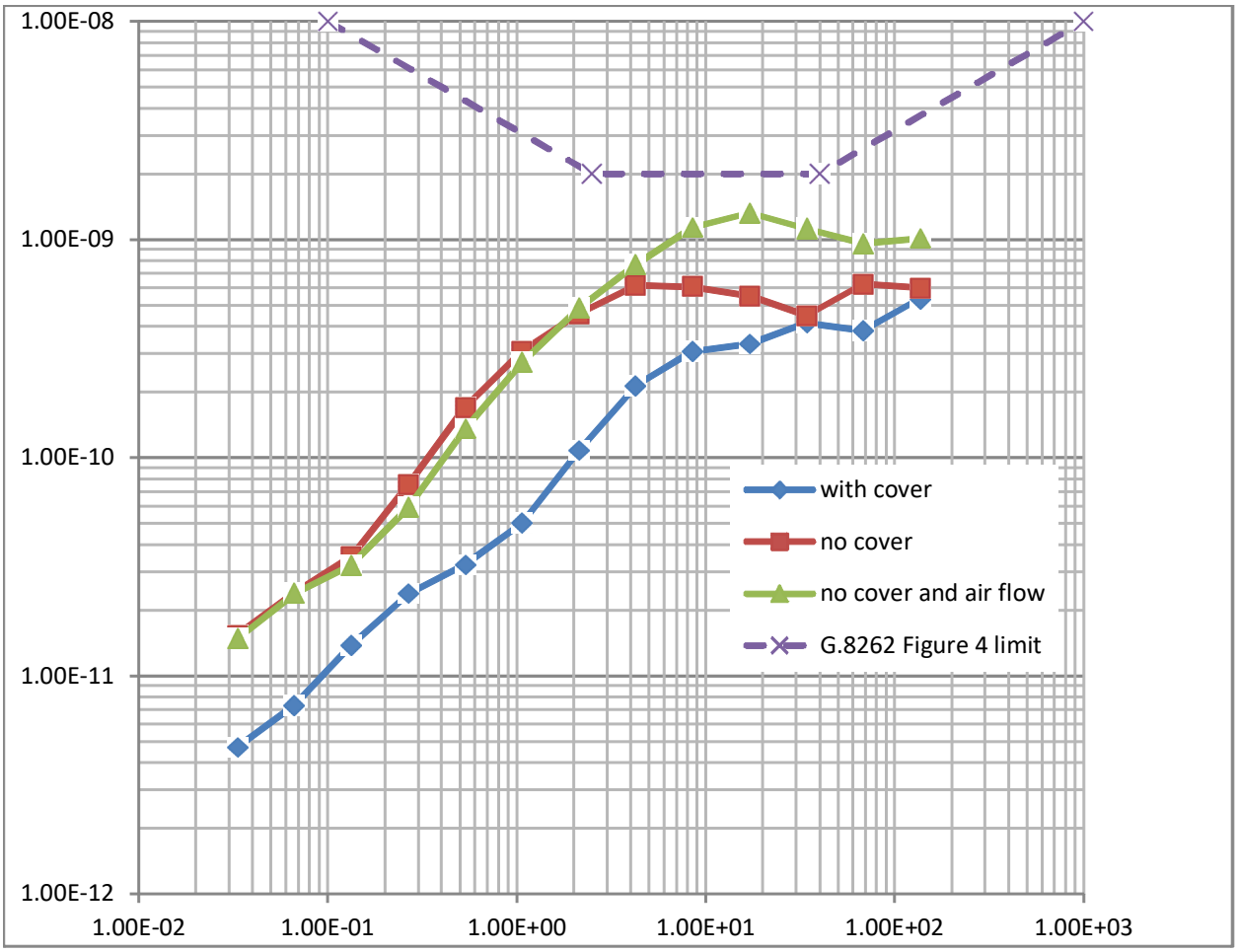

Figure 3. Typical Time Deviation Measurements

Figure 4 shows the same effect, but with a phase noise plot. The bold traces show the phase noise with a TCXO cover, and the upper, lighter, trace shows that the phase noise without the cover is higher for frequency offsets lower than 10 Hz. The TDEV and phase noise plots are consistent.

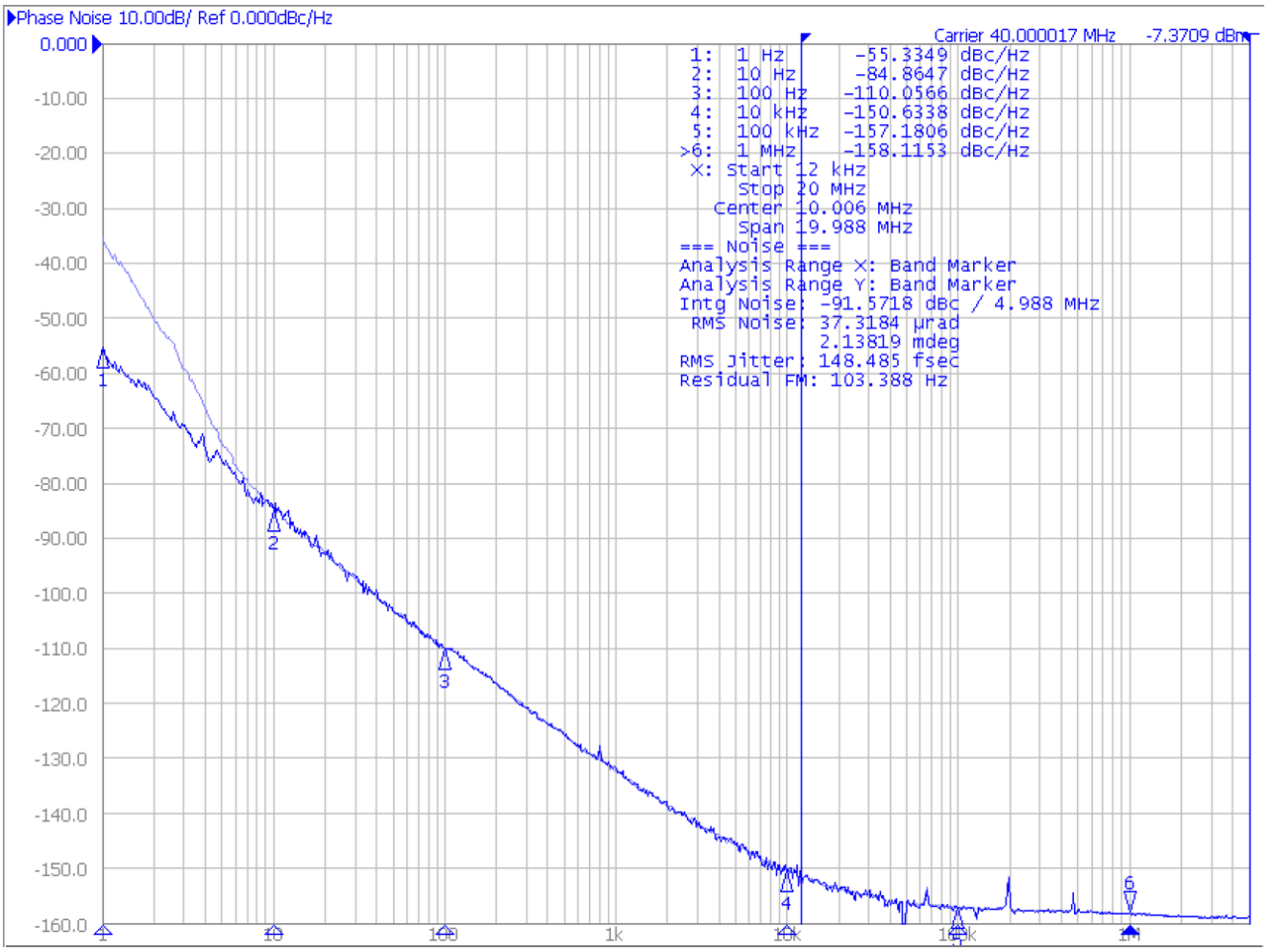

Figure 4. TCXO Phase Noise Plot (Cover vs. no Cover)

It is also important to be aware that TCXOs can be sensitive to shock and mechanical vibrations, and efforts should be made to minimize these factors.

6. Si5328 Lock Time Optimization

EEC Option 2 compliance requires a SyncE PLL with a 0.1 Hz loop bandwidth. Since PLL response time is inversely proportional to its loop bandwidth, SyncE PLLs generally require longer lock times than higher bandwidth PLLs. The Si5328 supports several features to minimize PLL lock time during normal operation:

1. The Si5328 supports a fast-lock feature that temporarily increases the loop bandwidth during lock acquisition to minimize overall lock time. Once the device has acquired lock, the Si5328 dynamically adjusts its loop bandwidth to the selected loop bandwidth (0.1 Hz to 10 Hz) for normal operation. Fast-lock is automatically enabled during internal calibration (ICAL, register bit 136.6) and during exit from holdover.
2. Fast-lock can be manually enabled to minimize lock time in other operating conditions, including:
    a. Input clock switch to a new, different frequency (<100 ppm difference between the old and new clock frequencies)
    b. Input clock frequency change without a clock switchover

For these applications, loss of lock (LOL) can be temporarily asserted to enable fast-lock. To manually assert LOL, two methods are available:

a. Set and immediately clear digital hold (DHOLD, register 3.5).
b. If there is a spare clock input, use manually-controlled input clock selection to select a clock input that is not connected and then immediately reselect the good clock source.

Document Change List

Revision 0.1 to Revision 0.2

- Fixed Vectron TCXO part number in Table 1.
- Add 50 Ω series resistor to Figure 1.

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