1. Description

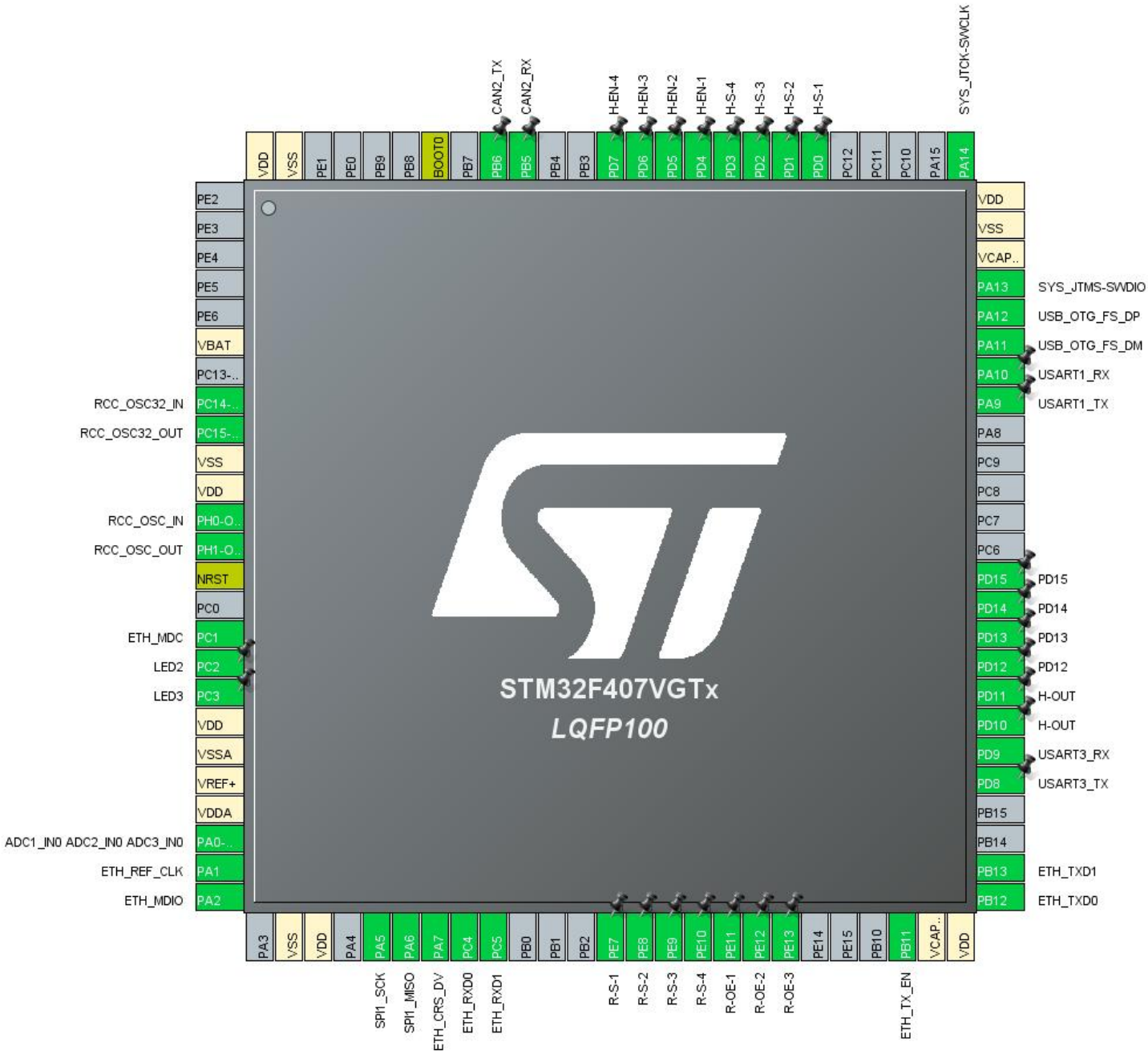
1.1. Project

Project Name	F407VGT6-FreeRTOSV1-lwip-jpeg
Board Name	custom
Generated with:	STM32CubeMX 5.2.0
Date	07/17/2019

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VGTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



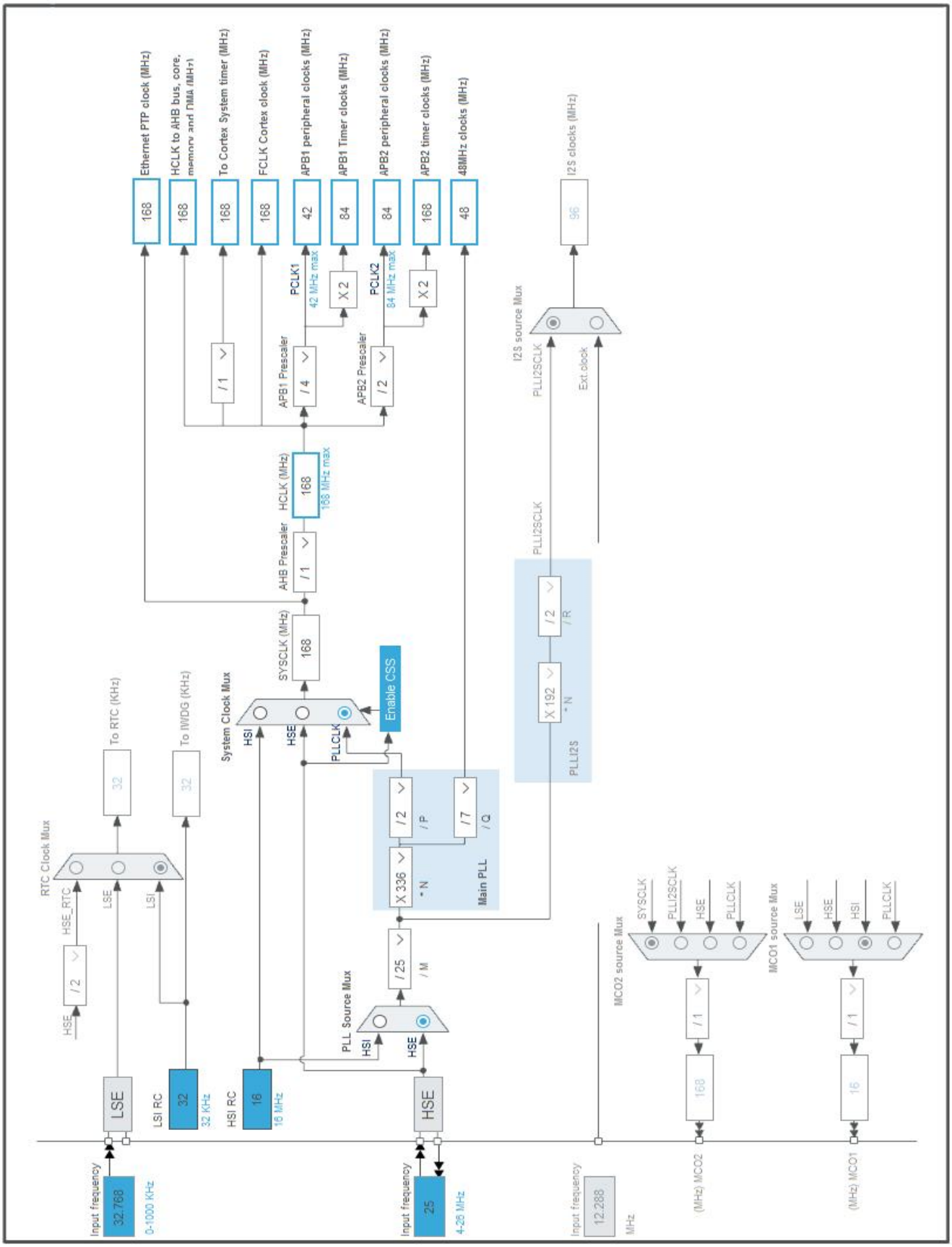
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
16	PC1	I/O	ETH_MDC	
17	PC2 *	I/O	GPIO_Output	LED2
18	PC3 *	I/O	GPIO_Output	LED3
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	ADC1_IN0, ADC2_IN0, ADC3_IN0	
24	PA1	I/O	ETH_REF_CLK	
25	PA2	I/O	ETH_MDIO	
27	VSS	Power		
28	VDD	Power		
30	PA5	I/O	SPI1_SCK	
31	PA6	I/O	SPI1_MISO	
32	PA7	I/O	ETH_CRS_DV	
33	PC4	I/O	ETH_RXD0	
34	PC5	I/O	ETH_RXD1	
38	PE7 *	I/O	GPIO_Output	R-S-1
39	PE8 *	I/O	GPIO_Output	R-S-2
40	PE9 *	I/O	GPIO_Output	R-S-3
41	PE10 *	I/O	GPIO_Output	R-S-4
42	PE11 *	I/O	GPIO_Output	R-OE-1
43	PE12 *	I/O	GPIO_Output	R-OE-2
44	PE13 *	I/O	GPIO_Output	R-OE-3
48	PB11	I/O	ETH_TX_EN	
49	VCAP_1	Power		
50	VDD	Power		

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
51	PB12	I/O	ETH_TXD0	
52	PB13	I/O	ETH_TXD1	
55	PD8	I/O	USART3_TX	
56	PD9	I/O	USART3_RX	
57	PD10 *	I/O	GPIO_Output	H-OUT
58	PD11 *	I/O	GPIO_Output	H-OUT
59	PD12 *	I/O	GPIO_Output	PD12
60	PD13 *	I/O	GPIO_Output	PD13
61	PD14 *	I/O	GPIO_Input	PD14
62	PD15 *	I/O	GPIO_Input	PD15
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
70	PA11	I/O	USB_OTG_FS_DM	
71	PA12	I/O	USB_OTG_FS_DP	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
81	PD0 *	I/O	GPIO_Output	H-S-1
82	PD1 *	I/O	GPIO_Output	H-S-2
83	PD2 *	I/O	GPIO_Output	H-S-3
84	PD3 *	I/O	GPIO_Output	H-S-4
85	PD4 *	I/O	GPIO_Output	H-EN-1
86	PD5 *	I/O	GPIO_Output	H-EN-2
87	PD6 *	I/O	GPIO_Output	H-EN-3
88	PD7 *	I/O	GPIO_Output	H-EN-4
91	PB5	I/O	CAN2_RX	
92	PB6	I/O	CAN2_TX	
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	F407VGT6-FreeRTOSV1-lwip-jpeg
Project Folder	D:\project\F407VGT-RTOSV1-lwip-jpeg
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.24.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VGTx
Datasheet	022152_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN0

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	**Triple combined regular simultaneous + injected simultaneous mode ***
DMA Access Mode	DMA access mode 1
Delay between 2 sampling phases	5 Cycles

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. ADC2

mode: IN0

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	**Triple combined regular simultaneous + injected**

	simultaneous mode *
DMA Access Mode	**DMA access mode 1 ***
Delay between 2 sampling phases	5 Cycles

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.3. ADC3

mode: IN0

7.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	**Triple combined regular simultaneous + injected simultaneous mode ***
DMA Access Mode	**DMA access mode 1 ***
Delay between 2 sampling phases	5 Cycles

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	

	Enabled *
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.4. CAN2

mode: Mode

7.4.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	16
Time Quantum	**380.95238095238096 ***
Time Quanta in Bit Segment 1	1 Time
Time Quanta in Bit Segment 2	1 Time
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

7.5. ETH

Mode: RMII

7.5.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled

General : Ethernet Configuration:

Ethernet MAC Address	00:80:E1:00:00:00
PHY Address	1

Ethernet Basic Configuration:

Rx Mode	Interrupt Mode
TX IP Header Checksum Computation	By hardware

7.5.2. Advanced Parameters:

External PHY Configuration:

PHY	**DP83848_PHY_ADDRESS ***
PHY Address Value	1
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x000000FF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	**0x0000FFFF ***
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***
Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***
Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	**0x0000 ***
Enable auto-negotiation function	**0x1000 ***
Restart auto-negotiation function	**0x0200 ***
Select the power down mode	**0x0800 ***
Isolate PHY from MII	**0x0400 ***
Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset	**0x1F ***
PHY Speed mask	**0x0004 ***
PHY Duplex mask	**0x0010 ***
PHY Interrupt Source Flag register Offset	**0x001D ***
PHY Link down inturrupt	**0x000B ***

7.6. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : BYPASS Clock Source

7.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

7.7. SPI1

Mode: Half-Duplex Slave

7.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.8. SYS

Debug: Serial Wire

Timebase Source: TIM2

7.9. USART1

Mode: Asynchronous

7.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.10. USART3

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.11. USB_OTG_FS

Mode: Device_Only

7.11.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

7.12. FREERTOS

Interface: CMSIS_V1

7.12.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.0.1
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

7.12.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled

xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

7.13. LIBJPEG

mode: Enabled

7.13.1. Config parameters:

Version:

LIBJPEG version	8d

MW configuration:

Data Stream management type	Stdio
FREERTOS	Enabled

General Settings:

Use FREERTOS Memory Allocator	Enabled

7.14. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

7.14.1. General Settings:

LwIP Version:

LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **)	2.0.3

IPv4 - DHCP Options:

LWIP_DHCP (DHCP Module)	Enabled

RTOS Dependency:

WITH_RTOS (Use FREERTOS ** CubeMX specific **)	Enabled

Protocols Options:

LWIP_ICMP (ICMP Module Activation)	Enabled
LWIP_IGMP (IGMP Module)	Disabled
LWIP_DNS (DNS Module)	Disabled
LWIP_UDP (UDP Module)	Enabled
MEMP_NUM_UDP_PCB (Number of UDP Connections)	4
LWIP_TCP (TCP Module)	Enabled
MEMP_NUM_TCP_PCB (Number of TCP Connections)	5

7.14.2. Key Options:

Infrastructure - OS Awarness Option:

NO_SYS (OS Awarness)	OS Used

Infrastructure - Timers Options:

LWIP_TIMERS (Use Support For sys_timeout)	Enabled

Infrastructure - Core Locking and MPU Options:

SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Enabled

Infrastructure - Heap and Memory Pools Options:

MEM_SIZE (Heap Memory Size)	1600

Infrastructure - Internal Memory Pool Sizes:

MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	8
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1

Pbuf Options:

PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	16
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592

IPv4 - ARP Options:

LWIP_ARP (ARP Functionality)	Enabled

Callback - TCP Options:

TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144
TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9

Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	Disabled

NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled

Infrastructure - Threading Options:

TCPIP_THREAD_NAME (TCPIP Thread Name)	"tcpip_thread"
TCPIP_THREAD_STACKSIZE (TCPIP Thread Stack Size)	1024
TCPIP_THREAD_PRIO (TCPIP Thread Priority Level)	3
TCPIP_MBOX_SIZE (TCPIP Mailbox Size)	6
DEFAULT_THREAD_NAME (Default LwIP Thread Name)	"lwIP"

DEFAULT_THREAD_STACKSIZE (Default LwIP Thread Stack Size)	1024
DEFAULT_THREAD_PRIO (Default LwIP Thread Priority Level)	3
DEFAULT_RAW_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN Raw)	0
DEFAULT_TCP_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN TCP)	6
DEFAULT_ACCEPTMBOX_SIZE (Default Mailbox Size for Incoming Connections)	6

Thread Safe APIs - Netconn Options:

LWIP_NETCONN (NETCONN API)	Enabled

Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Enabled
LWIP_COMPAT_SOCKETS (BSD-style Socket Functions Names)	1
LWIP_SOCKET_OFFSET (Socket Offset Number)	0

7.14.3. PPP:

PPP Options:

PPP_SUPPORT (PPP Module)	Disabled

7.14.4. IPv6:

IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	Disabled

7.14.5. HTTPD:

HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **)	Disabled

7.14.6. SNMP:

SNMP Options:

LWIP_SNMP (LwIP SNMP Agent)	Disabled

7.14.7. SNTP:

SNTP Options:

LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **)	Disabled

7.14.8. MDNS/TFTP:

MDNS Options:

LWIP_MDNS (Multicast DNS Support ** CubeMX specific **)	Disabled

TFTP Options:

LWIP_TFTP (TFTP Support ** CubeMX specific **)	**Enabled ***

7.14.9. Perf/Checks:

Sanity Checks:

LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks)	Disabled
LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks)	Disabled

Performance Options:

LWIP_PERF (Performace Testing for LwIP)	Disabled

7.14.10. Statistics:

Debug - Statistics Options:

LWIP_STATS (Statictics Collection)	Disabled

7.14.11. Checksum:

Infrastructure - Checksum Options:

CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **)	Disabled
LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif)	Disabled
CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets)	Disabled
CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets)	Disabled
CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets)	Disabled
CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets)	Disabled
CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets)	Disabled
CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets)	Disabled
CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets)	Disabled
CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets)	Disabled
CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets)	Disabled
CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets)	Disabled

7.14.12. Debug:

LwIP Main Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)	All

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PA0-WKUP	ADC2_IN0	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PA0-WKUP	ADC3_IN0	Analog mode	No pull-up and no pull-down	n/a	
CAN2	PB5	CAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB6	CAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down		

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					Very High *	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART3	PD8	USART3_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PD9	USART3_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED3
	PE7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	R-S-1
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	R-S-2
	PE9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	R-S-3
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	R-S-4
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	R-OE-1
	PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	R-OE-2
	PE13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	R-OE-3
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	H-OUT
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	H-OUT
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PD12
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PD13
	PD14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PD14
	PD15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PD15
	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	H-S-1
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	H-S-2
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	H-S-3
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	H-S-4

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	H-EN-1
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	H-EN-2
	PD6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	H-EN-3
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	H-EN-4

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	**High ***

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
TIM2 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	5	0
Ethernet global interrupt	true	5	0
Ethernet wake-up interrupt through EXTI line 19	true	5	0
CAN2 TX interrupts	true	5	0
CAN2 RX0 interrupts	true	5	0
CAN2 RX1 interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
SPI1 global interrupt	unused		
USART1 global interrupt	unused		
USART3 global interrupt	unused		
CAN2 SCE interrupt	unused		
USB On The Go FS global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

9. Software Pack Report