One. Chip characteristics

Part No	Scan channel number	applicable impedance range	dynamic power consumption(mA)	Standby power consumption(uA)	Operating Voltage (V)	Package
CST716	13	<30 K Ω	<5mA	<500uA	2.7 - 3.6	QFN 3X3-20L

two. Application schematic

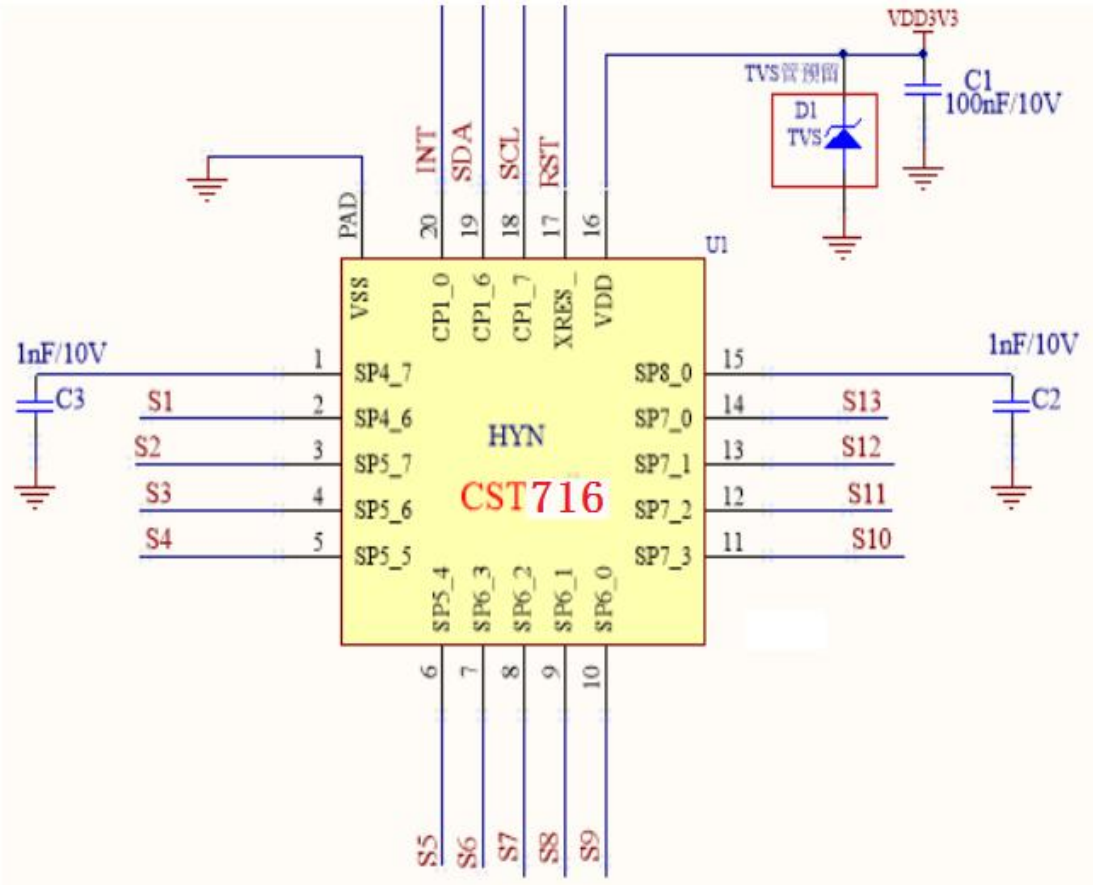


Figure one

Self-capacitive touch chip CST716 The number of channels from S1 Start to S13 , The channel application can be allocated arbitrarily, according to FPC drawing LAYOUT The wiring is convenient and free to choose.

three. FPC Design rules

2.1 Trace width

The minimum line width of the channel is 0.06mm , The median value is 0.07mm , The maximum value is 0.1mm , FPC in LAYOUT

Previously, we preferred median evaluation.

POWER (VDD) The width of the line is generally 0.15mm , The minimum width value is 0.1mm . To ensure the stability of the power supply

Qualitatively, it is recommended that in addition to the capacitance parameters in the schematic diagram, the power cord is connected to the magnetic beads in series at the input end of the po

According to the product power ripple.

The width of other signal lines is generally 0.1mm , The minimum width value is 0.07mm .

2.2 Via size

The via size is generally three values, as shown in Figure 2, generally we choose Preferred Parameter value, if via

Parameter should be less than Minimum When it is valued, communicate with the customer to confirm.

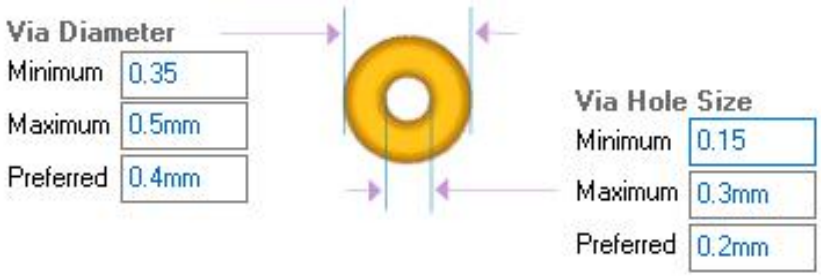


Figure II

2.3 Safety clearance

The minimum line spacing of the channel is 0.06mm , The general value is 0.07mm ;

Ground wire (GND) The minimum distance between other traces is 0.1mm, The general value is 0.15mm ;

The minimum distance between other traces and channel traces is 0.15mm , It is best to use ground wire isolation in the middle;

The minimum distance between all traces and vias is 0.06mm , The general value is 0.07mm ;

The minimum distance between vias and vias is 0.06mm, The general value is 1.0mm ;

All traces and FPC The minimum spacing of the borders is 0.15mm , The general value is 0.2mm ;

The minimum distance between copper and other traces is 0.1mm , The general value is 0.15mm ;

Copper and FPC The minimum spacing of the border is 0.15mm , The general value is 0.2mm .

2.4 FPC LAYOUT Precautions

2.4.1 Component placement according to FPC Depending on the location given by the structure, generally FPC Structure will give IC And peripheral devices

Specific location, the placement of peripheral devices FPC Keep the border to a minimum 0.4mm spacing. BPC capacitance C1, C3 want

Place close to the chip pins

2.4.2 IC Unused touch channels are suspended for processing, IC The substrate pad is grounded, and a via is placed on the substrate pad

Treatment (recommended to place at least 5 Vias), and copper (GND) Connect, place IC The reverse layer is patched in the steel sheet

Place a pad in the strong area (diameter 1mm The round pads on the left and right, open windows) are connected to the ground, the purpose is

Strong ground. As shown in Figure 3.

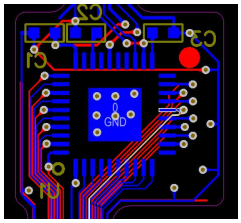


Figure three

2.4.3 The touch channel routing is generally the same line width and the same spacing, try to follow FPC Middle route, FPC Two

Leave enough space on the side to place the copper and connect it to the ground for protection; if it is the upper and lower layer wiring, the upper and lower layers are generally

The wiring should be staggered, and the channel wiring should not cross to prevent crosstalk (Figure 4).

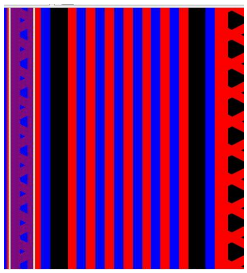


Figure Four

2.4.4 Copper paving is generally IC Pave solid copper in the reinforcement area, and pave copper with (usually the grid is set to 0.3mm,

The line width is set to 0.1mm), the rest of the place can also be grid copper or solid copper, all copper should be grounded. In order to reduce copper paving

Affect the welding of components, generally IC It is forbidden to spread copper on the bottom of the

Try to connect the disk to the ground with traces. As shown in Figure 5.

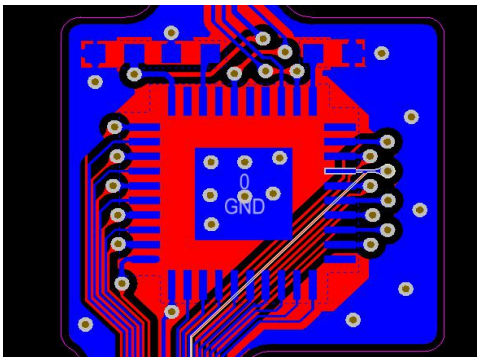


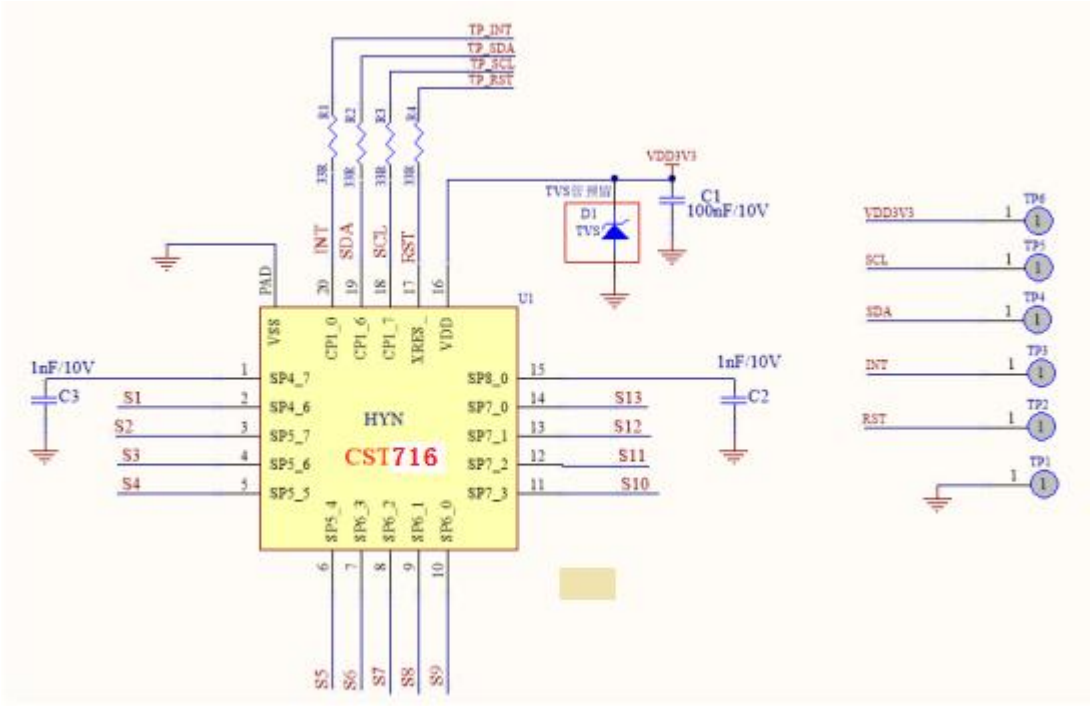
Figure 5

2.4.5 FPC Line to increase EMI Protection to improve anti-interference ability.

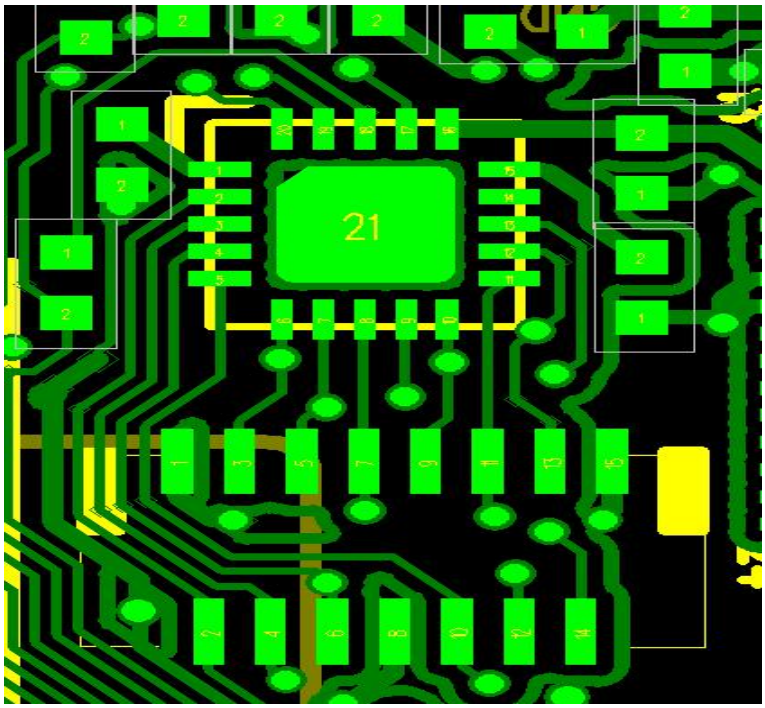
2.4.6 TP of FPC Do not cross or overlap the line with the RF antenna.

four. COB Design considerations

4.1 Application schematic



4.2. PCB Layout and routing



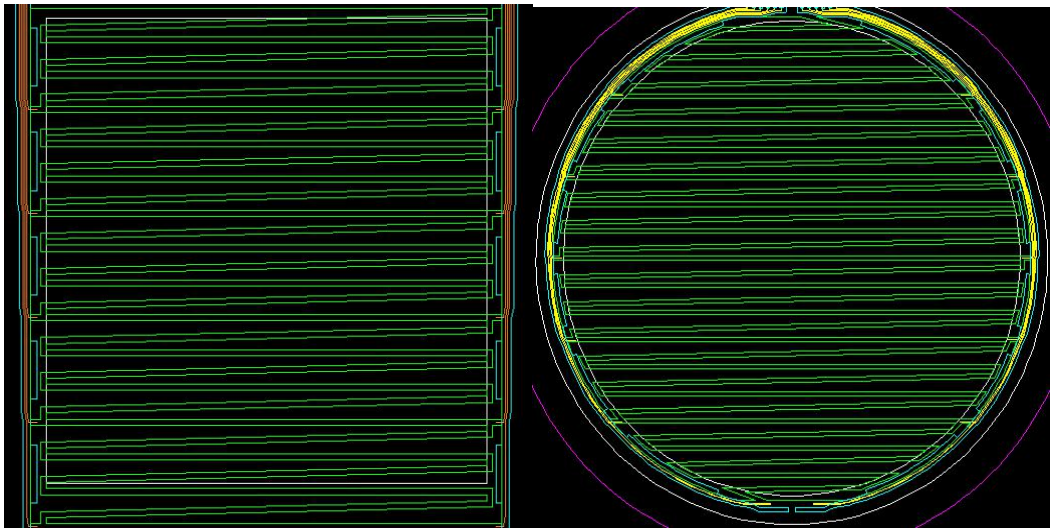
4.2.1 BPC capacitance(C2, C3) Close to the chip pins.

4.2.2 The channel wiring is connected to the connector PIN , Do not cross.

4.2.3 The channel wiring is isolated from other signal wires with ground wires.

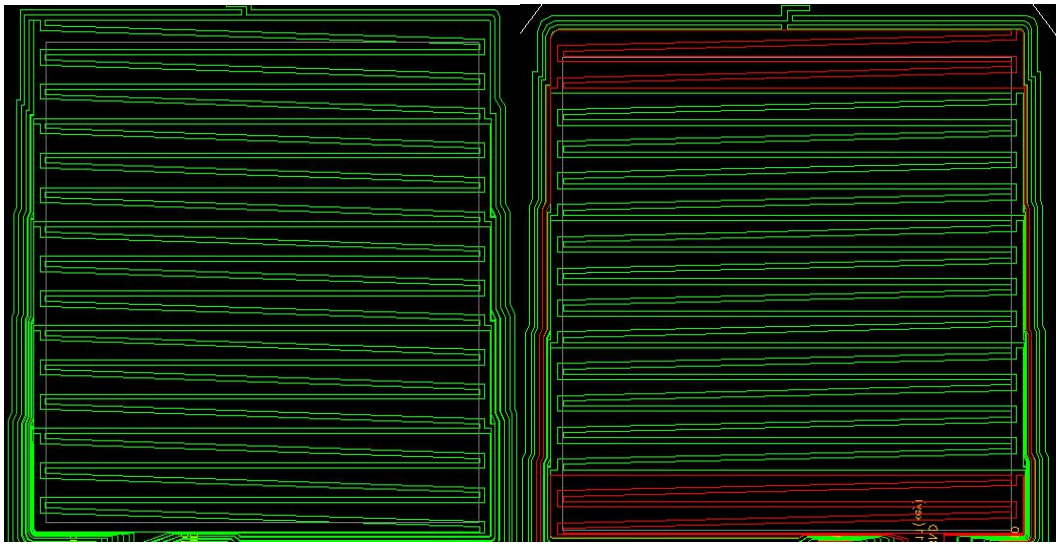
Fives. SENSOR Graphic design

Horizontal triangle pattern, support single point and gesture.

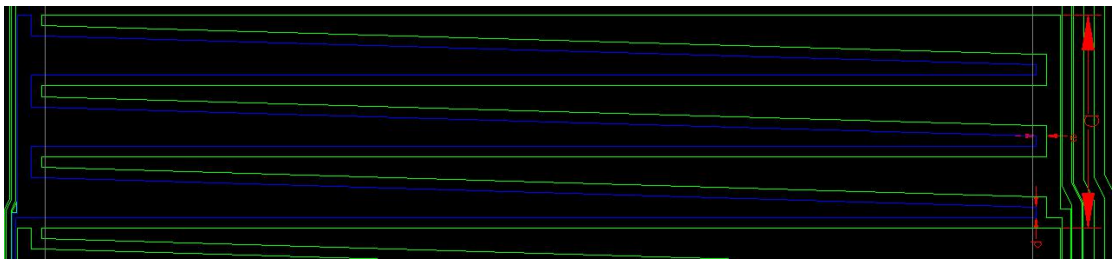


(1) Square window (2) Round window

" 333 "with" 242 "" type horizontal triangle pattern is all right, recommend" 333 "Type pattern, convenient for debugging.



(1)" 333 "type (2)" 242 "type



A : Pitch General advice 5~6.5mm Around, it is generally recommended to do at least 5 Pair channel

E : ito gap Depends on the process of the screen factory, generally 0.02~0.3mm .

D ：The width of the tip of the horizontal triangle, generally 0.3mm .