**ELEC 204 Digital Design Project Report**

Name: Demet Tümkaya, Mahmut Esat Pişkin

Date: 8/6/2022

1. **Introduction and objectives**

Explain the objectives of the lab (refer to the lab instruction sheet),

Explain what your code has to do and describe how you did it.

1. **Methods**

Explain the inputs (how many bits, names of the inputs),

Explain the outputs (how many bits, names of the outputs),

Explain what the VHDL code must do

Explain how your code works

Provide the truth table

1. **Problems encountered, errors and warnings resolved**

Explain what problems you encountered while writing your code.

Explain what synthesis errors and warnings you observed.

Explain what problems you had to solve (or could not) on your board even if your code could be synthesized successfully.

1. **Conclusion**

Provide a 1 paragraph summary of the lab and explain what you learned from this lab.

References

1. Please cite any resource (web site, book, youtube video) you used for this lab.

**Appendix 1. Project source code**

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**-- Company: Koç University**

**-- Engineer: Demet Tümkaya, Mahmut Esat Piskin**

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**-- Create Date: 10:02:05 06/07/2022**

**-- Design Name:**

**-- Module Name: final\_code - Behavioral**

**-- Project Name: MagicalLEDsOfStatistics**

**-- Target Devices:**

**-- Tool versions:**

**-- Description:**

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**-- Dependencies:**

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**-- Revision:**

**-- Revision 0.01 - File Created**

**-- Additional Comments:**

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**library IEEE;**

**use IEEE.STD\_LOGIC\_1164.ALL;**

**use IEEE.NUMERIC\_STD.ALL;**

**-- Uncomment the following library declaration if using**

**-- arithmetic functions with Signed or Unsigned values**

**--use IEEE.NUMERIC\_STD.ALL;**

**-- Uncomment the following library declaration if instantiating**

**-- any Xilinx primitives in this code.**

**--library UNISIM;**

**--use UNISIM.VComponents.all;**

**entity final\_code is**

**Port ( Clock : in STD\_LOGIC;**

**enter : in STD\_LOGIC;**

**input1 : in STD\_LOGIC\_VECTOR (3 downto 0);**

**input2 : in STD\_LOGIC\_VECTOR (3 downto 0);**

**input3 : in STD\_LOGIC\_VECTOR (3 downto 0);**

**result : out STD\_LOGIC\_VECTOR (15 downto 0);**

**mint: out STD\_LOGIC\_VECTOR (15 downto 0);**

**maxt: out STD\_LOGIC\_VECTOR (15 downto 0);**

**medt: out STD\_LOGIC\_VECTOR (15 downto 0);**

**ranget: out STD\_LOGIC\_VECTOR (15 downto 0));**

**end final\_code;**

**architecture Behavioral of final\_code is**

**signal count : integer := 3 ;**

**signal average : integer := 0;**

**shared variable result\_temp : integer := 0;**

**shared variable min\_temp : integer := 0;**

**shared variable max\_temp : integer := 0;**

**shared variable med\_temp : integer := 0;**

**shared variable range\_temp : integer := 0;**

**signal q : integer := 0;**

**shared variable in1\_int : integer ;**

**shared variable in2\_int : integer ;**

**shared variable in3\_int : integer ;**

**shared variable range\_int : integer:= 0 ;**

**shared variable min\_int : integer := 0;**

**shared variable max\_int : integer := 0;**

**shared variable med\_int : integer := 0;**

**shared variable result\_int : integer := 0;**

**begin**

**process(Clock)**

**begin**

**in1\_int := to\_integer(unsigned(input1));**

**in2\_int := to\_integer(unsigned(input2));**

**in3\_int := to\_integer(unsigned(input3));**

**if(rising\_edge(Clock)) then**

**if(average = 0) then**

**result\_int := in1\_int + in2\_int + in3\_int;**

**average <= 1;**

**elsif (average = 1) then**

**if (result\_int > count) then**

**result\_int := result\_int - count;**

**q <= q+1;**

**elsif (result\_int = count) then**

**result\_int := result\_int - count;**

**q <= q+1;**

**else**

**result\_temp := q;**

**q <= 0;**

**average <= 0;**

**end if;**

**end if;**

**end if;**

**if(rising\_edge(Clock)) then**

**min\_int := in1\_int;**

**med\_int := in2\_int;**

**max\_int := in3\_int;**

**if(min\_int > med\_int) then**

**med\_int := in1\_int;**

**min\_int := in2\_int;**

**end if;**

**if(med\_int > max\_int) then**

**max\_int := med\_int;**

**med\_int := in3\_int;**

**if(min\_int > med\_int) then**

**med\_int := min\_int;**

**min\_int:= in3\_int;**

**end if;**

**end if;**

**max\_temp := max\_int;**

**min\_temp := min\_int;**

**med\_temp := med\_int;**

**range\_int := max\_int - min\_int;**

**range\_temp := range\_int;**

**end if;**

**maxt <= std\_logic\_vector(to\_unsigned(max\_temp, 16));**

**mint <= std\_logic\_vector(to\_unsigned(min\_temp, 16));**

**medt <= std\_logic\_vector(to\_unsigned(med\_temp, 16));**

**ranget <= std\_logic\_vector(to\_unsigned(range\_temp, 16));**

**result <= std\_logic\_vector(to\_unsigned(result\_temp, 16));**

**end process;**

**end Behavioral;**

**Project Simulation Code**

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**-- Company: Koç University**

**-- Engineer: Demet Tümkaya, Mahmut Esat Piskin**

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**-- Create Date: 10:22:33 06/07/2022**

**-- Design Name:**

**-- Module Name:**

**-- Project Name: final\_project**

**-- Target Device:**

**-- Tool versions:**

**-- Description:**

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**-- VHDL Test Bench Created by ISE for module: final\_code**

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**-- Dependencies:**

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**-- Revision:**

**-- Revision 0.01 - File Created**

**-- Additional Comments:**

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**-- Notes:**

**-- This testbench has been automatically generated using types std\_logic and**

**-- std\_logic\_vector for the ports of the unit under test. Xilinx recommends**

**-- that these types always be used for the top-level I/O of a design in order**

**-- to guarantee that the testbench will bind correctly to the post-implementation**

**-- simulation model.**

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**LIBRARY ieee;**

**USE ieee.std\_logic\_1164.ALL;**

**-- Uncomment the following library declaration if using**

**-- arithmetic functions with Signed or Unsigned values**

**--USE ieee.numeric\_std.ALL;**

**ENTITY final\_sim IS**

**END final\_sim;**

**ARCHITECTURE behavior OF final\_sim IS**

**-- Component Declaration for the Unit Under Test (UUT)**

**COMPONENT final\_code**

**PORT(**

**Clock : IN std\_logic;**

**enter : IN std\_logic;**

**input1 : IN std\_logic\_vector(3 downto 0);**

**input2 : IN std\_logic\_vector(3 downto 0);**

**input3 : IN std\_logic\_vector(3 downto 0);**

**result : OUT std\_logic\_vector(15 downto 0);**

**mint : OUT std\_logic\_vector(15 downto 0);**

**maxt : OUT std\_logic\_vector(15 downto 0);**

**medt : OUT std\_logic\_vector(15 downto 0);**

**ranget : OUT std\_logic\_vector(15 downto 0)**

**);**

**END COMPONENT;**

**--Inputs**

**signal Clock : std\_logic := '0';**

**signal enter : std\_logic := '0';**

**signal input1 : std\_logic\_vector(3 downto 0) := (others => '0');**

**signal input2 : std\_logic\_vector(3 downto 0) := (others => '0');**

**signal input3 : std\_logic\_vector(3 downto 0) := (others => '0');**

**--Outputs**

**signal result : std\_logic\_vector(15 downto 0);**

**signal mint : std\_logic\_vector(15 downto 0);**

**signal maxt : std\_logic\_vector(15 downto 0);**

**signal medt : std\_logic\_vector(15 downto 0);**

**signal ranget : std\_logic\_vector(15 downto 0);**

**-- No clocks detected in port list. Replace <clock> below with**

**-- appropriate port name**

**constant Clock\_period : time := 100 ns;**

**BEGIN**

**-- Instantiate the Unit Under Test (UUT)**

**uut: final\_code PORT MAP (**

**Clock => Clock,**

**enter => enter,**

**input1 => input1,**

**input2 => input2,**

**input3 => input3,**

**result => result,**

**maxt => maxt,**

**mint => mint,**

**medt => medt,**

**ranget => ranget**

**);**

**-- Clock process definitions**

**Clock\_process :process**

**begin**

**Clock <= '0';**

**wait for Clock\_period/10;**

**Clock <= '1';**

**wait for Clock\_period/10;**

**end process;**

**-- Stimulus process**

**stim\_proc: process**

**begin**

**-- hold reset state for 100 ns.**

**enter <= '1';**

**input1 <= "0001";**

**input2 <= "0010";**

**input3 <= "0011";**

**wait for 250 ns;**

**input1 <= "0100";**

**input2 <= "0101";**

**input3 <= "0110";**

**wait for 250 ns;**

**input1 <= "0111";**

**input2 <= "1000";**

**input3 <= "1001";**

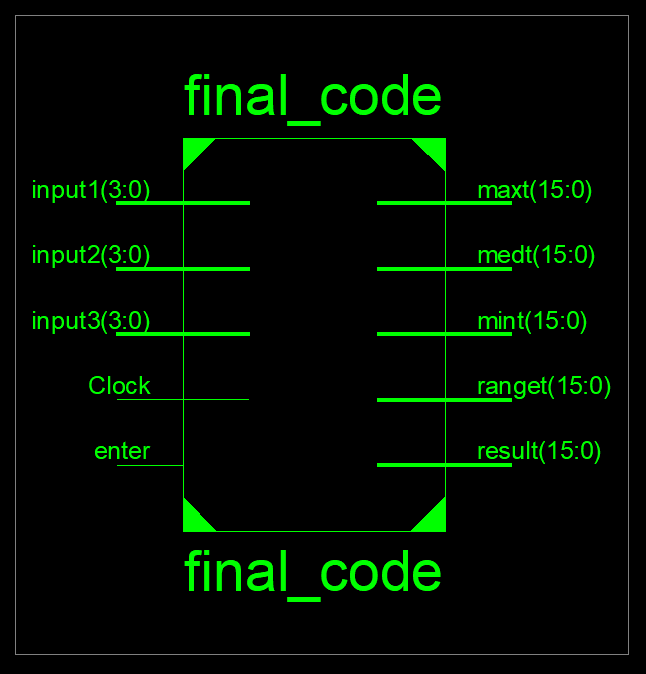
**-- insert stimulus here**

**wait;**

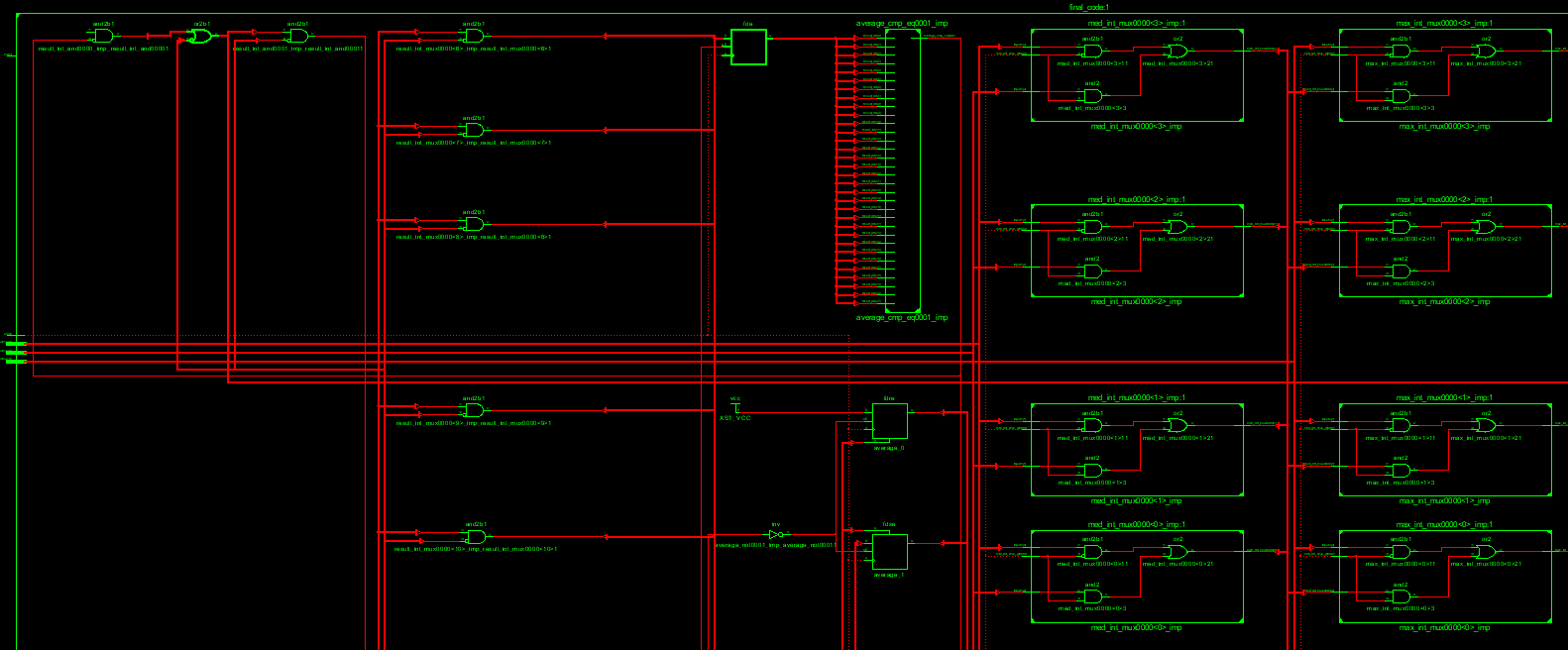
**end process;**

**END;**

**Appendix 2. RTL schematics**

metin, skorbord içeren bir resim

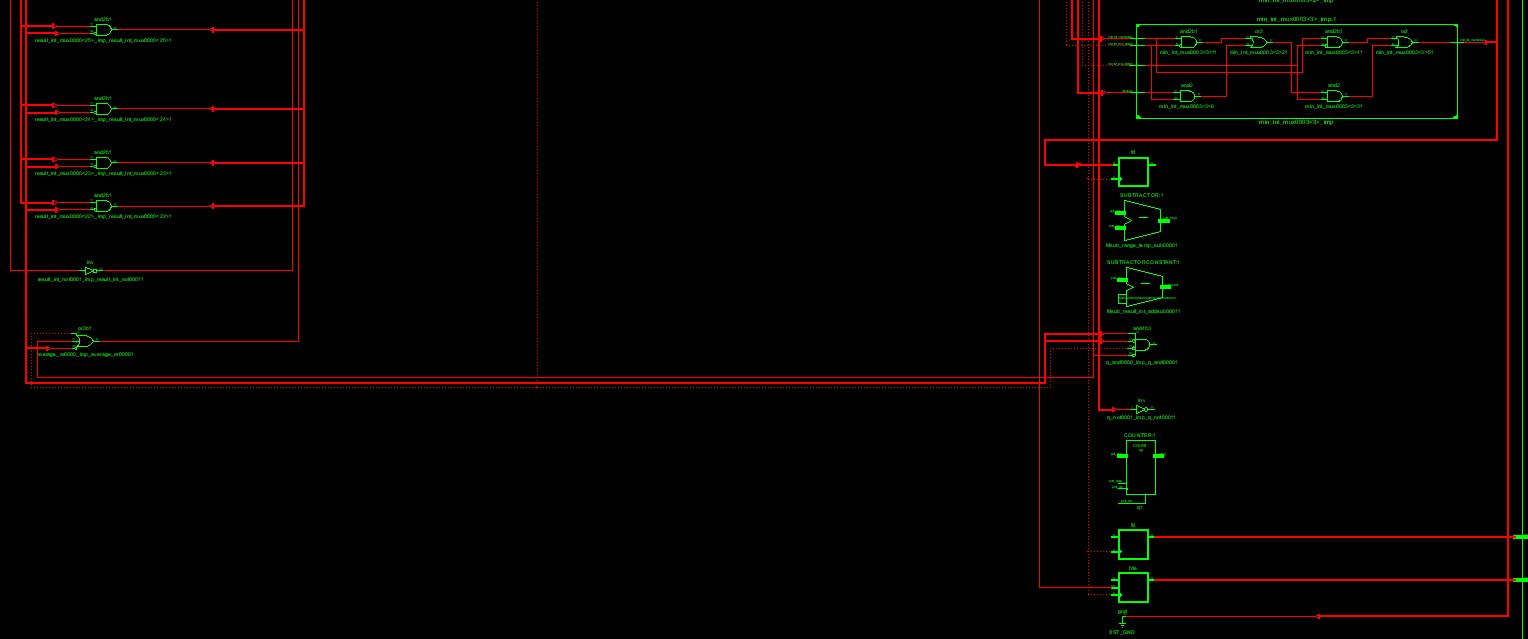
Açıklama otomatik olarak oluşturuldu



metin, elektronik eşyalar, ekran görüntüsü içeren bir resim

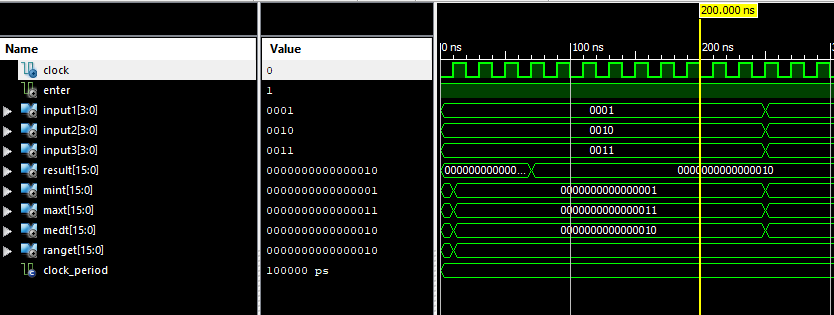
Açıklama otomatik olarak oluşturuldumetin, elektronik eşyalar, skorbord içeren bir resim

Açıklama otomatik olarak oluşturuldumetin, elektronik eşyalar içeren bir resim

Açıklama otomatik olarak oluşturuldu

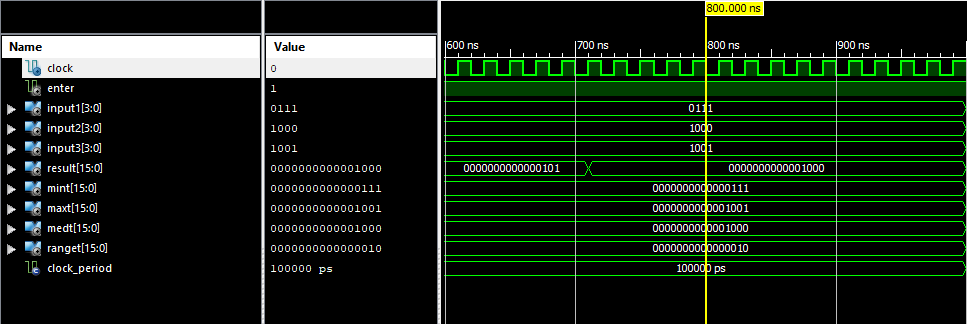
**Appendix 3. Photos showing working code**

**FPGA is not available, so we add our simulation here with 3 examples**



metin içeren bir resim

Açıklama otomatik olarak oluşturuldu



**Appendix 4. Screenshots from Xilinx for the errors and other board issues**

**There are no errors in our code, but we have number of warnings**

metin içeren bir resim

Açıklama otomatik olarak oluşturuldu

metin, pencere içeren bir resim

Açıklama otomatik olarak oluşturuldu

**No errors in simulation**

metin içeren bir resim

Açıklama otomatik olarak oluşturuldu