

# Hot Chips Processor Conference

## Hot Chips Conference: Day 2 Highlights

### **DeepMind Keynote sets the stage for next gen AI computer architecture**

Google's DeepMind, at the frontier of AI research, laid bare the limitations of data intensive approach to Deep Learning that is driving AI architectures today. While demand for compute is growing at ~10x Y/Y, present day AI architectures are only delivering a 40% Y/Y increase in compute capacity and creating an unsustainably large gap between demand and supply. DeepMind suggested System Level innovation would be critical for Data Center scale compute that will ultimately enable Artificial General Intelligence - bolstering our favourable view on NVDA acquisition of Mellanox.

### **Wafer Scale Computing – Cerebras Gen 1 Installed, in-use, larger Gen 2 in labs**

Cerebras announced that multiple units of CS1 system are in use today across multiple verticals. Cerebras' chip spans the entire wafer, uses >46,000 sq-mm of silicon with 1.2T transistors (>20x Nvidia Ampere), consists of 400,000 AI optimized cores, 16GB of on-chip memory & is mfg on TSMC 16nm. Cerebras has made solid progress on its software stack that uses parallelism & Sparsity to unlock cluster scale AI performance. It also announced CS2 (850,000 AI cores, 2.6T transistors, TSMC 7nm) has seen first silicon in the lab. While we don't see CS going main stream, it speaks to our view that a large AI driven compute tide is lifting many boats, NVDA remains well positioned.

### **Google Deep Dive into TPUv2/v3 architecture,**

While TPUv1 was designed as co-processor to the CPU and geared towards inference, Google is relying on a combination of improved Execution Core units, High Bandwidth Memory and interconnect to enable training on TPUv2/v3. While performance may not be strictly comparable to Ampere powered NVDA DGX (8x A100, 5 petaFLOPS AI of performance), Google is building Training Pods (TPUv2, 256 chips, 11.5 petaFLOPS; TPUv3 1024 Chips, > 100 petaFLOPS) to unlock Super Computer like performance. Google indicated that it had no roadmap at this time to offer pods on GCP.

### **Beyond CPU – Fungible unveils a new class of Microprocessors – DPU**

With network speeds growing faster than compute, Data center scaling is being hampered inefficient data interchange between servers & inefficient execution of computations within each node, creating a new dedicated class of compute - Data Processing unit (DPU). Fungible, a Silicon Valley start-up unveiled Fungible F1 (DPU).

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## **Key Note: DeepMind**

### **AI Research – Road Ahead**

Key takeaways

- DeepMind – Apollo Program for AI - Artificial General Intelligence is the goal
  - Neuroscience is a catalyst for AI and AI research feeds back into Neuroscience
  - Virtual environments accelerate AI but carry complexity
  - ML is a method to infer knowledge from observation
- Data Intensive AI/search is not practical
  - Reduce breadth of search tree by policy networks
  - Smarter ways to reduce data intensive training
  - Model based Reinforcement learning – make good decisions from experience and through imagination as learning can be very expensive and time consuming
  - DeepMind research focusing on learning for real life
    - Using Graph networks as one tool
    - ML based simulations have made a lot of ground in the last few years
- Demand and supply for Compute
  - Scaling up compute works – usefulness of ML scales independent of data size – driven by algorithms - more search/more compute gives better models of the world
  - Algorithms efficiency gains are not enough , computation demand has gone up 10x /year since 2012
  - CPU perf has barely budged
  - AI hardware has improved roughly 40% /year
  - If demand growth holds – it isn't sustainable long term
- Bridging the gap – 3 opportunities to do so

- Think about Systems, not the Chips
  - Optimize the throughput of the entire research systems
    - Sustained Performance/TCO is important for research
    - Average FLOP utilization is 20% of peak flops – job startup time, compiler issues, contention, runtime memory bound, I/O starvation
    - System performance per \$ matters – Designing systems top down for Data Center scale is more important
    - Designing Warehouse scale computers
  - Not much room at the bottom
    - Si, Power and Software – matter for computers
    - Floor of cost/instruction 1000x lower than where we are
    - Power – sunlight is abundant , 3x order of magnitude away from floor from a basic stand point
      - Components disappearing into silicon
      - Make more computers and more silicon
    - Move everything into silicon – even if solutions look expensive in the near term
      - Forces you to add components that you only really need
      - Exploit non linearities
      - New rules – paradigm shifts
        - Smaller simpler chips – easy to scale up
        - Fewer components in Si
        - Huge quantities
        - Cheap , less reliable
    - Software Floor
      - AI agents are distributed systems

- Big gains come from paradigm shifts in chips – CPU-> GPU->TPU
  - Diversity of Hardware gives rise to different/flexible software
  - High software overhead can cause over investment
  - AI programs are far more constrained than general; purpose
  - Constrained by data flow , constrained by arithmetic
  - Compiler friction is a huge opportunity – deep learning for compilers has come
- Data Center as a computer
- Conclusions
  - A research is good area for systems design
  - Start focusing on whole systems
  - Time to exploit economies of scale – simpler chips
  - Embrace advances in ML for the design of software infrastructure

## Google TPU V2/V3 for Training

TPU V1 – training bottleneck

TPUV2/V3 fixes that

Training – challenges

- more compute, more memory , wider operands, more programmability and harder parallelization
- ambitious on a budget

Goals

- Quickly, high perf, at scale, tackle new workloads out of the box

## Cost effective

- TPU v1 data and computation bandwidth loop was the focus
- TPU v2 –
  - single vector memory instead of buffers
  - Matrix co-processor
  - Went to HBM for bandwidth
  - Interconnect fabric to scale and connect multiple cores
  - 2 cores per chip – fewer bigger cores are easier to program

## TPU core

- VLIW arch
- Scalar unit -322b VLIW bundle
- Vector unit – 128 vector lanes , dual issue 32 bit vector lane
- MMU
  - 128x128 systolic array
  - Bfloat 16 multiply
  - Float 32 accumulation
  - Transpose , reduction permute unit
- Memory System
  - SRAM based scratch pads
  - Add HBM for capacity and high bandwidth
  - HBM stores vectors and matrices
  - 700GB/sec per chip memory bandwidth from HBM
  - 2 cores each connected to half of the HBM
- Interconnect
  - 4 off chip links 500Gbps link
  - 2D torus
  - Most area to compute cores , Bfloat gives them compute density

## TPU V3

- Doubled matrix mult units
- Bumped up clock frequency

- 2x HBM capacity
- +30% B/W by faster HBM
- Interconnect 4x nodes

TPU V3 has 2x perf over V2

Hardware software co-design, build it quickly, high performance at scale ,  
xla compiler, HBM , matrix units simple and efficient

### Chips to systems

- V1 – built as co processor to CPU – good for inference, single chip chip solutions
- V2/v3- ML super computer
  - Multiple chips working in conjunction
  - 4TPUs connected in corus on a board – synchronous parallel training
  - Training pod
    - V2 64 boards x 4 chips = 256
    - V3 = 1024 =
    - V2 11.5 PF, \$TB HBM
    - , PTU v3 > 100 PF , 32TB HBM
- Used in production applications
  - V3- linear scaling at 1024 chips
- V3 vs. V2 - \
  - Peak per 2.7x
  - Memory bandwidth = 30%
  - Increased compute was better utilized on v3
  - Software stack improvements driving gains
  - V2, v3 also do well on inference e- lower latency in v2 (3x) even while getting larger batch sizes vs. v1
  - V2 has more memory bandwidth – lower latency allowed ro larger batches , thru put 10x, 2x lower latency

- V3 lowers latency by another 30%
- TPU systems with 256-1024 chips run product ion apps at scale

GCP – availability – no external road map

## Cerebras

Software /Hardware co-design

Need co design to solve DL problems

- 1.2 Trillion transistors, 400k AI cores, TSMC 16nm,
- CS1 – cluster scale DL performance – programmed by standard ML frameworks, installs at standard DC racks.
- Many systems in use and delivered to customers

400k cores optimized for DL

Compute

Fine grained, fully independent and programmable

Sparsity m dynamic workloads

Memory

Fully distributed high perf on-chip memory

Communication

High b/w , low latency interconnect

2D mesh spans across the entire wafer

Linear performance cluster-scale performance on a single chip

SW co-designed software for scale from very beginning

- Custom software

- Extract from high level framework -> match->place->link

## Matching Kernel Library

- Kernel is auto generated
  - Polyhedral techniques for loop unrolling
- Also have hand optimized kernels

## Mapping strategy for each kernel – model and data parallelism

- Allocate compute , memory and fabric to each kernel by optimization

## High degree of flexibility and performance

- Software stack – model parallel and data parallel
- Harvesting and inducing sparsity
- Dynamic neural network execution

## Wafer scale gets performance from parallelism

- Data Parallelism
  - For smaller workloads- run layer replicas
  - Small batch size
  - 8 replicas can scale to 400kl cores
  - Linear performance at medium batch size
- Model parallelism
- The 2 points are the ends of a spectrum and software stack allows you to choose across the spectrum – based on workload
- Single kernel can be split across multiple units- GPU is tough as limited I/o
- Small batch size
- No weight sync overhead

- 4 layer BERT performance scale linearly – model parallelism on wafer scale gets you linear scale

## Sparsity

- Harvest natural sparsity in neural network - 1.2x performance improvement
- Induce sparsity when necessary – 1.7x-2.4x perf gains
  - 1.7x with ReLU;
  - 2.4x perf gains with Relu +50% sparsity
- Core is designed for sparsity

BERT has no natural sparsity

- 1.5x perf gain with 50% induced sparsity
- ML user has full control of techniques

Codesign – designed to unlock smarter techniques and scale

CS1 is the most powerful single node

- Model and data parallelism
- Cluster scale performance on a single chip
- Flexible parallelism and flexible execution

## Gen 2

- 850,000 AI optimized cores
- 2.6 Trillion Transistor
- TSMC 7nm process
- Working in the lab today
- Software has been codesigned
- Unlocking new workloads

Main benefit of wafer scale engine

- GPU and TPU see linear scaling in some workloads
- Only some workloads can scale on GPU/TPU
- Cerebras is opening door to novel ML techniques – models will not be able to run on traditional hardware. Traditional data parallelism will not apply
- New computer arch for deep learning

1.2Tbps Ethernet interconnect have designed

Borrowing ideas from EDA industry to solve compiling issues, but although placing 400k , placing and routing smaller number of elements

## Silicon Photonics for AI - Light Matter

Mars is an AI accelerator based on Silicon Photonics

Optical computations

Chips are getting hotter, transistors are not getting faster

AI is creating an explosion in compute demand

Photonics Core

3 benefits for optics

- Optical data transport more energy efficient, no RC coefficient
- Optical Tensor Core – higher frequency , less energy and lower latency
  - Using MZI interferometer for computation
  - Need programmable phase shifters –
  - Mars uses Nano Optical Electro Mechanical System
- Parallel Processing – wavelength and polarization multiplexing
  - Optical Vector MAC – compute tile
  - 64x64 matrix '1Ghz vector rate

- 50mW laser
- Digital core
  - Mars SoC
  - 14nm custom ASIC
  - 50mm<sup>2</sup>
- 3d stacking
- Software stack ready

## Pensando , Distributed services Architecture

Distributed Services arch

- No service stitching requires all functions are present everywhere
- Policy, automation , observability, ecosystems
- Distributed services card – PCIe card , with Pensando chip

Chip arch of P4 Pensando Chip

- Networking function to manage Ethernet , processing path, NOC
- DMA transfer capability

P4 pipeline design

- Has local SRAM, TCAM, DRAM cache
- 8 stages apply match action tables
- Pipeline ends at a Deparser or DMA unit

P4 stage design

- Table Engine
- Match processing units
- Stage data logic

Central Packet Buffer

- Connects P4 pipelines to MACs

- Shared memory switch

PCIe Virtualization services

- PCIe switches , devices are configurable
- Ethernet controller, RDMA device, NVMe drive etc can be configured

Security embedded in all chips

Capri – TSMC 16nm, shipping in volume

Elba TSMC 7nm running in the lab

Architecture remains consistent between the 2 chips

Switched from HBM to DDR for more memory capacity

## Fungible DPU

DPU sits at the intersection of network , compute and storage

New category of microprocessor

Problems facing data centers

- Footprint is too large
- Scalling challenges
- Increasing complexity
- Security

Headwinds

- Network and storage performance increasing faster than compute perf
- Apps need access to large data sets
- Moores law
- Security attacks

Hyper disaggregated scale out

- X86, GPU servers, SSD, HDD servers

Root cause

Inefficient data centric computations inside nodes

Network stack, storage, virtualization and security stack

Inefficient data exchange between nodes

Fungible addresses all 5 root causes

Fungible DPU sits inside each server. Connects to PCIe and Ethernet

Implements through fabric

Cross sectional bandwidth, Low latency, jitter, control , security

F1 DPU

8 data clusters

- 192 processor threads
- 6 cores x 4 threads
- 6 accelerators tightly coupled to general purpose CPU

Control cluster,

- Control plane on DPU – 4 cores x 2 thread
- Provisions for Security

fast on chip network

Memory, i/o – connect to PCIe and Ethernet , supports DDR4, HBM

- CPU – MIPS 64 , floating point and SIMD .Full hardware virtualization, large caches
- Network engine – low latency MAC, FEC
- Host engine is high performance 512G
- Endpoint for x86 or ARM CPU

Novel model for data path programming

Comes with a complete software stack

Invented a new category of Microprocessor- Multicore MIMD

High throughput dis-aggregation and pooling

Why use MIPS rather than ARM or RISC V

- Best one for solving data centric configurations very efficiently
- Do not depend strongly on any specific ISA

DPU vs. competition

- DPU Solves 2 critical problems in the data center
  - Node to node interactions between servers are inefficient
  - Data centric computations are executed inefficiently on general purpose compute
- DPU – solves the problems

True Fabric vss. Standard Ethernet

- True fabric is built on top of Ethernet
- True Fabric is open standard tech, operates both on IP over Ethernet and TCP-IP over Ethernet

Scalability comes from

- Bandwidth of individual interfaces
- Overall capacity of network

## **Intel, Agilex FPGA for Data Center**

### **Core Arch**

- Next Gen Core arch
- New micro arch customized for 10nm (SuperFin)
- 40% higher perf, 40% lower power- coming from routing/core fabric innovations, clocking

Advanced memory /network

- DDR4/5, HBM2e, Optane
- Transceiver tiles with speeds up to 116Gbps
- PCIe Gen 5, CXL interconnect

Second gen EMIB

Software stack

- One API ecosystem
- Leading Edge EDA with Intel Quartus Prime Software
  - Re-timing – lack of scalable sequential verification tools

## **Xilinx, Versal Premium Series**

Versal overview

- ACAP – adaptable platform
- 3 engines – CPU (ARM), DSP, FPGA programmable engines
- Interface: PCIe Gen 5, DDR4, Transceivers, Ethernet
- Built, preconfigured for Data Center –
- Programmable NoC – connects DSP, compute and interface
- Hardened implementation of – network IP

## Key blocks

- Start with PL
- Add noc, processor backbone
- Memory controllers, Protocol engines, SerDes
- Adaptable kernels

## Device Architecture

- DCMAC= 600G of ethernet
  - Handles all protocol related functions
- 100G Multirate Ethernet
- 400G High-Speed Crypto Engine (HSC)
- **XSR die to Die interface- 2 dies can come from different foundries – Chiplets**
- PCIe Gen 5
- Hardened PCIe/CXL controllers
- Programmable logic surrounded by hardened IP
- 4th gen SSIT from TSMC (Stacked Silicon Interposer Tech)
- Delivering more than more – 2.6X protocol B/W,

## Target market

- Wire, Data Center, Testing, Aerospace

- Enabling next gen Data Center interconnect
- Scale out Fabrics

Fab in TSMC 7nm, TSMC CoWoS, 107 INT TOPS engine performance peak,  
92 B transistors , on chip memory of 1Gb

High speed networking engines, Hardened Soc shell up and running before  
logic programming

4th Gen SSIT die stacking enables very large devices

Adaptable SoC with large bandwidth and compute density

## **Valuation Method and Risk Statement**

NVIDIA: Valuation methodology: Our PT is based on applying a P/E multiple.

NVIDIA company-specific risks include: 1) competition from AMD in graphics processors (GPUs) and professional visualization products (Quadro), which historically have driven the bulk of the company's gross profit, 2) intense competition in ARM-based applications processors (Tegra), where rivals seek to leapfrog NVIDIA's early lead in dual-core technology, 3) emerging competition from Intel with its many-integrated core (MIC) Knights processor family vs the company's professional GPU computing products (Tesla), where Intel's approach could be more flexible and easier to develop software for than Tesla. In addition, NVIDIA faces the semiconductor sector risk where revenue trends have historically been linked to corporate profitability, which could be challenged for robust growth, as the economic recovery has been more subdued vs prior deep downturns.

INTC has a major presence in the data center. However the data center is getting more competitive. Some of AMD's share gains in the data center at INTC's expense look priced into INTC stock at present levels. However should AMD CPU show more traction in the Data Center than our expectations, leading to an even more accelerated share loss trajectory for INTC, this could present a downside risk to INTC stock. Further, although NVDA dominates GPU space, as more compute migrates away from INTC CPU to NVDA GPU, an accelerated pace of this migration also represents a downside risk.

Should INTC resolve its manufacturing challenges sooner than the recently indicated 12 month shift, this would present an upside risk.

Due to ramping depreciation, for INTC we use an EV/FCF multiple basis but use P/E as sanity-check.

We value AMD using EV/FCF methodology.

Upside risk to our AMD thesis include higher-than-anticipated penetration into cloud/data center servers and better traction in AI. Downside risks include margin pressure in the form of aggressive price competition from Intel and an inability to effectively shift production to TSMC in a timely manner.

For MRVL We use a PE multiple methodology for valuation.

Cloud customers are desperate for another source beyond AVGO/CSCO, but it could take time for the next window to open. In storage, we may be underestimating the internal controller efforts and capabilities at SSD suppliers.

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12-Month Rating	Definition	Coverage <sup>1</sup>	IB Services <sup>2</sup>
Buy	FSR is > 6% above the MRA.	49%	32%
Neutral	FSR is between -6% and 6% of the MRA.	39%	30%
Sell	FSR is > 6% below the MRA.	13%	20%
Short-Term Rating	Definition	Coverage <sup>3</sup>	IB Services <sup>4</sup>
Buy	Stock price expected to rise within three months from the time the rating was assigned because of a specific catalyst or event.	<1%	<1%
Sell	Stock price expected to fall within three months from the time the rating was assigned because of a specific catalyst or event.	<1%	<1%

Source: UBS. Rating allocations are as of 30 June 2020.

1:Percentage of companies under coverage globally within the 12-month rating category.

2:Percentage of companies within the 12-month rating category for which investment banking (IB) services were provided within the past 12 months.

3:Percentage of companies under coverage globally within the Short-Term rating category.

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**UBS Securities LLC:** Timothy Arcuri; Pradeep Ramani; Diana Chang; Seth Gilbert.

### Company Disclosures

Company Name	Reuters	12-month rating	Short-term rating	Price	Price date
<b>Advanced Micro Devices Inc</b> <sup>16, 20</sup>	AMD.O	Neutral (CBE)		N/A	US\$81.66 18 Aug 2020
<b>Intel Corp.</b> <sup>6a, 6b, 7, 16</sup>	INTC.O	Buy		N/A	US\$48.65 18 Aug 2020
<b>International Business Machines Corp.</b> <sup>6b, 7, 16</sup>	IBM.N	Neutral		N/A	US\$124.92 18 Aug 2020
<b>Marvell Technology Group</b> <sup>16</sup>	MRVL.O	Buy		N/A	US\$33.38 18 Aug 2020
<b>NVIDIA Corp</b> <sup>13, 16</sup>	NVDA.O	Buy		N/A	US\$490.43 18 Aug 2020

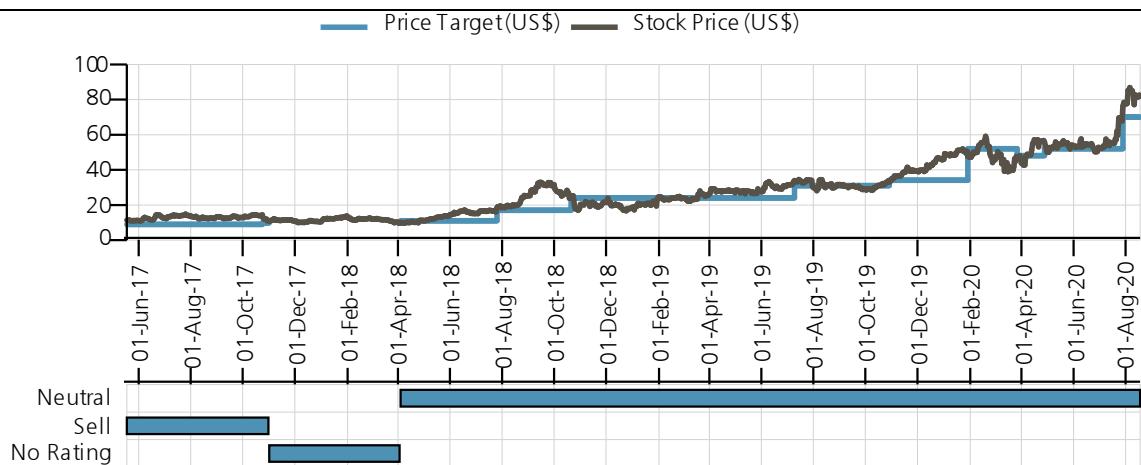
Source: UBS. All prices as of local market close.

Ratings in this table are the most current published ratings prior to this report. They may be more recent than the stock pricing date

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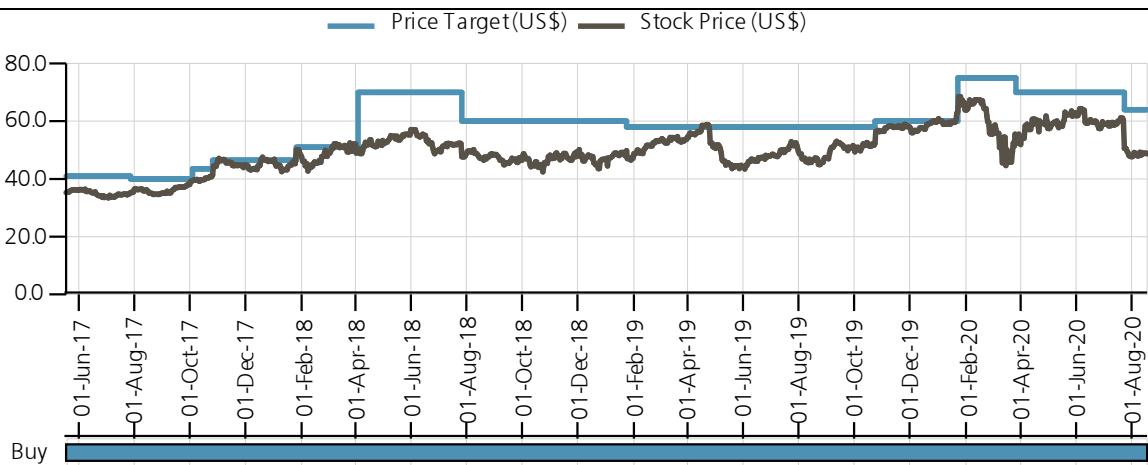
## Advanced Micro Devices Inc (US\$)



Date	Stock Price (US\$)	Price Target (US\$)	Rating
2017-05-18	11.28	9.0	Sell
2017-10-24	14.25	9.75	Sell
2017-11-01	10.8	-	No Rating
2018-04-04	9.77	11.0	Neutral
2018-07-26	18.35	17.0	Neutral
2018-10-21	23.66	25.0	Neutral
2018-10-24	22.79	24.0	Neutral
2019-07-10	33.79	31.0	Neutral
2019-10-29	33.03	34.0	Neutral
2020-01-29	47.51	52.0	Neutral
2020-03-27	46.58	48.0	Neutral
2020-04-28	55.51	52.0	Neutral
2020-07-29	76.09	70.0	Neutral

Source: UBS; as of 18 Aug 2020

## Intel Corp. (US\$)

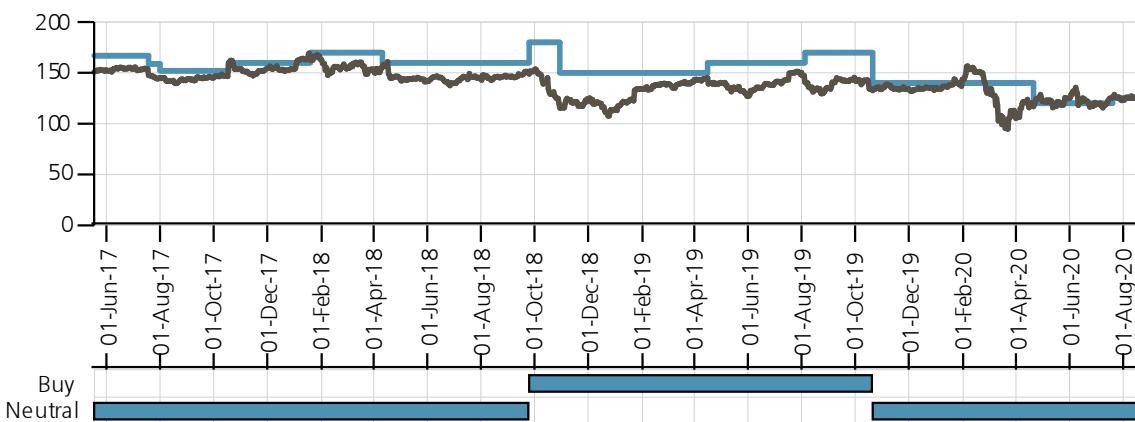


Date	Stock Price (US\$)	Price Target (US\$)	Rating
2017-05-18	35.22	41.0	Buy
2017-07-28	35.31	40.0	Buy
2017-10-04	39.34	43.5	Buy
2017-10-26	41.35	46.5	Buy
2018-01-26	50.08	51.0	Buy
2018-04-04	49.99	70.0	Buy
2018-07-27	47.68	60.0	Buy
2019-01-24	49.76	58.0	Buy
2019-10-24	52.23	60.0	Buy
2020-01-23	63.32	75.0	Buy
2020-03-27	52.37	70.0	Buy
2020-07-24	50.59	64.0	Buy

Source: UBS; as of 18 Aug 2020

### International Business Machines Corp. (US\$)

— Price Target(US\$) — Stock Price (US\$)

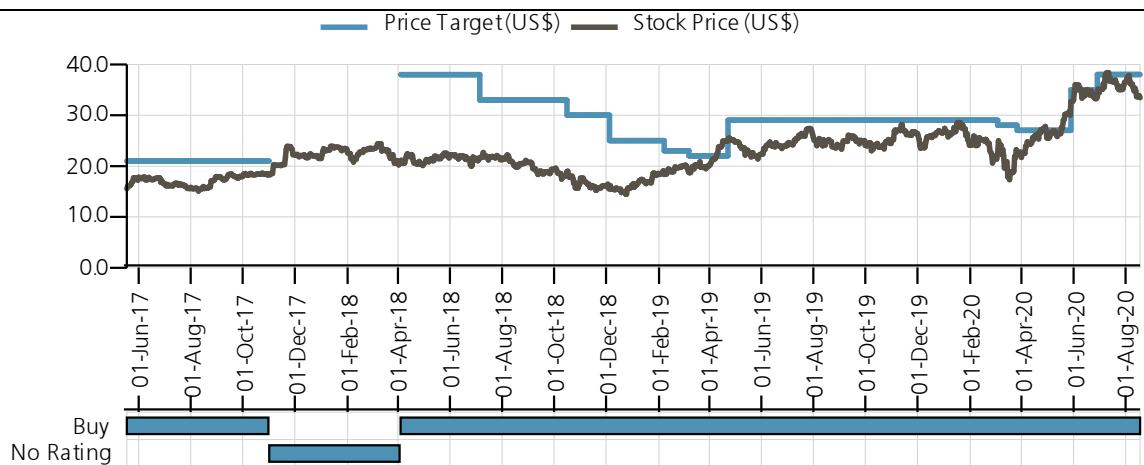


Buy  
Neutral

Date	Stock Price (US\$)	Price Target (US\$)	Rating
2017-05-18	150.78	167.0	Neutral
2017-07-19	147.53	159.0	Neutral
2017-08-01	145.3	152.0	Neutral
2017-10-18	159.53	160.0	Neutral
2018-01-19	162.37	170.0	Neutral
2018-04-11	155.36	160.0	Neutral
2018-09-25	148.91	180.0	Buy
2018-10-30	115.4	150.0	Buy
2019-04-16	145.14	160.0	Buy
2019-08-05	140.76	170.0	Buy
2019-10-21	132.58	140.0	Neutral
2020-04-21	116.76	120.0	Neutral
2020-07-20	126.37	125.0	Neutral

Source: UBS; as of 18 Aug 2020

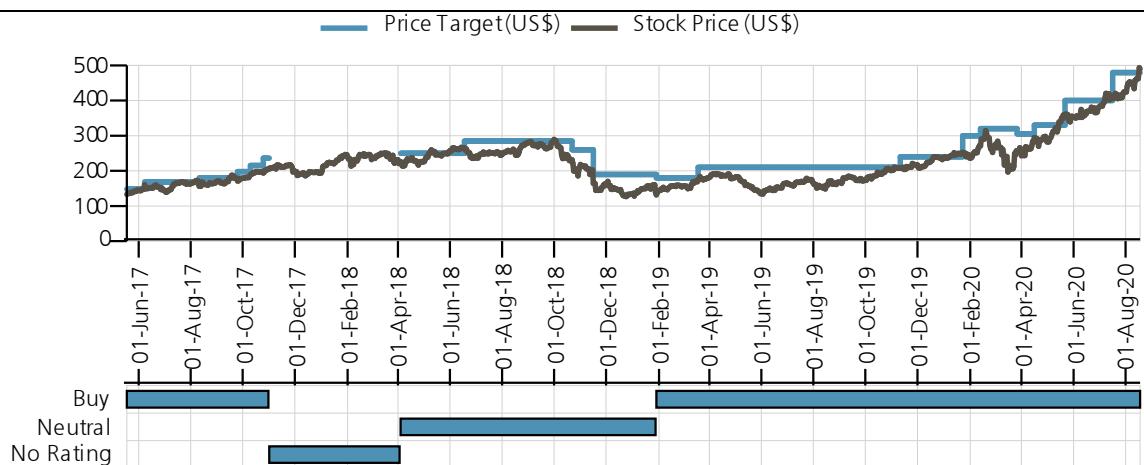
## Marvell Technology Group (US\$)



Date	Stock Price (US\$)	Price Target (US\$)	Rating
2017-05-18	15.51	21.0	Buy
2017-11-01	18.29	-	No Rating
2018-04-04	20.8	38.0	Buy
2018-07-06	21.63	33.0	Buy
2018-10-16	18.87	30.0	Buy
2018-12-05	15.5	25.0	Buy
2019-02-07	18.33	23.0	Buy
2019-03-08	18.68	22.0	Buy
2019-04-23	25.12	29.0	Buy
2020-03-04	22.59	28.0	Buy
2020-03-27	22.35	27.0	Buy
2020-05-29	32.62	35.0	Buy
2020-06-29	33.56	38.0	Buy

Source: UBS; as of 18 Aug 2020

## NVIDIA Corp (US\$)



Date	Stock Price (US\$)	Price Target (US\$)	Rating
2017-05-18	133.07	148.0	Buy
2017-06-08	159.94	168.0	Buy
2017-08-11	155.96	180.0	Buy
2017-09-25	171.0	198.0	Buy
2017-10-10	188.93	215.0	Buy
2017-10-25	193.66	236.0	Buy
2017-11-01	207.2	-	No Rating
2018-04-04	226.24	250.0	Neutral
2018-06-18	265.09	285.0	Neutral
2018-10-22	231.22	260.0	Neutral
2018-11-16	164.43	190.0	Neutral
2019-01-29	131.6	180.0	Buy
2019-03-19	175.71	210.0	Buy
2019-11-11	208.18	240.0	Buy
2020-01-23	252.86	300.0	Buy
2020-02-13	270.78	320.0	Buy
2020-03-27	252.73	305.0	Buy
2020-04-16	294.7	330.0	Buy
2020-05-22	361.05	400.0	Buy
2020-07-17	408.06	480.0	Buy

Source: UBS; as of 18 Aug 2020

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