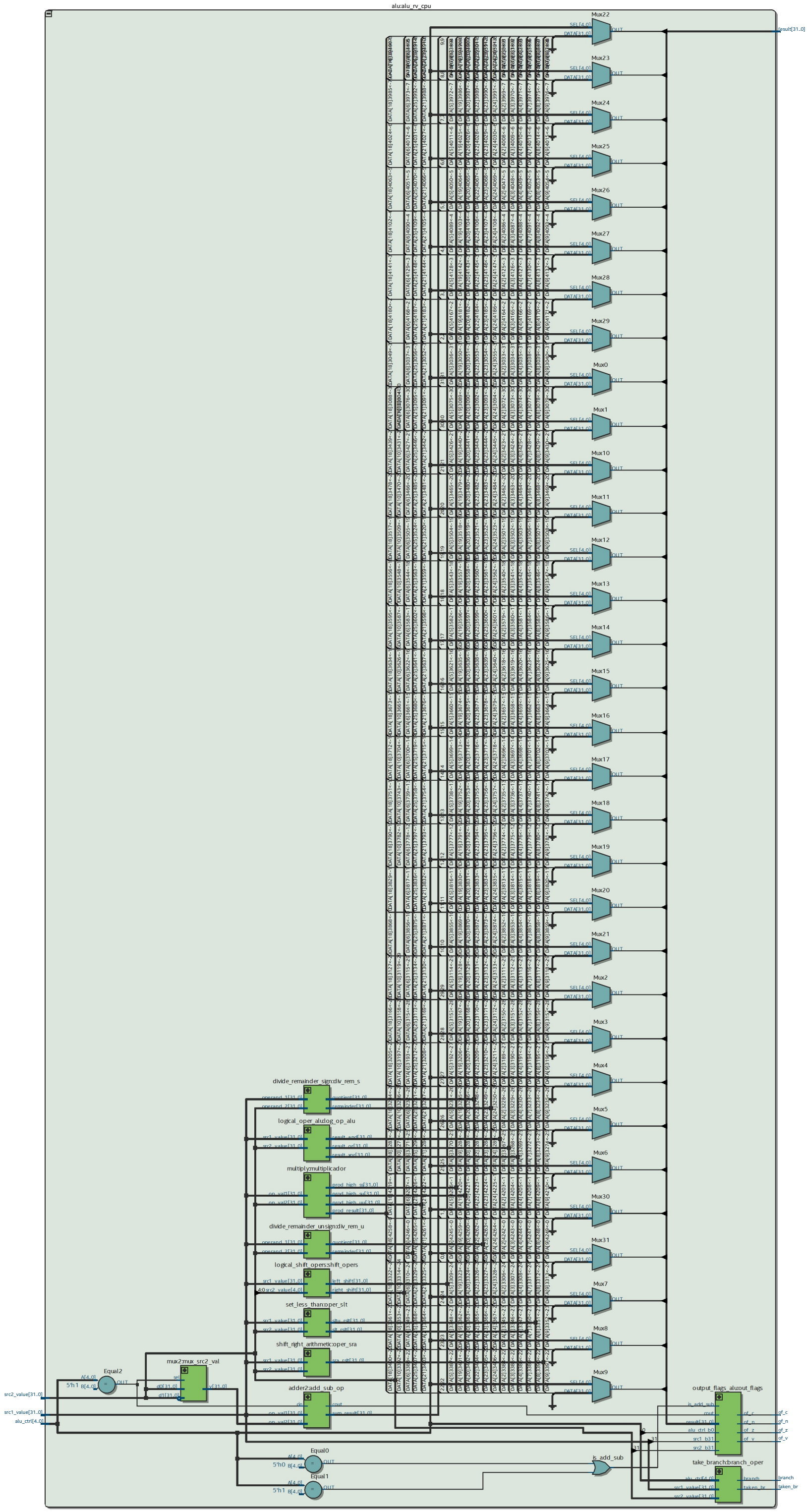
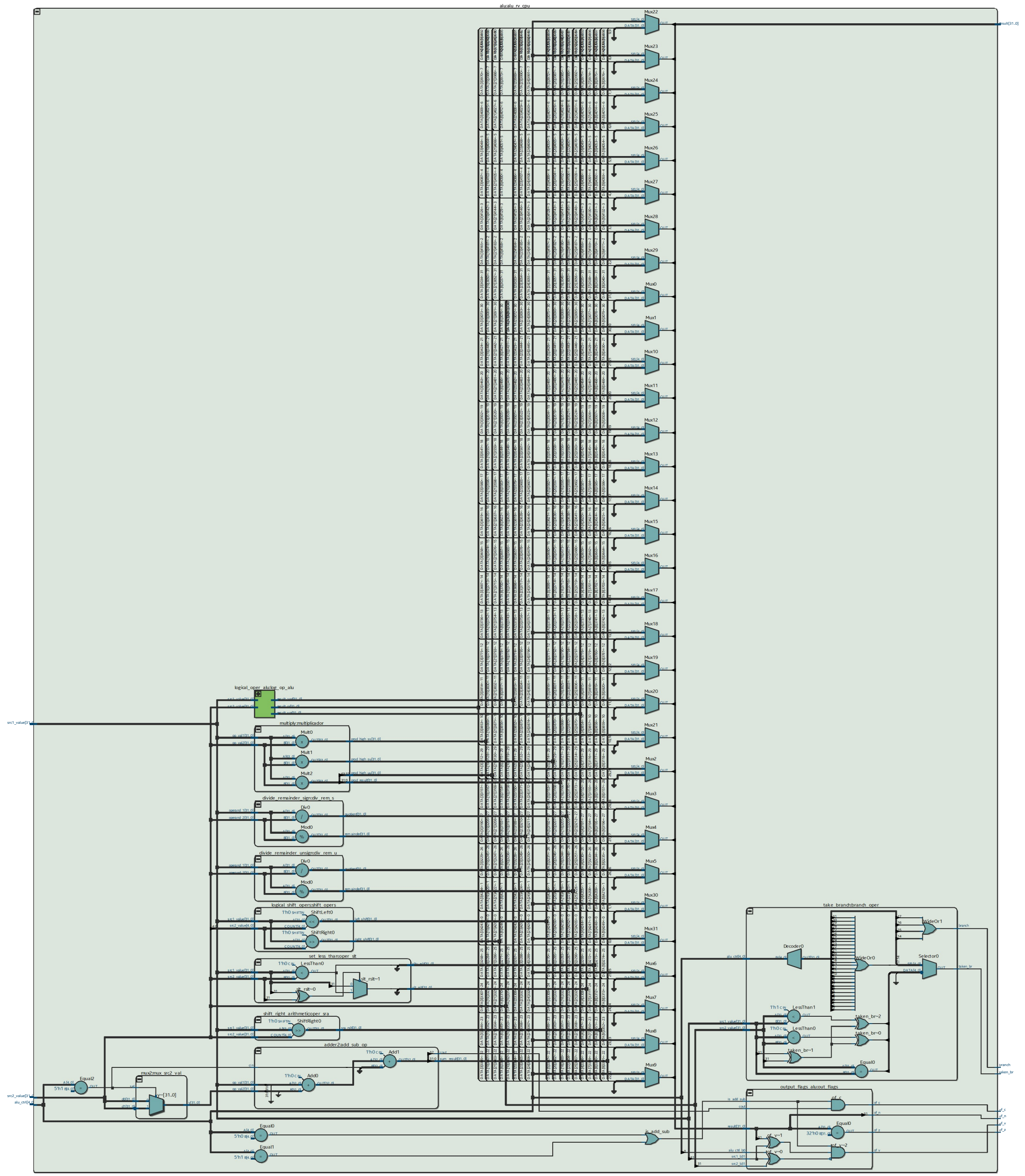

alu:alu_rv_cpu
Mux22
Mux23
Mux24
Mux25
Mux26
Mux27
Mux28
Mux29
Mux0
Mux1
Mux10
Mux11
Mux12
Mux13
Mux14
Mux15
Mux16
Mux17
Mux18
Mux19
Mux20
Mux21
Mux2
Mux3
Mux4
Mux5
Mux6
Mux30
Mux31
Mux7
Mux8
Mux9
result[31..0]
divide_remainder_sign:div_rem_s
logical_oper_alu:log_op_alu
multiply:multiplicador
divide_remainder_unsign:div_rem_u
logical_shift_opers:shift_opers
set_less_than:oper_slt
shift_right_arithmetic:oper_sra
mux2:mux_src2_val
adder2:add_sub_op
Equal2
Equal0
Equal1
is_add_sub
output_flags_alu:out_flags
take_branch:branch_oper
src2_value[31..0]
src1_value[31..0]
alu_ctrl[4..0]


alu:alu_rv_cpu
result[31..0]
src1_value[31..0]
src2_value[31..0]
alu_ctrl[4..0]
logical_oper_alu:log_op_alu
multiply:multiplicador
Mult0
Mult1
Mult2
divide_remainder_sign:div_rem_s
Div0
Mod0
divide_remainder_unsign:div_rem_u
logical_shift_opers:shift_opers
ShiftLeft0
ShiftRight0
set_less_than:oper_slt
LessThan0
slt_rslt~0
slt_rslt~1
shift_right_arithmetic:oper_sra
adder2:add_sub_op
Add1
Add0
mux2:mux_src2_val
Equal2
Equal0
Equal1
take_branch:branch_oper
Decoder0
WideOr0
WideOr1
Selector0
LessThan1
taken_br~2
taken_br~0
taken_br~1
branch
taken_br
output_flags_alu:out_flags
of_c
of_v~1
of_v~0
of_v~2
is_add_sub
Mux0
Mux1
Mux2
Mux3
Mux4
Mux5
Mux6
Mux7
Mux8
Mux9
Mux10
Mux11
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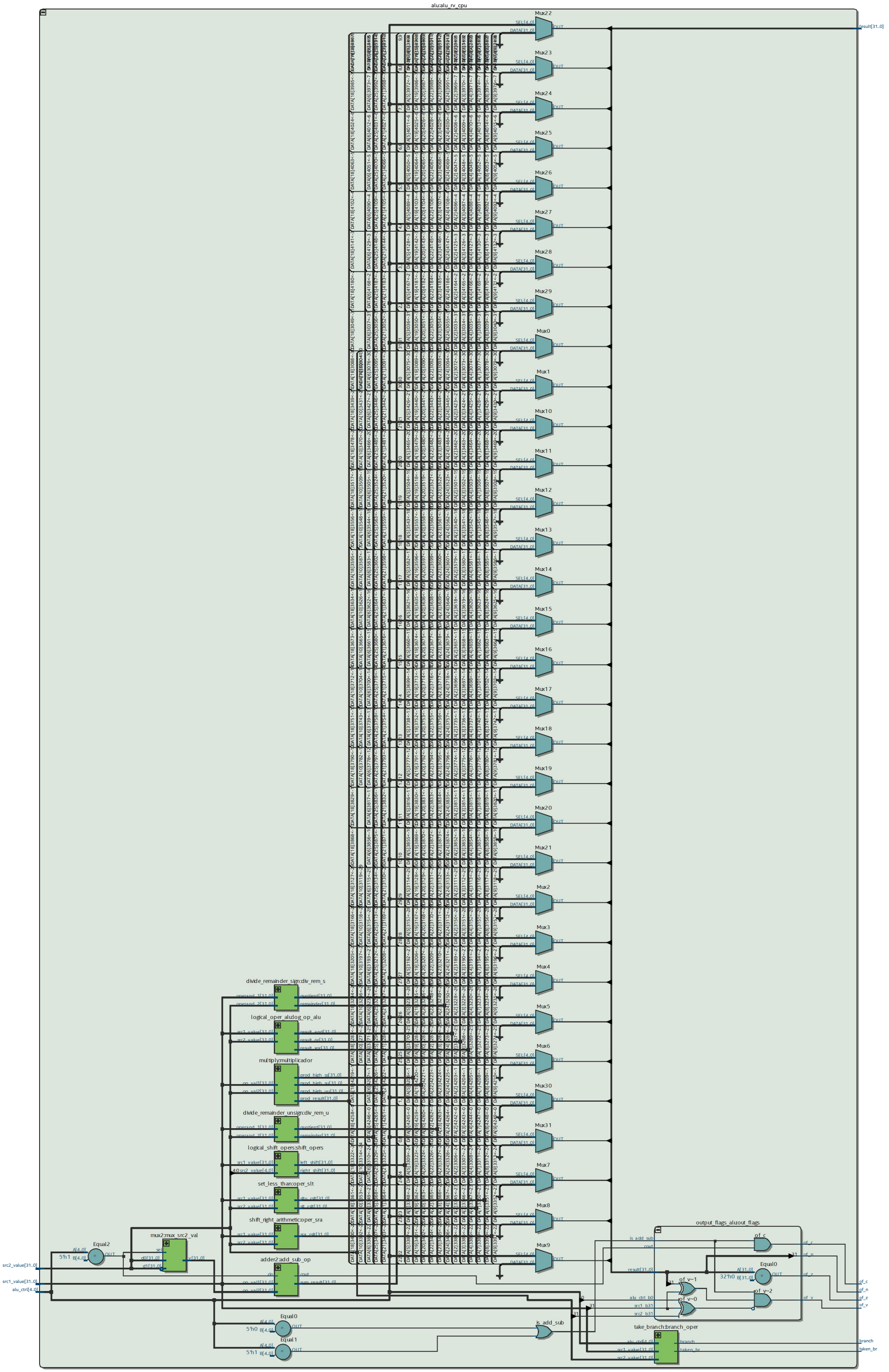
Mux29
Mux30
Mux31


alu:alu_rv_cpu
result[31..0]
divide_remainder_sign:div_rem_s
logical_oper_alu:log_op_alu
multiply:multiplicador
divide_remainder_unsign:div_rem_u
logical_shift_opers:shift_opers
set_less_than:oper_slt
shift_right_arithmetic:oper_sra
mux2:mux_src2_val
adder2:add_sub_op
Equal2
Equal0
Equal1
output_flags_alu:out_flags
take_branch:branch_oper
is_add_sub
src2_value[31..0]
src1_value[31..0]
alu_ctrl[4..0]
branch
taken_br
of_c
of_n
of_z
of_v

User Flash Memory