

1. Description

1.1. Project

Project Name	ps_vcu
Board Name	custom
Generated with:	STM32CubeMX 6.6.1
Date	04/10/2025

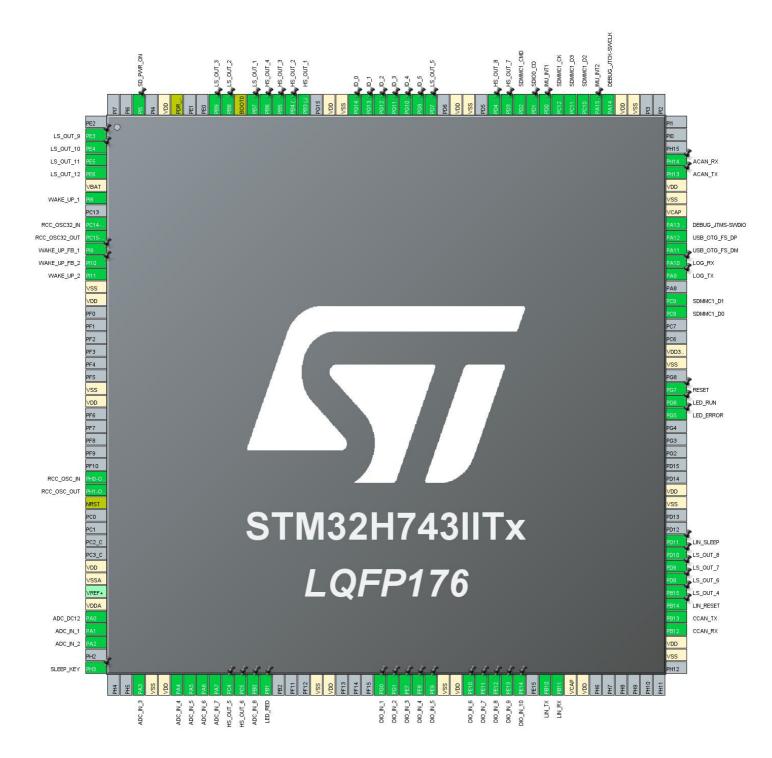
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743IITx
MCU Package	LQFP176
MCU Pin number	176

1.3. Core(s) information

Core(s)	ARM Cortex-M7

2. Pinout Configuration



3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP176	(function after		Function(s)	
	reset)		,	
2	PE3 *	I/O	GPIO_Output	LS_OUT_9
3	PE4 *	1/0	GPIO_Output	LS_OUT_10
4	PE5	I/O	TIM15_CH1	LS_OUT_11
5	PE6	I/O	TIM15_CH2	LS_OUT_12
6	VBAT	Power	111113_0112	L3_001_12
7	PI8	I/O	PWR_WKUP3	WAKE_UP_1
9	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	WARE_OI_I
10	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
11	PI9 *	I/O	GPIO_Output	WAKE_UP_FB_1
12	PI10 *	I/O	GPIO_Output	WAKE_UP_FB_2
13	PI11	I/O	PWR_WKUP4	WAKE_UP_2
14	VSS	Power		
15	VDD	Power		
22	VSS	Power		
23	VDD	Power		
29	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
30	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
31	NRST	Reset		
36	VDD	Power		
37	VSSA	Power		
39	VDDA	Power		
40	PA0	I/O	ADC1_INP16	ADC_DC12
41	PA1	I/O	ADC1_INP17	ADC_IN_1
42	PA2	I/O	ADC1_INP14	ADC_IN_2
44	PH3 *	I/O	GPIO_Input	SLEEP_KEY
47	PA3	I/O	ADC1_INP15	ADC_IN_3
48	VSS	Power		
49	VDD	Power		
50	PA4	I/O	ADC1_INP18	ADC_IN_4
51	PA5	I/O	ADC1_INP19	ADC_IN_5
52	PA6	I/O	ADC1_INP3	ADC_IN_6
53	PA7	I/O	ADC1_INP7	ADC_IN_7
54	PC4 *	I/O	GPIO_Output	HS_OUT_5
55	PC5 *	I/O	GPIO_Output	HS_OUT_6

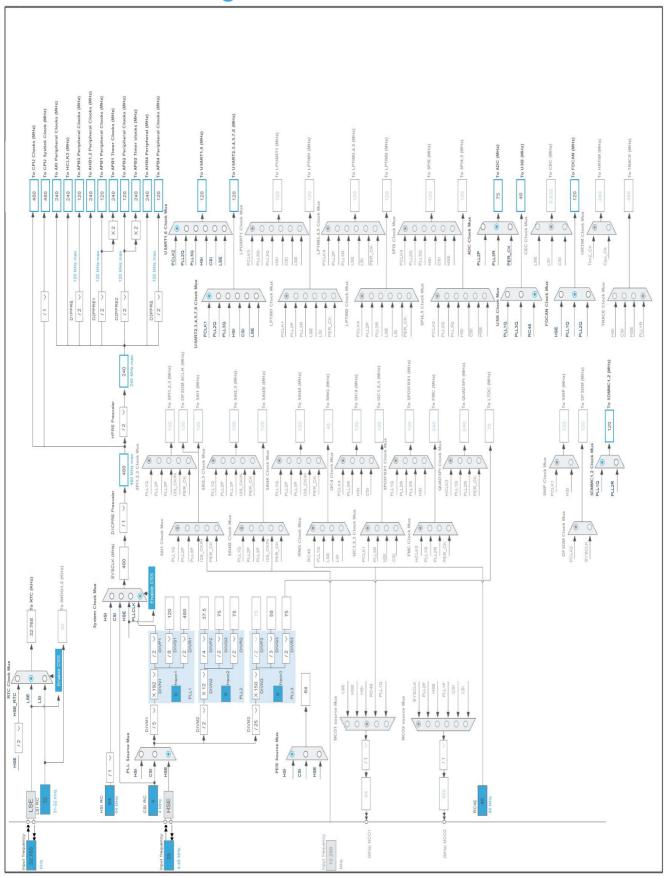
Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP176	(function after		Function(s)	
	reset)			
56	PB0	I/O	ADC1_INP9	ADC_IN_8
57	PB1	I/O	TIM3_CH4	LED_RED
61	VSS	Power	111110_0114	LED_KED
62	VDD	Power		
66	PG0 *	I/O	GPIO_Input	DIO_IN_1
67	PG1 *	1/0	GPIO_Input	DIO_IN_2
68	PE7 *	1/0	GPIO_Input	DIO_IN_3
69	PE8 *	1/0	GPIO_Input	DIO_IN_4
70	PE9 *	1/0	GPIO_Input	DIO_IN_5
71	VSS	Power	Or IO_IIIput	DIO_II1_3
72	VDD	Power		
73	PE10 *	I/O	GPIO_Input	DIO_IN_6
74	PE11 *	1/0	GPIO_Input	DIO_IN_7
75	PE12 *	1/0	GPIO_Input	DIO_IN_8
76	PE13 *	1/0	GPIO_Input	DIO_IN_9
	PE13 *	I/O		
77			GPIO_Input	DIO_IN_10
79	PB10	1/0	USART3_TX	LIN_TX
80	PB11	I/O	USART3_RX	LIN_RX
81	VCAP	Power		
82	VDD	Power		
90	VSS	Power		
91	VDD	Power		
92	PB12	I/O	FDCAN2_RX	CCAN_RX
93	PB13	I/O	FDCAN2_TX	CCAN_TX
94	PB14 *	I/O	GPIO_Output	LIN_RESET
95	PB15	I/O	TIM12_CH2	LS_OUT_4
96	PD8 *	I/O	GPIO_Output	LS_OUT_6
97	PD9 *	I/O	GPIO_Output	LS_OUT_7
98	PD10 *	I/O	GPIO_Output	LS_OUT_8
99	PD11 *	I/O	GPIO_Output	LIN_SLEEP
102	VSS	Power		
103	VDD	Power		
109	PG5 *	I/O	GPIO_Output	LED_ERROR
110	PG6 *	I/O	GPIO_Output	LED_RUN
111	PG7 *	I/O	GPIO_Output	RESET
113	VSS	Power		
114	VDD33_USB	Power		
117	PC8	I/O	SDMMC1_D0	
118	PC9	I/O	SDMMC1_D1	

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP176	(function after		Function(s)	
2011110	reset)		r directori(e)	
120	PA9	I/O	LICADTA TV	LOC TY
120			USART1_TX	LOG_TX
121	PA10	1/0	USART1_RX	LOG_RX
122	PA11	I/O	USB_OTG_FS_DM	
123	PA12	I/O	USB_OTG_FS_DP	
124	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
125	VCAP	Power		
126	VSS	Power		
127	VDD	Power		
128	PH13	I/O	FDCAN1_TX	ACAN_TX
129	PH14	I/O	FDCAN1_RX	ACAN_RX
135	VSS	Power		
136	VDD	Power		
137	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
138	PA15 (JTDI) *	I/O	GPIO_Input	IMU_INT2
139	PC10	I/O	SDMMC1_D2	
140	PC11	I/O	SDMMC1_D3	
141	PC12	I/O	SDMMC1_CK	
142	PD0 *	I/O	GPIO_Input	IMU_INT1
143	PD1 *	I/O	GPIO_Input	SDIO0_CD
144	PD2	I/O	SDMMC1_CMD	
145	PD3 *	I/O	GPIO_Output	HS_OUT_7
146	PD4 *	I/O	GPIO_Output	HS_OUT_8
148	VSS	Power		
149	VDD	Power		
151	PD7 *	I/O	GPIO_Output	LS_OUT_5
152	PG9 *	I/O	GPIO_Input	ID_5
153	PG10 *	I/O	GPIO_Input	ID_4
154	PG11 *	I/O	GPIO_Input	ID_3
155	PG12 *	I/O	GPIO_Input	ID_2
156	PG13 *	I/O	GPIO_Input	ID_1
157	PG14 *	I/O	GPIO_Input	ID_0
158	VSS	Power		
159	VDD	Power		
161	PB3 (JTDO/TRACESWO)	I/O	TIM2_CH2	HS_OUT_1
162	PB4 (NJTRST)	I/O	TIM3_CH1	HS_OUT_2
163	PB5	I/O	TIM3_CH2	HS_OUT_3
164	PB6	I/O	TIM4_CH1	HS_OUT_4
165	PB7	I/O	TIM4_CH2	LS_OUT_1
166	воото	Boot	0112	
.00				

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
167	PB8	I/O	TIM4_CH3	LS_OUT_2
168	PB9	I/O	TIM4_CH4	LS_OUT_3
171	PDR_ON	Reset		
172	VDD	Power		
174	PI5 *	I/O	GPIO_Output	SD_PWR_ON

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



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5. Software Project

5.1. Project Settings

Name	Value
Project Name	ps_vcu
Project Folder	D:\ddl\work\VCU\ps_vcu\board\stm32h743iit6
Toolchain / IDE	MDK-ARM V5.32
Firmware Package Name and Version	STM32Cube FW_H7 V1.10.0
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x800

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_FDCAN1_Init	FDCAN1
4	MX_FDCAN2_Init	FDCAN2
5	MX_RTC_Init	RTC
6	MX_USART1_UART_Init	USART1
7	MX_TIM13_Init	TIM13
8	MX_ADC1_Init	ADC1
9	MX_USART3_UART_Init	USART3
10	MX_ADC3_Init	ADC3
11	MX_TIM3_Init	TIM3

Rank	Function Name	Peripheral Instance Name
12	MX_TIM2_Init	TIM2
13	MX_TIM4_Init	TIM4
14	MX_TIM12_Init	TIM12
15	MX_TIM15_Init	TIM15
16	MX_SDMMC1_SD_Init	SDMMC1
17	MX_FATFS_Init	FATFS
18	MX_USB_DEVICE_Init	USB_DEVICE

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743IITx
Datasheet	DS12110_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

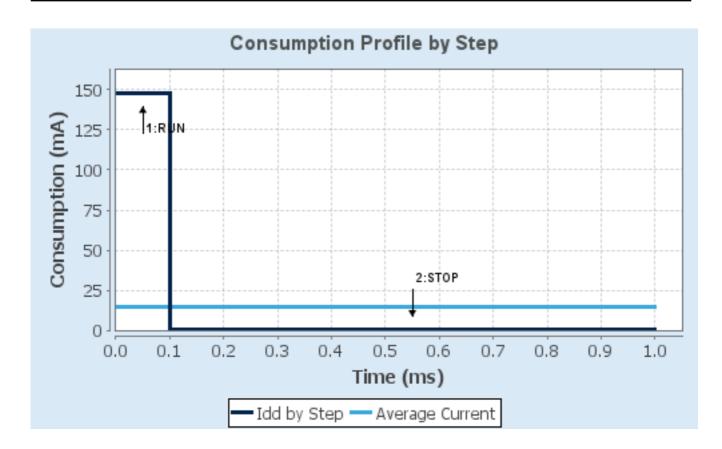
6.4. Sequence

	1	
Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0-High	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	ITCM	NA
CPU Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL	Flash-OFF
Clock Source Frequency	24 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	148 mA	150 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Ta Max	105.91	124.98
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	14.94 mA
Battery Life	1 day, 17 hours	Average DMIPS	1027.2001
			DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1

IN3: IN3 Single-ended

mode: IN7 mode: IN9 mode: IN14 mode: IN15

IN16: IN16 Single-ended

mode: IN17

IN18: IN18 Single-ended

mode: IN19

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

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src='jar:file:/D:/Program%20Files/STMicroelectronics/STM32Cube/STM32CubeMX/STM32CubeMX.exe!/c om/st/microxplorer/image/snk/error.png'

ADC_Settings</html>:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 16-bit resolution

Scan Conversion Mode Enabled

Continuous Conversion Mode Enabled *

Discontinuous Conversion Mode Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data overwritten *

Left Bit Shift No bit shift

Conversion Data Management Mode

DMA Circular Mode *

Low Power Auto Wait Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable
Enable Regular Oversampling Disable
Number Of Conversion 9 *

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None
Rank 1

Channel 16 *
Sampling Time 810.5 Cycles *

Offset Number No offset
Offset Signed Saturation Disable
Rank 2 *

Channel 17 *
Sampling Time 810.5 Cycles *

Offset Number No offset
Offset Signed Saturation Disable
Rank 3 *

Channel 14 *
Sampling Time 810.5 Cycles *

Offset Number No offset
Offset Signed Saturation Disable
Rank 4 *

Channel 15 *
Sampling Time 810.5 Cycles *

Offset Number No offset
Offset Signed Saturation Disable
Rank 5 *

Channel 18 *
Sampling Time 810.5 Cycles *

Offset Number No offset
Offset Signed Saturation Disable

Rank 6 *

Channel 19 *
Sampling Time 810.5 Cycles *

 Offset Number
 No offset

 Offset Signed Saturation
 Disable

 Rank
 7 *

 Channel
 Channel 3

Sampling Time 810.5 Cycles *

Offset Number No offset
Offset Signed Saturation Disable
Rank 8 *

Channel 7 *
Sampling Time 810.5 Cycles *

Offset Number No offset
Offset Signed Saturation Disable
Rank 9 *

Channel 9 *

Sampling Time 810.5 Cycles *

Offset Number No offset
Offset Signed Saturation Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

7.2. ADC3

mode: Temperature Sensor Channel

7.2.1. Parameter Settings:

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ADC_Settings</html>:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 16-bit resolution

Scan Conversion Mode

Continuous Conversion Mode

Discontinuous Conversion Mode

Disabled

Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data overwritten *

Left Bit Shift No bit shift

Low Power Auto Wait Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable
Enable Regular Oversampling Disable
Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None Rank 1

Channel Channel Temperature Sensor

Sampling Time 810.5 Cycles *

Offset Number No offset
Offset Signed Saturation Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

7.3. CORTEX M7

7.3.1. Parameter Settings:

Speculation default mode Settings:

Speculation default mode Disabled

Cortex Interface Settings:

CPU ICache Enabled *
CPU DCache Enabled *

Cortex Memory Protection Unit Control Settings:

MPU Control Mode

Background Region Privileged accesses only + MPU Enabled

during hard fault, NMI and FAULTMASK handlers *

Cortex Memory Protection Unit Region 0 Settings:

MPU Region Enabled *

MPU Region Base Address 0x20000000 *

MPU Region Size

MPU SubRegion Disable

0x0 *

MPU TEX field level level 0

MPU Access Permission ALL ACCESS PERMITTED *

MPU Instruction Access ENABLE
MPU Shareability Permission DISABLE
MPU Cacheable Permission ENABLE *
MPU Bufferable Permission ENABLE *

Cortex Memory Protection Unit Region 1 Settings:

MPU Region Enabled *

MPU Region Base Address 0x24000000 *

MPU Region Size 512KB *

MPU SubRegion Disable

0x0 *

MPU TEX field level level 0

MPU Access Permission ALL ACCESS PERMITTED *

MPU Instruction Access ENABLE

MPU Shareability Permission ENABLE *

MPU Cacheable Permission ENABLE *

MPU Bufferable Permission DISABLE

Cortex Memory Protection Unit Region 2 Settings:

MPU Region Enabled *

MPU Region Base Address 0x30000000 *

MPU Region Size 512KB *
MPU SubRegion Disable 0x0 *
MPU TEX field level level 0

MPU Access Permission ALL ACCESS PERMITTED *

MPU Instruction Access ENABLE

MPU Shareability Permission DISABLE

MPU Cacheable Permission ENABLE *

MPU Bufferable Permission ENABLE *

Cortex Memory Protection Unit Region 3 Settings:

MPU Region Enabled *

MPU Region Base Address 0x38000000 *

MPU Region Size 64KB *

MPU SubRegion Disable 0x0 *

MPU TEX field level level 0

MPU Access Permission ALL ACCESS PERMITTED *

MPU Instruction Access ENABLE

MPU Shareability Permission DISABLE

MPU Cacheable Permission ENABLE *

MPU Bufferable Permission ENABLE *

Cortex Memory Protection Unit Region 4 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 5 Settings:

MPU Region

Disabled

Cortex Memory Protection Unit Region 6 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 7 Settings:

MPU Region

Disabled

Cortex Memory Protection Unit Region 8 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 9 Settings:

MPU Region Disable

Cortex Memory Protection Unit Region 10 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 11 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 12 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 13 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 14 Settings:

MPU Region Disabled

Cortex Memory Protection Unit Region 15 Settings:

MPU Region Disabled

7.4. DEBUG

Debug: Serial Wire

7.5. FDCAN1

mode: Activated

7.5.1. Parameter Settings:

Basic Parameters:

Frame Format Classic mode

Mode Normal mode

Auto Retransmission Disable

Transmit Pause Disable

Protocol Exception Enable *

Nominal Sync Jump Width 8 *

Data Prescaler 6 *

Data Sync Jump Width 8 *

Data Time Seg1 31 *

Data Time Seg2 8 *

Message Ram Offset 0

Std Filters Nbr 128 *

Ext Filters Nbr 0

Rx Fifo0 Elmts Nbr 32 *

Rx Fifo0 Elmt Size 8 bytes data field

Rx Fifo1 Elmts Nbr 0

Rx Fifo1 Elmt Size 8 bytes data field

Rx Buffers Nbr 0

Rx Buffer Size 8 bytes data field

Tx Events Nbr 0
Tx Buffers Nbr 0

Tx Fifo Queue Elmts Nbr 32 *

Tx Fifo Queue Mode FIFO mode
Tx Elmt Size 8 bytes data field

Clock Calibration Unit:

Clock Calibration Disable

Bit Timings Parameters:

Nominal Prescaler 6 *

Nominal Time Quantum 50.0 *
Nominal Time Seg1 31 *
Nominal Time Seg2 8 *

Nominal Time for one Bit 2000 *

Nominal Baud Rate 500000 *

7.6. FDCAN2

mode: Activated

7.6.1. Parameter Settings:

Basic Parameters:

Frame Format Classic mode

Mode Normal mode

Auto Retransmission Disable

Transmit Pause Disable

Protocol Exception Enable *

Nominal Sync Jump Width 8 *

Data Prescaler 6 *

Data Sync Jump Width 8 *

Data Time Seg1 31 *

Data Time Seg2 8 *

Message Ram Offset 0x406 *

Std Filters Nbr 1 *

Ext Filters Nbr 0 Rx Fifo0 Elmts Nbr 0

Rx Fifo0 Elmt Size 8 bytes data field

Rx Fifo1 Elmts Nbr 32 *

Rx Fifo1 Elmt Size 8 bytes data field

Rx Buffers Nbr

Rx Buffer Size 8 bytes data field

Tx Events Nbr 0 Tx Buffers Nbr 0 Tx Fifo Queue Elmts Nbr 32 *

Tx Fifo Queue Mode FIFO mode Tx Elmt Size 8 bytes data field

Clock Calibration Unit:

Clock Calibration Disable

Bit Timings Parameters:

Nominal Prescaler 6 *

Nominal Time Quantum 50.0 * Nominal Time Seg1 31 * Nominal Time Seg2 8 *

2000 * Nominal Baud Rate 500000 *

7.7. PWR

mode: Wake-Up 3 mode: Wake-Up 4

Nominal Time for one Bit

7.8. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator Low Speed Clock (LSE): Crystal/Ceramic Resonator

7.8.1. Parameter Settings:

Power Parameters:

PWR_LDO_SUPPLY SupplySource

Power Regulator Voltage Scale Power Regulator Voltage Scale 0

RCC Parameters:

TIM Prescaler Selection Disabled HSE Startup Timout Value (ms) 100 LSE Startup Timout Value (ms) 5000

LSE Drive Capability

LSE oscillator low drive capability

CSI Calibration Value 16
HSI Calibration Value 32

System Parameters:

VDD voltage (V) 3.3

Flash Latency(WS) 4 WS (5 CPU cycle)

Product revision rev.Y

PLL range Parameters:

PLL1 clock Input range Between 4 and 8 MHz
PLL3 input frequency range Between 1 and 2 MHz
PLL1 clock Output range Wide VCO range
PLL3 clock Output range MEDIUM VCO range

7.9. RTC

mode: Activate Clock Source mode: Activate Calendar 7.9.1. Parameter Settings:

General:

Hour Format Hourformat 24

Asynchronous Predivider value 127
Synchronous Predivider value 255

Calendar Time:

Data Format Binary data format *

Hours 14 *
Minutes 16 *
Seconds 30 *

Day Light Saving: value of hour adjustment Daylightsaving None Store Operation Storeoperation Reset

Calendar Date:

Week Day Wednesday *

Month March *
Date 20 *
Year 55 *

7.10. SDMMC1

Mode: SD 4 bits Wide bus 7.10.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made Rising transition

SDMMC Clock output enable when the bus is idle

Disable the power save for the clock

SDMMC hardware flow control

The hardware control flow is disabled

SDMMC clock divide factor 4 *
Is external transceiver present ? no

7.11. SYS

Timebase Source: TIM7

7.12. TIM2

Clock Source : Internal Clock Channel2: PWM Generation CH2

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 2399 *

Counter Mode Up

Counter Period (AutoReload Register - 32 bits value) 49999 *

Internal Clock Division (CKD) No Division auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source Disable

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (32 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

7.13. TIM3

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2 Channel4: PWM Generation CH4

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 2399 *

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 4999 *
Internal Clock Division (CKD) No Division

auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source Disable

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

PWM Generation Channel 4:

Mode PWM mode 1
Pulse (16 bits value) 50000 *
Output compare preload Enable

Fast Mode Disable CH Polarity High

7.14. TIM4

Clock Source: Internal Clock
Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 2399 *
Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 4999 *

Internal Clock Division (CKD) No Division auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source Disable

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

PWM Generation Channel 2:

Mode PWM mode 1
Pulse (16 bits value) 50000 *

Output compare preload Enable
Fast Mode Disable
CH Polarity High

PWM Generation Channel 3:

Mode PWM mode 1
Pulse (16 bits value) 50000 *

Output compare preload Enable
Fast Mode Disable
CH Polarity High

PWM Generation Channel 4:

ModePWM mode 1Pulse (16 bits value)**50000** *Output compare preloadEnableFast ModeDisableCH PolarityHigh

7.15. TIM12

Channel2: PWM Generation CH2

7.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

auto-reload preload

A399 *

49999 *

Disable

Clear Input:

Clear Input Source Disable

PWM Generation Channel 2:

Mode PWM mode 1
Pulse (16 bits value) 50000 *

Output compare preload Enable
Fast Mode Disable
CH Polarity High

7.16. TIM13

mode: Activated

7.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

Auto-reload preload

Separation (PSC - 16 bits value)

Up

Separation (PSC - 16 bits value)

Separation (PSC - 1

7.17. TIM15

mode: Clock Source

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2

7.17.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 2399 *
Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 49999 *
Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 8 bits value) 0
auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State Disable
BRK Polarity High
BRK Filter (4 bits value) 0

BRK Sources Configuration

Digital Input
 COMP1
 COMP2
 Disable
 DFSDM
 Disable

Break And Dead Time management - Output Configuration:

Automatic Output State Disable
Off State Selection for Run Mode (OSSR) Disable
Off State Selection for Idle Mode (OSSI) Disable
Lock Configuration Off

PWM Generation Channel 1:

Mode PWM mode 1
Pulse (16 bits value) 50000 *

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

PWM Generation Channel 2:

Mode PWM mode 1
Pulse (16 bits value) 50000 *

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

7.18. USART1

Mode: Asynchronous

7.18.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
ClockPrescaler 1

Fifo Mode Disable

Txfifo Threshold 1 eighth full configuration Rxfifo Threshold 1 eighth full configuration

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable Disable **RX Pin Active Level Inversion** Disable Data Inversion TX and RX Pins Swapping Disable Overrun Enable DMA on RX Error Enable MSB First Disable

7.19. USART3

Mode: LIN

7.19.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable
Break Detect Length 10 Bits
ClockPrescaler 1
Fifo Mode Disable

Txfifo Threshold 1 eighth full configuration
Rxfifo Threshold 1 eighth full configuration

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable RX Pin Active Level Inversion Disable Data Inversion Disable Disable TX and RX Pins Swapping Enable Overrun DMA on RX Error Enable MSB First Disable

7.20. USB_OTG_FS

Mode: Device_Only

7.20.1. Parameter Settings:

Speed Full Speed 12MBit/s

Enable internal IP DMA Disabled
Low power Disabled
Battery charging Disabled
Link Power Management Disabled
Use dedicated end point 1 interrupt Disabled
VBUS sensing Disabled
Signal start of frame Disabled

7.21. FATFS

mode: SD Card

7.21.1. Set Defines:

Version:

FATFS version R0.12c

Function Parameters:

FS_READONLY (Read-only mode) Disabled
FS_MINIMIZE (Minimization level) Disabled

USE_STRFUNC (String functions) Enabled with LF -> CRLF conversion

USE_FIND (Find functions)

USE_MKFS (Make filesystem function)

USE_FASTSEEK (Fast seek function)

USE_EXPAND (Use f_expand function)

USE_CHMOD (Change attributes function)

USE_LABEL (Volume label functions)

Enabled *

USE_FORWARD (Forward function)

Disabled

Disabled *

Locale and Namespace Parameters:

CODE_PAGE (Code page on target) U.S. *

USE_LFN (Use Long Filename) Enabled with dynamic working buffer on the STACK *

MAX_LFN (Max Long Filename) 255

LFN_UNICODE (Enable Unicode)

STRF_ENCODE (Character encoding)

UTF-8

FS_RPATH (Relative Path)

Disabled

Physical Drive Parameters:

VOLUMES (Logical drives) 1

MAX_SS (Maximum Sector Size) 512

MIN_SS (Minimum Sector Size) 512

MULTI_PARTITION (Volume partitions feature) Disabled

USE_TRIM (Erase feature) Disabled

FS_NOFSINFO (Force full FAT scan) 0

System Parameters:

FS_TINY (Tiny mode) Disabled
FS_EXFAT (Support of exFAT file system) Disabled

FS_NORTC (Timestamp feature) Dynamic timestamp

FS_REENTRANT (Re-Entrancy) Enabled
FS_TIMEOUT (Timeout ticks) 1000
USE_MUTEX Disabled

SYNC_t (O/S sync object) osSemaphoreId_t

FS_LOCK (Number of files opened simultaneously)

7.21.2. Advanced Settings:

SDIO/SDMMC:

SDMMC instance SDMMC1
Use dma template Enabled
BSP code for SD Generic

7.21.3. Platform Settings:

Detect_SDIO PD1

7.22. FREERTOS

Interface: CMSIS_V2

7.22.1. Config parameters:

API:

FreeRTOS API CMSIS v2

Versions:

FreeRTOS version 10.3.1 CMSIS-RTOS version 2.00

MPU/FPU:

ENABLE_MPU Disabled ENABLE_FPU Disabled

Kernel settings:

USE_PREEMPTION Enabled

CPU_CLOCK_HZ SystemCoreClock

TICK_RATE_HZ 1000 MAX_PRIORITIES 56 MINIMAL_STACK_SIZE 128 MAX_TASK_NAME_LEN 16 USE_16_BIT_TICKS Disabled IDLE_SHOULD_YIELD Enabled USE_MUTEXES Enabled USE_RECURSIVE_MUTEXES Enabled USE_COUNTING_SEMAPHORES Enabled

QUEUE_REGISTRY_SIZE 8

USE_APPLICATION_TASK_TAG Disabled

ENABLE_BACKWARD_COMPATIBILITY Enabled
USE_PORT_OPTIMISED_TASK_SELECTION Disabled
USE_TICKLESS_IDLE Disabled
USE_TASK_NOTIFICATIONS Enabled
RECORD_STACK_HIGH_ADDRESS Disabled

Memory management settings:

Memory Allocation Dynamic / Static

TOTAL_HEAP_SIZE 15360

Memory Management scheme heap 1 *

Hook function related definitions:

USE_IDLE_HOOK Disabled
USE_TICK_HOOK Disabled
USE_MALLOC_FAILED_HOOK Disabled
USE_DAEMON_TASK_STARTUP_HOOK Disabled
CHECK_FOR_STACK_OVERFLOW Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS Disabled
USE_TRACE_FACILITY Enabled
USE_STATS_FORMATTING_FUNCTIONS Disabled

Co-routine related definitions:

USE_CO_ROUTINES Disabled

MAX_CO_ROUTINE_PRIORITIES 2

Software timer definitions:

USE_TIMERS Enabled
TIMER_TASK_PRIORITY 2
TIMER_QUEUE_LENGTH 10
TIMER_TASK_STACK_DEPTH 256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY 15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY 5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE size_t
USE_POSIX_ERRNO Disabled

CMSIS-RTOS V2 flags:

USE_OS2_THREAD_SUSPEND_RESUME Enabled
USE_OS2_THREAD_ENUMERATE Enabled
USE_OS2_EVENTFLAGS_FROM_ISR Enabled
USE_OS2_THREAD_FLAGS Enabled
USE_OS2_TIMER Enabled
USE_OS2_MUTEX Enabled

7.22.2. Include parameters:

Include definitions:

vTaskPrioritySet Enabled uxTaskPriorityGet Enabled Enabled vTaskDelete Disabled vTaskCleanUpResources Enabled vTaskSuspend vTaskDelayUntil Enabled Enabled vTaskDelay Enabled xTaskGetSchedulerState xTaskResumeFromISR Enabled xQueueGetMutexHolder Enabled Disabled xSemaphoreGetMutexHolder Disabled pcTaskGetTaskName uxTaskGetStackHighWaterMark Enabled xTaskGetCurrentTaskHandle Enabled Enabled eTaskGetState xEventGroupSetBitFromISR Disabled xTimerPendFunctionCall Enabled Disabled xTaskAbortDelay xTaskGetHandle Disabled uxTaskGetStackHighWaterMark2Disabled

7.22.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT Disabled

Project settings (see parameter description first):

Use FW pack heap file Enabled

7.23. USB DEVICE

Class For FS IP: Mass Storage Class

7.23.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)

1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)

USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors) 512

USBD_SELF_POWERED (Enabled self power) Enabled

USBD_DEBUG_LEVEL (USBD Debug Level) 0: No debug message

Class Parameters:

MSC_MEDIA_PACKET (Media I/O buffer Size) 512

7.23.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier) 1155

LANGID_STRING (Language Identifier) English (United States)

MANUFACTURER_STRING (Manufacturer Identifier) STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier) 22314

PRODUCT_STRING (Product Identifier) STM32 Mass Storage

CONFIGURATION_STRING (Configuration Identifier) MSC Config
INTERFACE_STRING (Interface Identifier) MSC Interface

^{*} User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_INP16	Analog mode	No pull-up and no pull-down	n/a	ADC_DC12
	PA1	ADC1_INP17	Analog mode	No pull-up and no pull-down	n/a	ADC_IN_1
	PA2	ADC1_INP14	Analog mode	No pull-up and no pull-down	n/a	ADC_IN_2
	PA3	ADC1_INP15	Analog mode	No pull-up and no pull-down	n/a	ADC_IN_3
	PA4	ADC1_INP18	Analog mode	No pull-up and no pull-down	n/a	ADC_IN_4
	PA5	ADC1_INP19	Analog mode	No pull-up and no pull-down	n/a	ADC_IN_5
	PA6	ADC1_INP3	Analog mode	No pull-up and no pull-down	n/a	ADC_IN_6
	PA7	ADC1_INP7	Analog mode	No pull-up and no pull-down	n/a	ADC_IN_7
	PB0	ADC1_INP9	Analog mode	No pull-up and no pull-down	n/a	ADC_IN_8
DEBUG	PA13 (JTMS/SWDI O)	DEBUG_JTMS- SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWC LK)	DEBUG_JTCK- SWCLK	n/a	n/a	n/a	
FDCAN1	PH13	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	ACAN_TX
	PH14	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	ACAN_RX
FDCAN2	PB12	FDCAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	CCAN_RX
	PB13	FDCAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	CCAN_TX
PWR	PI8	PWR_WKUP3	n/a	n/a	n/a	WAKE_UP_1
	PI11	PWR_WKUP4	n/a	n/a	n/a	WAKE_UP_2
RCC	PC14- OSC32_IN (OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	
	PH0- OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SDMMC1	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
TIM2	PB3 (JTDO/TRA CESWO)	TIM2_CH2	Alternate Function Push Pull	Pull-down *	Low	HS_OUT_1
TIM3	PB1	TIM3_CH4	Alternate Function Push Pull	Pull-up *	Low	LED_RED
	PB4 (NJTRST)	TIM3_CH1	Alternate Function Push Pull	Pull-down *	Low	HS_OUT_2
	PB5	TIM3_CH2	Alternate Function Push Pull	Pull-down *	Low	HS_OUT_3
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	Pull-down *	Low	HS_OUT_4
	PB7	TIM4_CH2	Alternate Function Push Pull	Pull-up *	Low	LS_OUT_1
	PB8	TIM4_CH3	Alternate Function Push Pull	Pull-up *	Low	LS_OUT_2
	PB9	TIM4_CH4	Alternate Function Push Pull	Pull-up *	Low	LS_OUT_3
TIM12	PB15	TIM12_CH2	Alternate Function Push Pull	Pull-up *	Low	LS_OUT_4
TIM15	PE5	TIM15_CH1	Alternate Function Push Pull	Pull-up *	Low	LS_OUT_11
	PE6	TIM15_CH2	Alternate Function Push Pull	Pull-up *	Low	LS_OUT_12
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	LOG_TX
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	LOG_RX
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	LIN_TX
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	LIN_RX
USB_OTG_ FS	PA11	USB_OTG_FS_ DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	USB_OTG_FS_ DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PE3	GPIO_Output	Output Push Pull	Pull-up *	Low	LS_OUT_9
	PE4	GPIO_Output	Output Push Pull	Pull-up *	Low	LS_OUT_10
	PI9	GPIO_Output	Output Push Pull	Pull-down *	Low	WAKE_UP_FB_1
	PI10	GPIO_Output	Output Push Pull	Pull-down *	Low	WAKE_UP_FB_2
	PH3	GPIO_Input	Input mode	Pull-up *	n/a	SLEEP_KEY
	PC4	GPIO_Output	Output Push Pull	Pull-down *	Low	HS_OUT_5
	PC5	GPIO_Output	Output Push Pull	Pull-down *	Low	HS_OUT_6
	PG0	GPIO_Input	Input mode	Pull-up *	n/a	DIO_IN_1
	PG1	GPIO_Input	Input mode	Pull-up *	n/a	DIO_IN_2
	PE7	GPIO_Input	Input mode	Pull-up *	n/a	DIO_IN_3
	PE8	GPIO_Input	Input mode		n/a	DIO_IN_4

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
				Pull-up *		
	PE9	GPIO_Input	Input mode	Pull-up *	n/a	DIO_IN_5
	PE10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	DIO_IN_6
	PE11	GPIO_Input	Input mode	Pull-up *	n/a	DIO_IN_7
	PE12	GPIO_Input	Input mode	Pull-up *	n/a	DIO_IN_8
	PE13	GPIO_Input	Input mode	Pull-up *	n/a	DIO_IN_9
	PE14	GPIO_Input	Input mode	Pull-up *	n/a	DIO_IN_10
	PB14	GPIO_Output	Output Push Pull	Pull-up *	Low	LIN_RESET
	PD8	GPIO_Output	Output Push Pull	Pull-up *	Low	LS_OUT_6
	PD9	GPIO_Output	Output Push Pull	Pull-up *	Low	LS_OUT_7
	PD10	GPIO_Output	Output Push Pull	Pull-up *	Low	LS_OUT_8
	PD11	GPIO_Output	Output Push Pull	Pull-down *	Low	LIN_SLEEP
	PG5	GPIO_Output	Output Push Pull	Pull-up *	Low	LED_ERROR
	PG6	GPIO_Output	Output Push Pull	Pull-up *	Low	LED_RUN
	PG7	GPIO_Output	Output Push Pull	Pull-up *	Low	RESET
	PA15 (JTDI)	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IMU_INT2
	PD0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IMU_INT1
	PD1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SDIO0_CD
	PD3	GPIO_Output	Output Push Pull	Pull-down *	Low	HS_OUT_7
	PD4	GPIO_Output	Output Push Pull	Pull-down *	Low	HS_OUT_8
	PD7	GPIO_Output	Output Push Pull	Pull-up *	Low	LS_OUT_5
	PG9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ID_5
	PG10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ID_4
	PG11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ID_3
	PG12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ID_2
	PG13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ID_1
	PG14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ID_0
	PI5	GPIO_Output	Output Push Pull	Pull-down *	Low	SD_PWR_ON

8.2. DMA configuration

nothing configured in DMA service

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

8.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	15	0	
System tick timer	true	15	0	
FDCAN1 interrupt 0	true	5	0	
FDCAN2 interrupt 0	true	5	0	
USART1 global interrupt	true	8	0	
USART3 global interrupt	true	5	0	
TIM8 update interrupt and TIM13 global interrupt	true	6	0	
SDMMC1 global interrupt	true	5	0	
TIM7 global interrupt	true	15	0	
USB On The Go FS global interrupt	true	5	0	
PVD and AVD interrupts through EXTI line 16	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
ADC1 and ADC2 global interrupts	unused			
FDCAN1 interrupt 1	unused			
FDCAN2 interrupt 1	unused			
TIM2 global interrupt	unused			
TIM3 global interrupt	unused			
TIM4 global interrupt	unused			
TIM8 break interrupt and TIM12 global interrupt	unused			
FDCAN calibration unit interrupt	unused			
FPU global interrupt	unused			
USB On The Go FS End Point 1 Out global interrupt	unused			
USB On The Go FS End Point 1 In global interrupt	unused			
TIM15 global interrupt	unused			
HSEM1 global interrupt	unused			
ADC3 global interrupt	unused			
Interrupt for all 6 wake-up pins	unused			

8.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
FDCAN1 interrupt 0	false	true	true
FDCAN2 interrupt 0	false	true	true
USART1 global interrupt	false	true	true
USART3 global interrupt	false	true	true
TIM8 update interrupt and TIM13 global interrupt	false	true	true
SDMMC1 global interrupt	false	true	true
TIM7 global interrupt	false	true	true
USB On The Go FS global interrupt	false	true	true

^{*} User modified value

9. System Views

9.1. Category view

9.1.1. Current

ps_	_vcu	Pro	ject
Configura	ation	Re	port

9.1.2. Without filters

9.2. Power Domain view

10. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32h7_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip

System View https://www.st.com/resource/en/svd/stm32h7-svd.zip

Description

Presentations https://www.st.com/resource/en/product_presentation/microcontrollers_st

m32h7_series_product_overview.pdf

Presentations https://www.st.com/resource/en/product_presentation/stm32-

stm8_embedded_software_solutions.pdf

Presentations https://www.st.com/resource/en/product_presentation/stm32_eval-

tools_portfolio.pdf

Presentations https://www.st.com/resource/en/product_presentation/stm32_stm8_functi

onal-safety-packages.pdf

Presentations https://www.st.com/resource/en/product_presentation/stm32-

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Flyers https://www.st.com/resource/en/flyer/flstm32trust.pdf

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Security Bulletin https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-

protection-statement-for-stmicroelectronics-certified-products-

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Application Notes https://www.st.com/resource/en/application_note/an1709-emc-design-

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Application Notes https://www.st.com/resource/en/application_note/an2606-stm32-

- microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
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- Application Notes https://www.st.com/resource/en/application_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4539-hrtim-cookbook-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4566-extending-the-dac-performance-of-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4750-handling-of-soft-errors-in-stm32-applications-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4776-generalpurpose-timer-cookbook-for-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4803-highspeed-si-simulations-using-ibis-and-boardlevel-simulations-using-hyperlynx-si-on-stm32-mcus-and-mpus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4839-level-1-cache-on-stm32f7-series-and-stm32h7-series-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4891-stm32h72x-stm32h73x-and-singlecore-stm32h74x75x-system-architecture-and-performance-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4936-migration-of-microcontroller-applications-from-stm32f7-series-to-stm32h743753-line-

- stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4989-stm32-microcontroller-debug-toolbox-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4990-getting-started-with-sigmadelta-digital-interface-on-applicable-stm32-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an5027-interfacing-pdm-digital-microphones-using-stm32-mcus-and-mpus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an5033-stm32cube-mcu-package-examples-for-stm32h7-series-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an5073-receiving-spdif-audio-stream-with-the-stm32f4f7h7-series-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an5312-migration-from-revy-to-revy-for-stm32h743753-and-stm32h750-value-line-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an5354-getting-started-with-the-stm32h7-series-mcu-16bit-adc-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4760-quadspiinterface-on-stm32-microcontrollers-and-microprocessors-stmicroelectronics.pdf
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- Application Notes https://www.st.com/resource/en/application_note/an5612-esd-protection-of-stm32-mcus-and-mpus-stmicroelectronics.pdf
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- Application Notes https://www.st.com/resource/en/application_note/an4991-how-to-wake-up-an-stm32-microcontroller-from-lowpower-mode-with-the-usart-or-the-lpuart-stmicroelectronics.pdf
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