Computer Vision HW Acceleration for Driver Assistance

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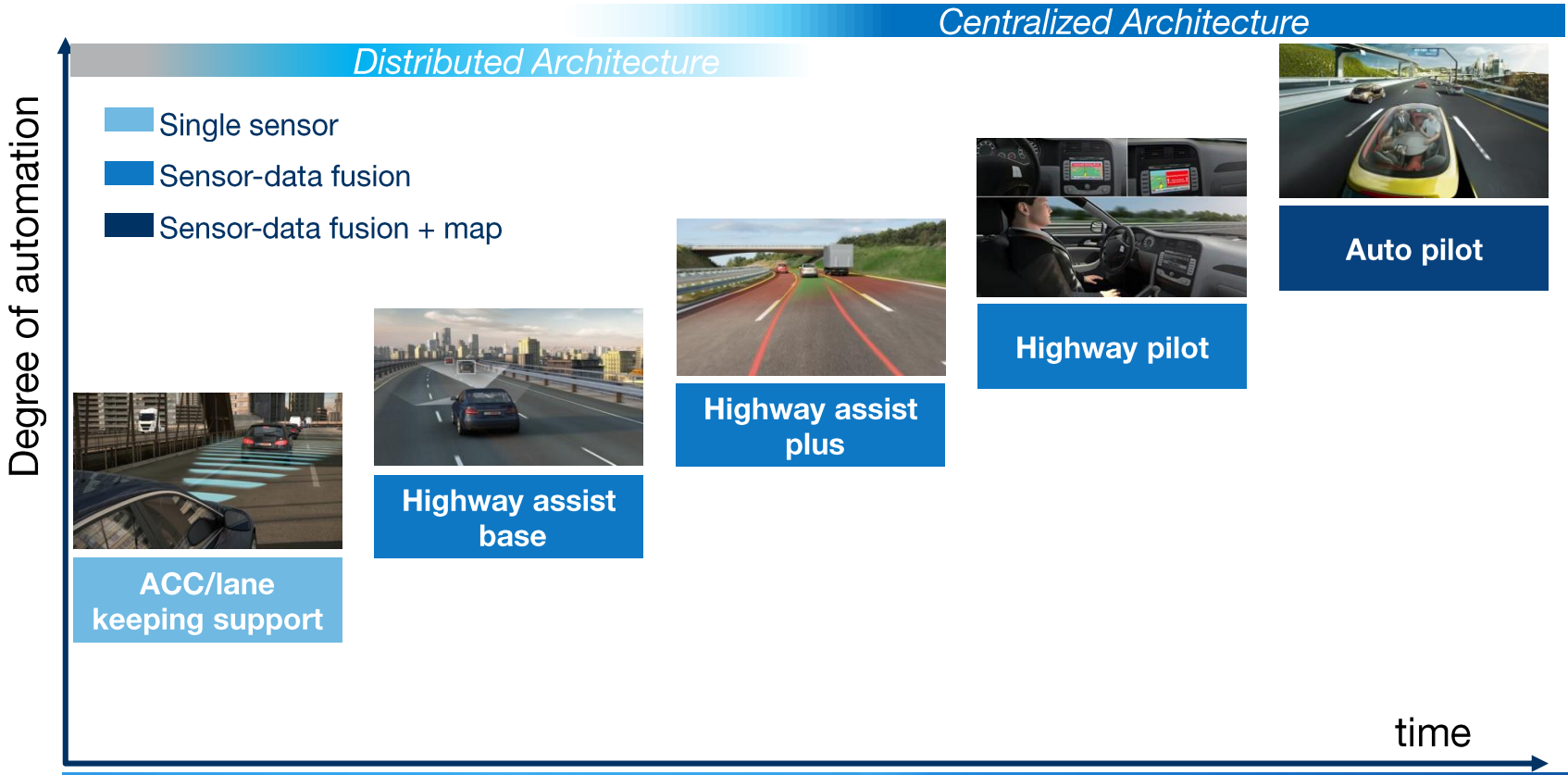
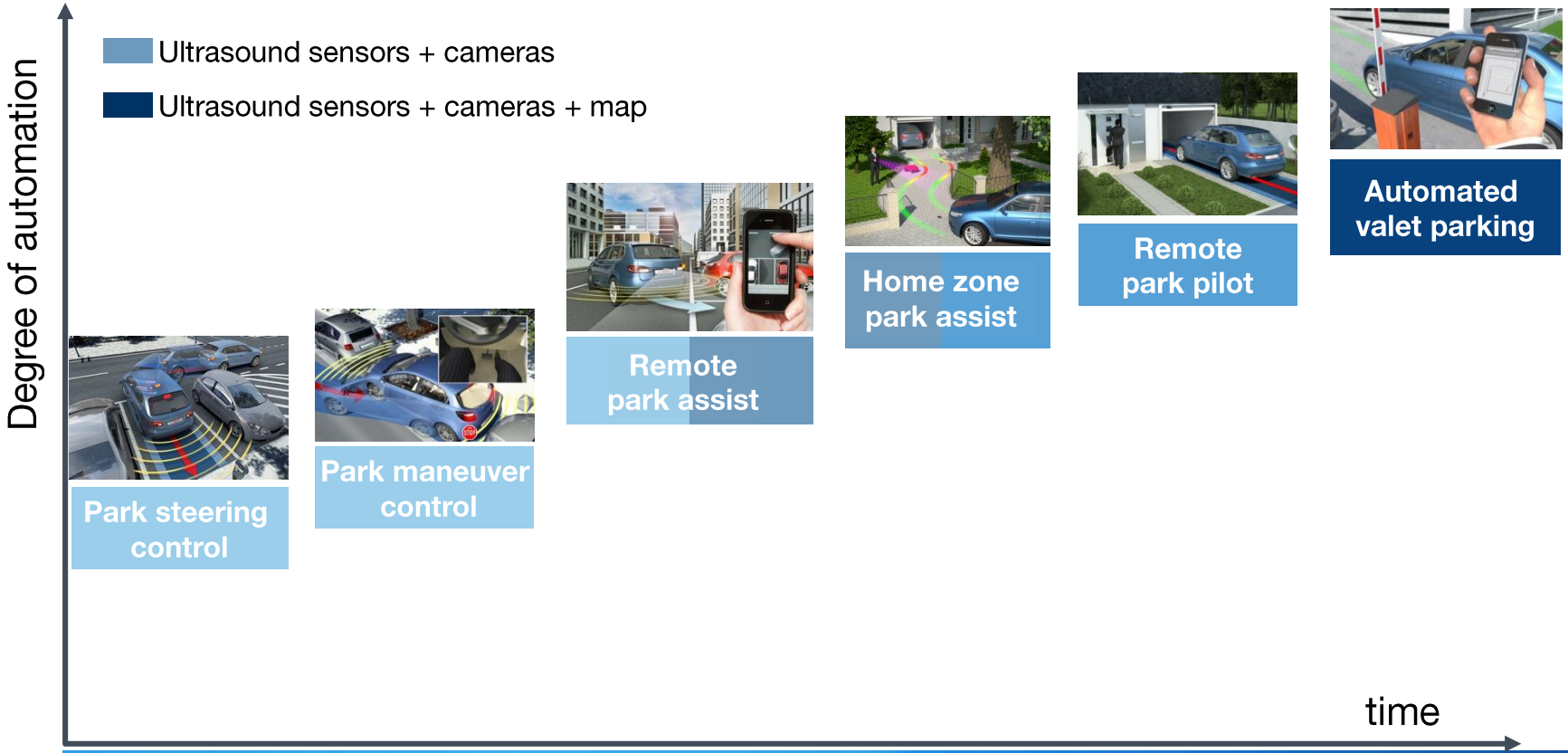
Driver Assistance Systems - Driving



Driver Assistance Systems - Parking



Driver Assistance Functions

Emergency braking

Lane keeping/changing

Evasion

Pedestrian protection

Turning and crossing

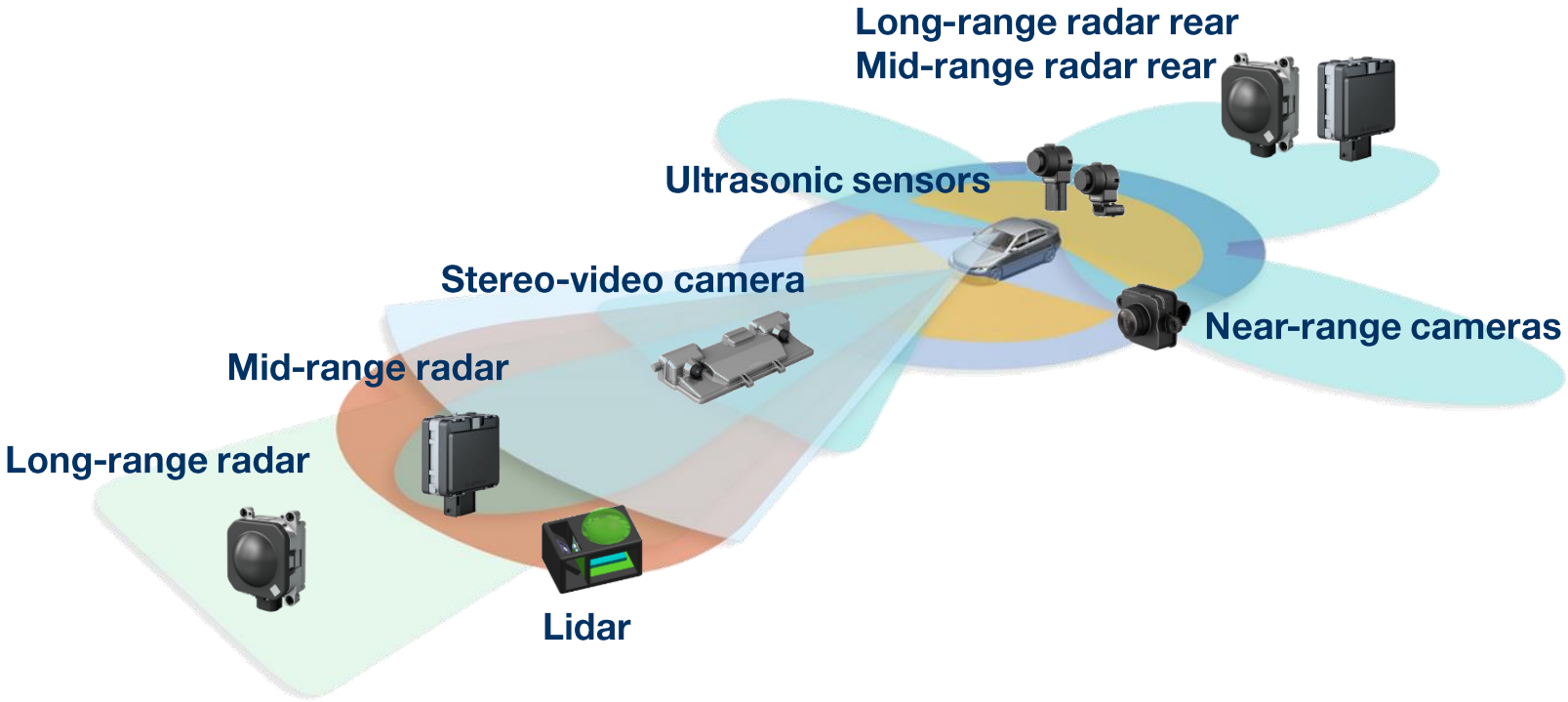
Travelling (distance/speed)

Driver monitoring

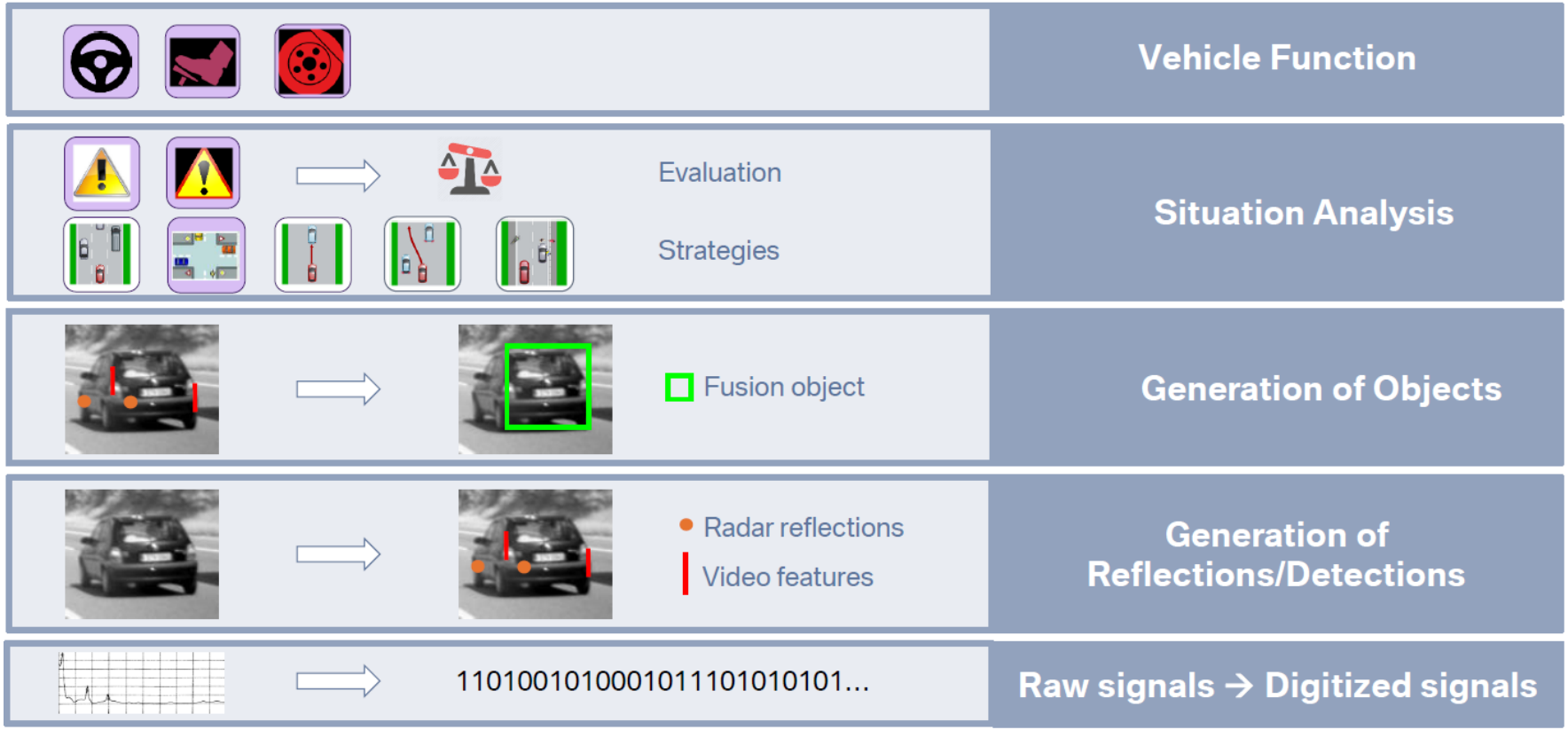
Light and sight

Parking and maneuvering

Driver Assistance Sensors



Autonomous Driving – Processing Chain



Autonomous Driving – Computer Vision

SENSING

Sensor Development

Signal Processing

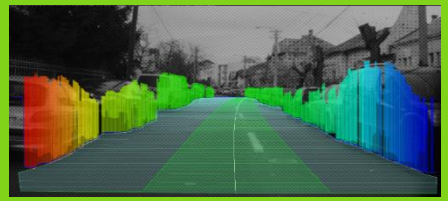
PERCEPTION

Disparity / Optical Flow
Structure from Motion

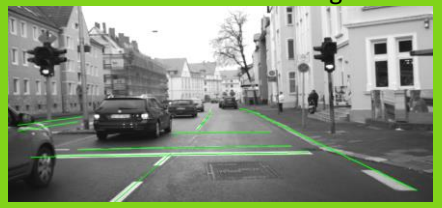
Deep Learning
Semantic Segmentation
Sensor Data Fusion

AI

3D Measurements



Classic Lane Markings



Complex Lane Markings

Missing Lane Markings

Classical control models

INTERACT,CONTROL

PLANNING

Deep Learning for Behavior Prediction

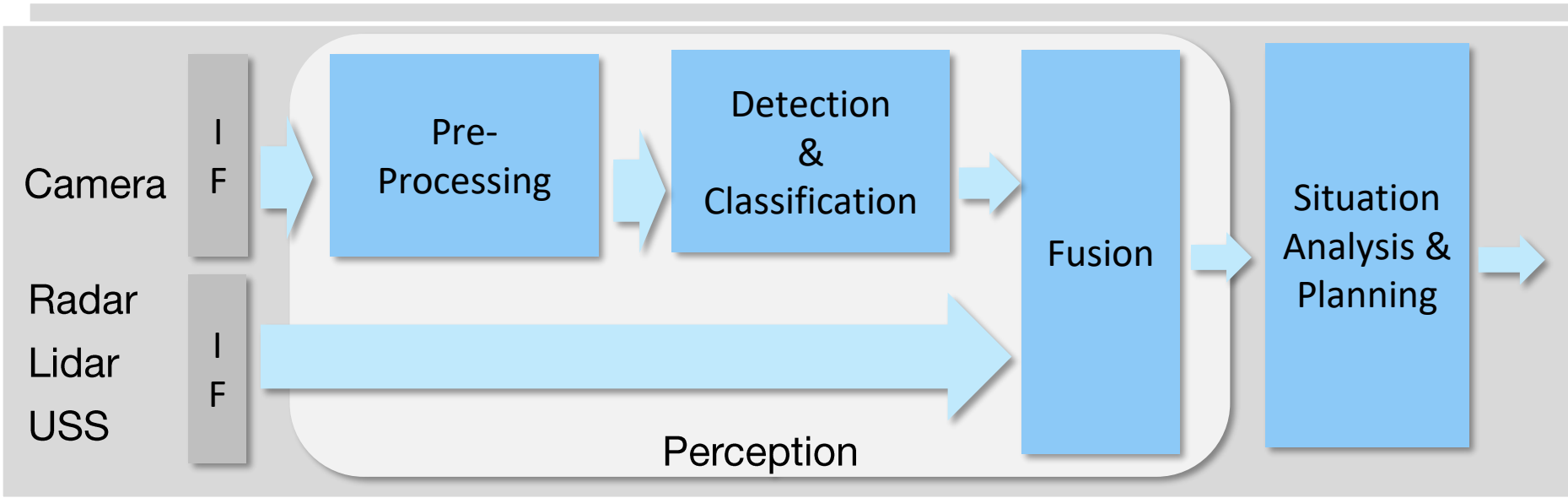
Reinforcement Learning for Planning

AI

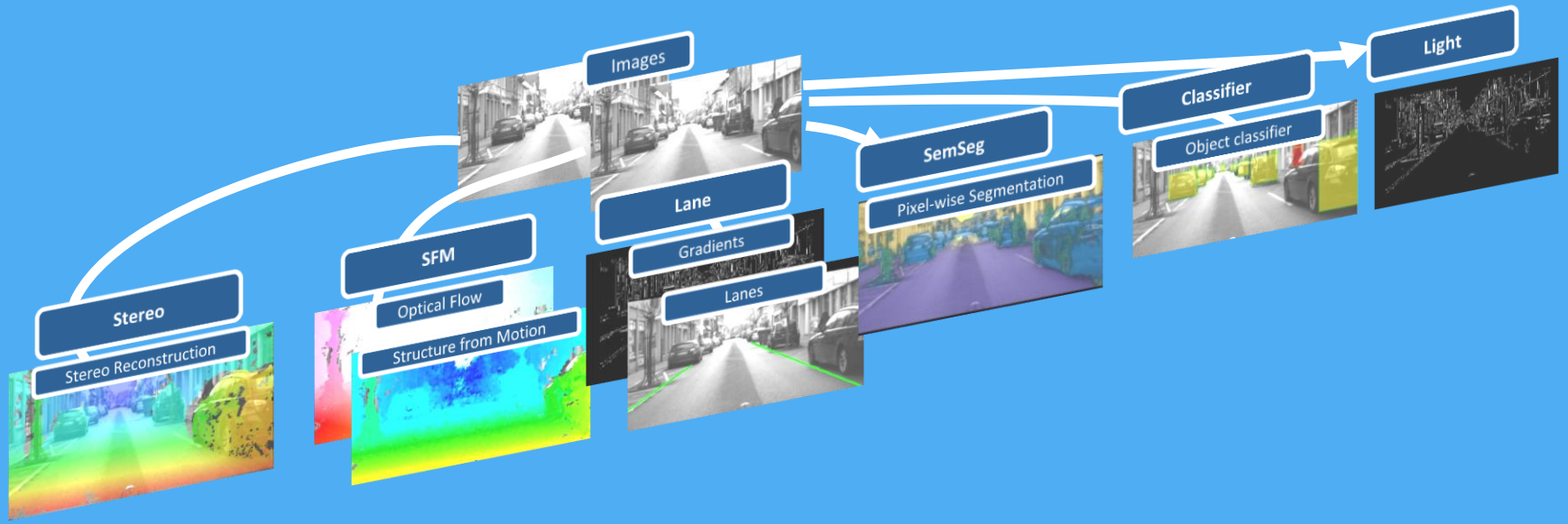
Behaviour Prediction

Behaviour Planning

Autonomous Driving – Perception & Planning

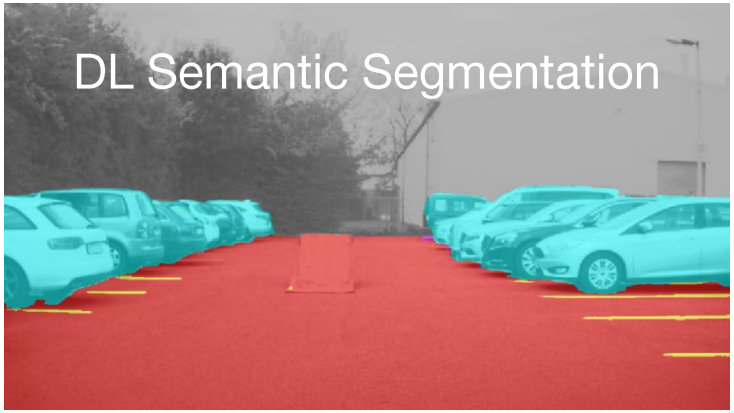


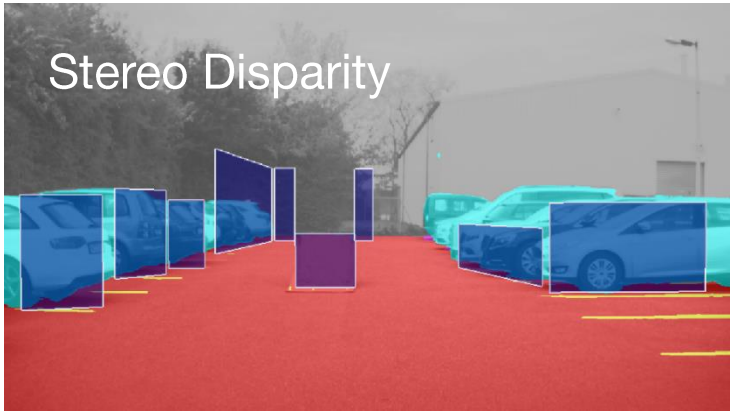
Multi-Path Approach – Computer Vision



Multi-Path Approach Benefit

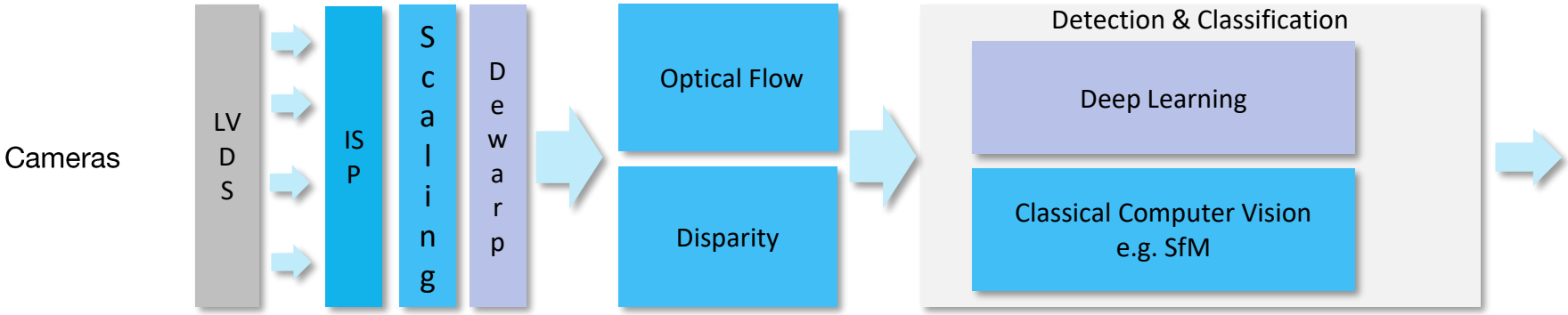
- Gray obstacle with road texture





- Multipath obstacle detection will assure safe path and delimiter estimation
- Increasing detection probability due to additional redundancy

Autonomous Driving – CV Multi-Path Processing



Programmable

- multiple different algorithms, defined at runtime
- standard HW building blocks

- control and execution overhead
- parallelism & throughput compromise

➢ **High flexibility**

x 10
Power Efficiency
vs. typical DSP

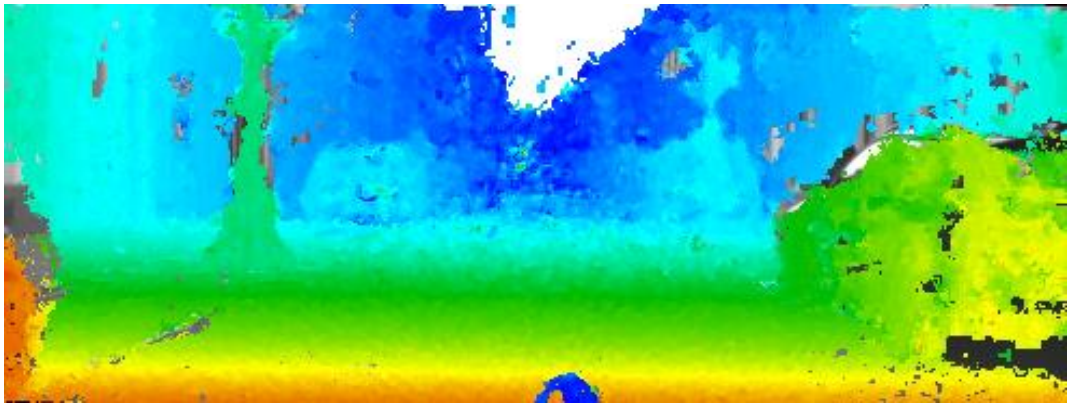
Configurable

- fixed algorithm(s), defined at design time
- higher upfront effort for optimization & validation

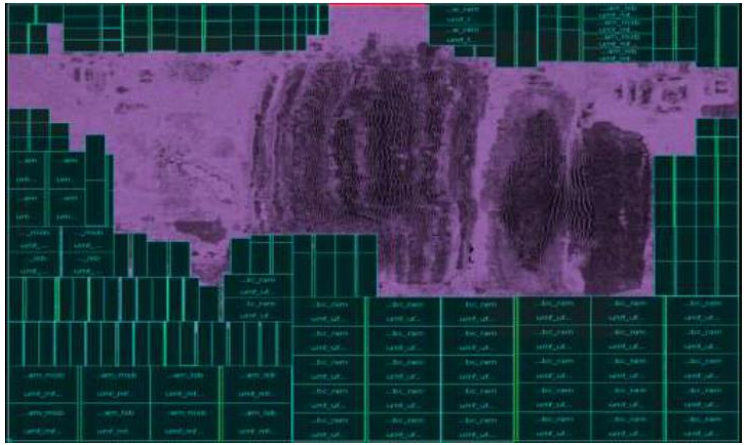
- minimum overhead (e.g. ctrl registers … typ. 100-1000)
- maximum optimization possible (no HW compromises)

➢ **High power- & cost efficiency**

Optical Flow Acceleration - Example



- 16 nm FF
- 533 MHz
- < 0,5 W at full HD 60fps



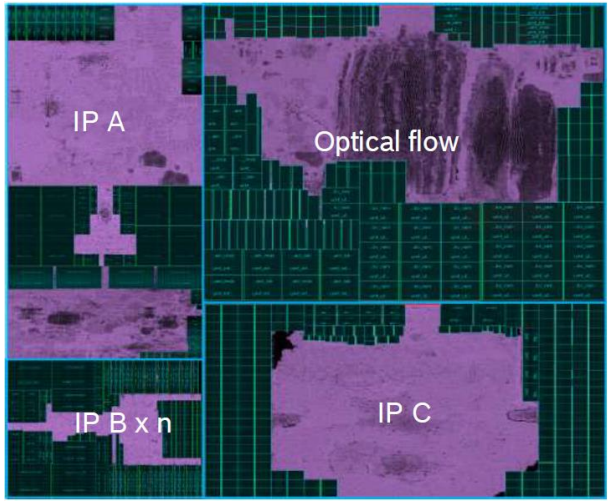
ADAS CV Pre-Processing Acceleration - Example

- OF, Disparity & Classifier HW IP modules
- HD 60/30 fps, 16 nm FF

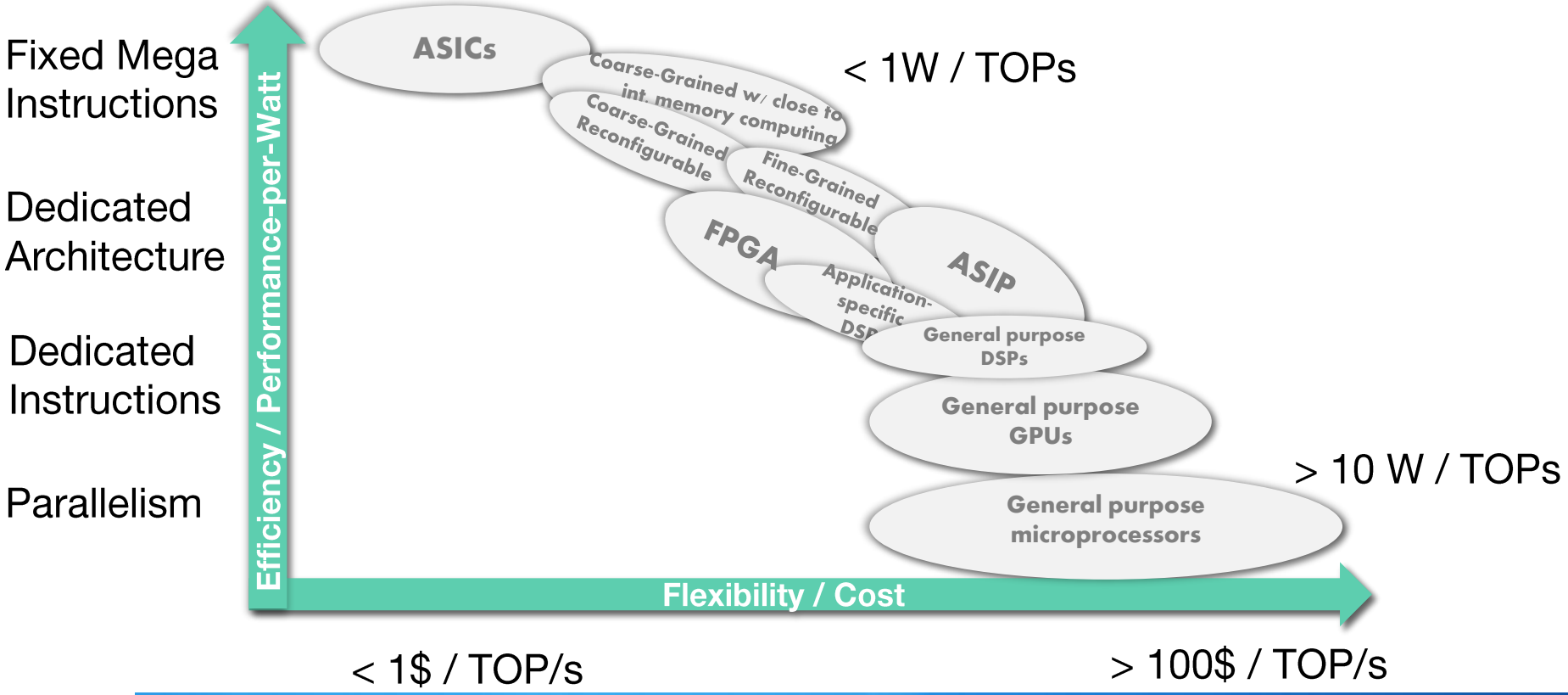
➢ Enabling high performant & power efficient ADAS SoCs

➢ Enabling smart cameras (incl. DL) <5 W

➢ Enabling ADAS L3 ECU without water-cooling

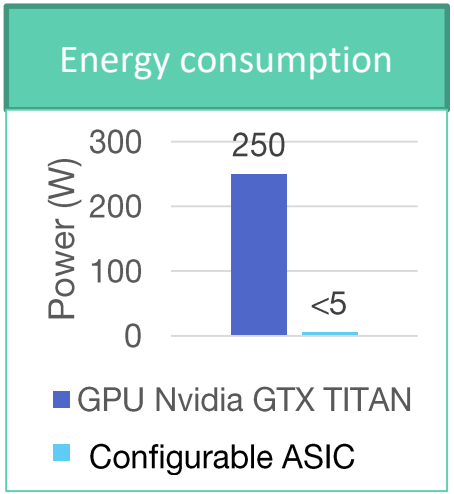


DL Acceleration: Efficiency vs. Flexibility

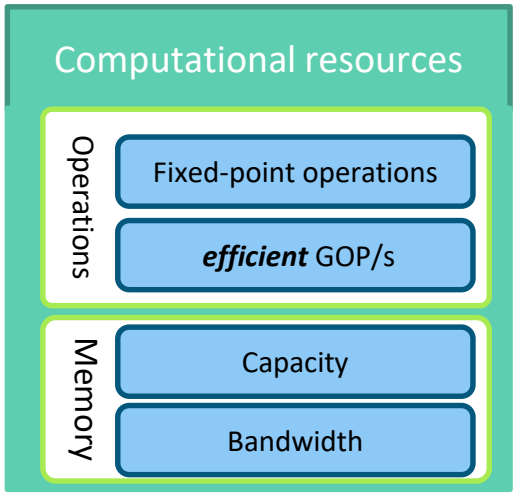


Deep Learning goes embedded

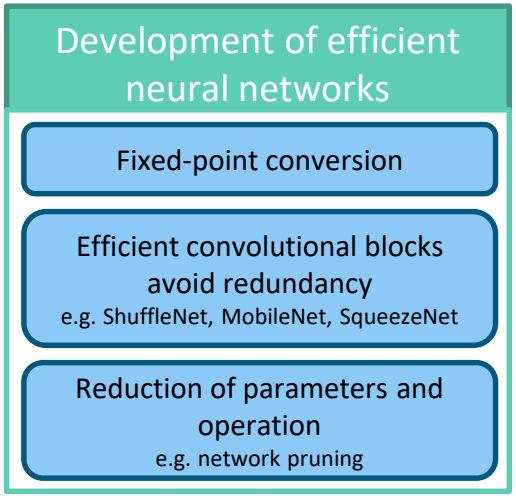
- Low energy consumption is key for ADAS systems
- Standard GPUs need to be replaced with dedicated embedded hardware
- Configurable ASICs deliver best in class power efficiency



2 Orders of Magnitude Difference



Influencing Factors



Development approaches

Embedded Deep Learning - Semantic Segmentation

Standard VGG16

BoschNet

- 50x smaller
- better segmentation

DL vs Classic CV Depth Analysis

Analysis Method	KPI	Classic CV (HW accel.)	Deep Learning
Disparity	Quality	Very good	Good
	Calculation Requirement	1	~70
Optical Flow	Quality	Very good	Fair (2x outlier ratio)
	Calculation Requirement	1	~70

- Quality of DL depth analysis not yet acceptable for automotive
- Calculation requirements still substantial higher than classical CV

Summary

- Superior performance by combination of classical CV and deep learning
- HD video proceeding is pushing the calculation requirements to the limits
- Low power consumption is key enabler

➢ HW acceleration IP is a must for affordable mass market ADAS

Resources

- Bosch Mobility Solutions:

http://www.bosch-mobility-solutions.com/en/

- OF/DISP Benchmarks

http://hci-benchmark.org/

https://hci.iwr.uni-heidelberg.de/benchmarks

http://www.cvlibs.net/datasets/kitti/index.php

- AI / DL Acceleration
- https://www.nanalyze.com/2017/05/12-ai-hardware-startups-new-ai-chips/

THANK YOU