
STM32
CubeMX

1. Description

1.1. Project

Project Name	14 FSMC_LCD
Board Name	custom
Generated with:	STM32CubeMX 6.0.1
Date	09/12/2021

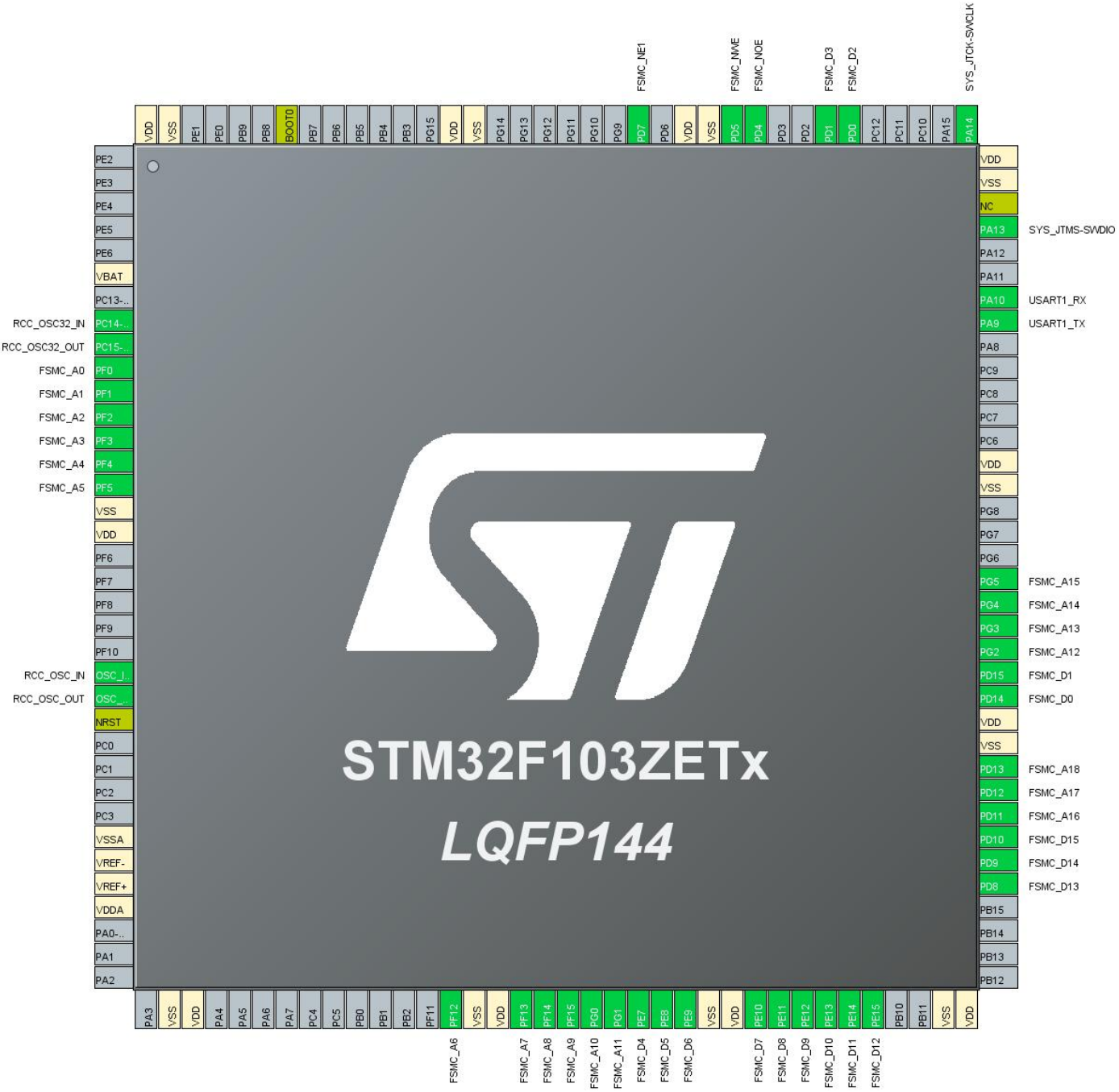
1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103ZETx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M3

2. Pinout Configuration



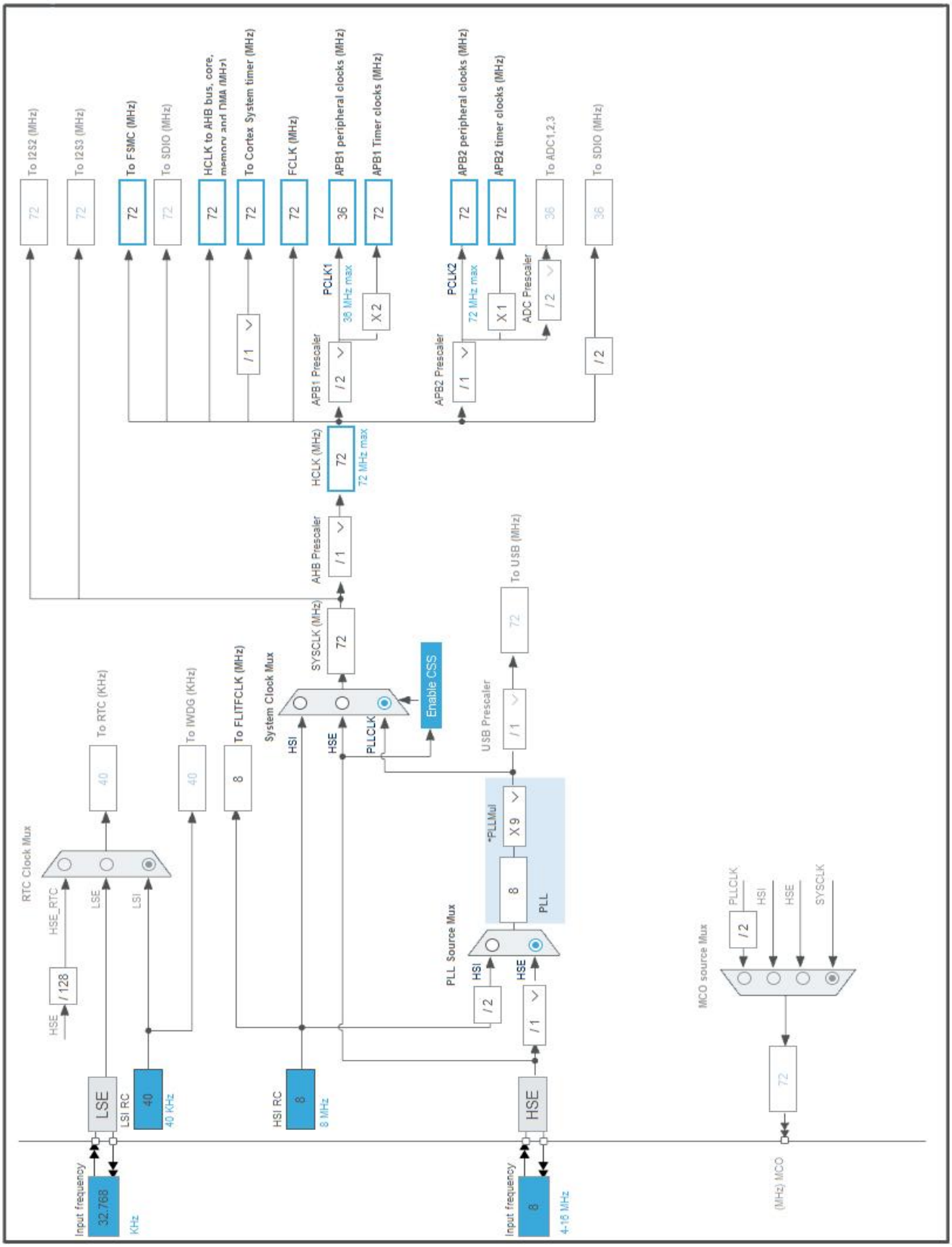
3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
10	PF0	I/O	FSMC_A0	
11	PF1	I/O	FSMC_A1	
12	PF2	I/O	FSMC_A2	
13	PF3	I/O	FSMC_A3	
14	PF4	I/O	FSMC_A4	
15	PF5	I/O	FSMC_A5	
16	VSS	Power		
17	VDD	Power		
23	OSC_IN	I/O	RCC_OSC_IN	
24	OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
30	VSSA	Power		
31	VREF-	Power		
32	VREF+	Power		
33	VDDA	Power		
38	VSS	Power		
39	VDD	Power		
50	PF12	I/O	FSMC_A6	
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	FSMC_A7	
54	PF14	I/O	FSMC_A8	
55	PF15	I/O	FSMC_A9	
56	PG0	I/O	FSMC_A10	
57	PG1	I/O	FSMC_A11	
58	PE7	I/O	FSMC_D4	
59	PE8	I/O	FSMC_D5	
60	PE9	I/O	FSMC_D6	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	FSMC_D7	
64	PE11	I/O	FSMC_D8	
65	PE12	I/O	FSMC_D9	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
66	PE13	I/O	FSMC_D10	
67	PE14	I/O	FSMC_D11	
68	PE15	I/O	FSMC_D12	
71	VSS	Power		
72	VDD	Power		
77	PD8	I/O	FSMC_D13	
78	PD9	I/O	FSMC_D14	
79	PD10	I/O	FSMC_D15	
80	PD11	I/O	FSMC_A16	
81	PD12	I/O	FSMC_A17	
82	PD13	I/O	FSMC_A18	
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	FSMC_D0	
86	PD15	I/O	FSMC_D1	
87	PG2	I/O	FSMC_A12	
88	PG3	I/O	FSMC_A13	
89	PG4	I/O	FSMC_A14	
90	PG5	I/O	FSMC_A15	
94	VSS	Power		
95	VDD	Power		
101	PA9	I/O	USART1_TX	
102	PA10	I/O	USART1_RX	
105	PA13	I/O	SYS_JTMS-SWDIO	
106	NC	NC		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
114	PD0	I/O	FSMC_D2	
115	PD1	I/O	FSMC_D3	
118	PD4	I/O	FSMC_NOE	
119	PD5	I/O	FSMC_NWE	
120	VSS	Power		
121	VDD	Power		
123	PD7	I/O	FSMC_NE1	
130	VSS	Power		
131	VDD	Power		
138	BOOT0	Boot		
143	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
144	VDD	Power		

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	14 FSMC_LCD
Project Folder	D:\shiyanshi\practice\STM32\CubeMx\14 FSMC_LCD
Toolchain / IDE	MDK-ARM V5.27
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.4
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	IP Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_FSMC_Init	FSMC
4	MX_USART1_UART_Init	USART1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103ZETx
Datasheet	DS5792_Rev12

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

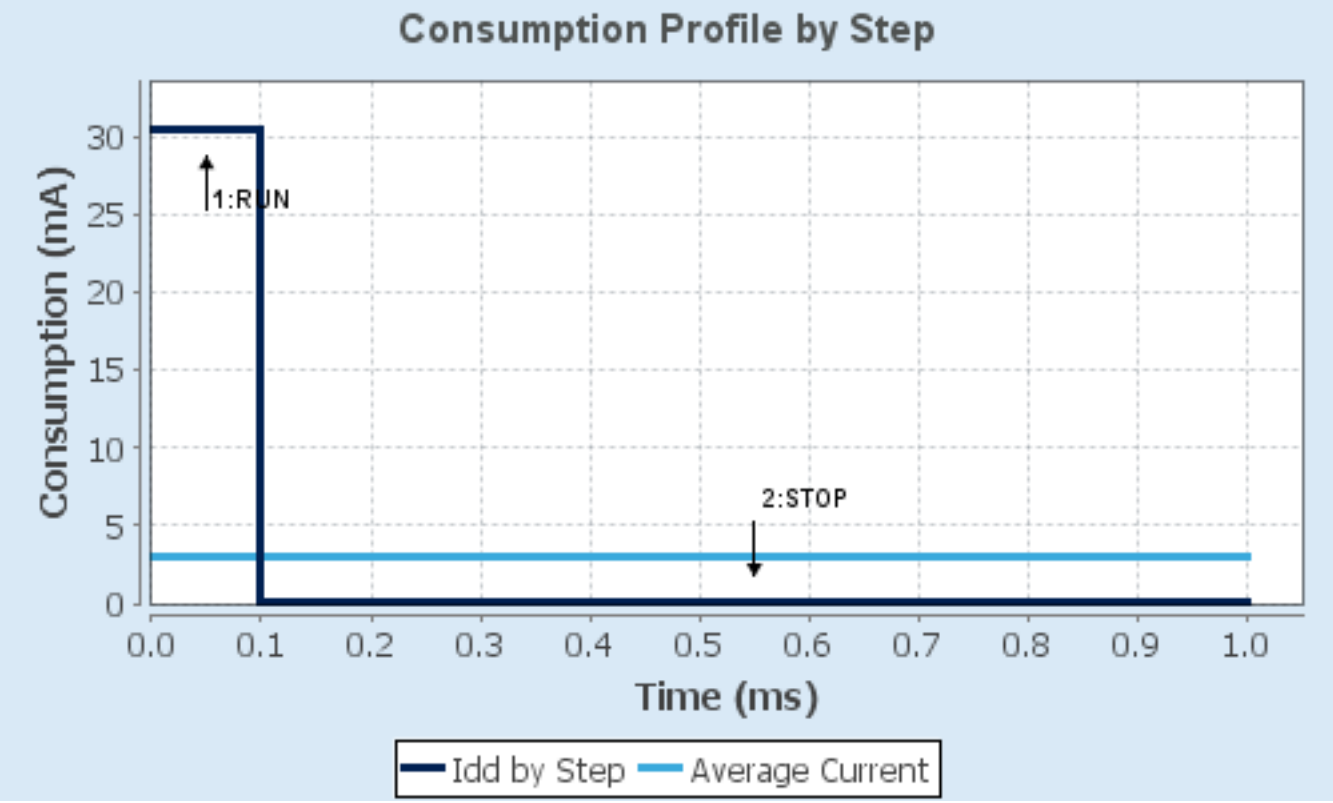
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	30.5 mA	25 µA
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	101.98	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	3.07 mA
Battery Life	1 month, 15 days, 15 hours	Average DMIPS	61.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
30
25
20
15
10
5
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. FSMC

NOR Flash/PSRAM/SRAM/ROM/LCD 1

Chip Select: NE1

Memory type: SRAM

Address: 19 bits

Data: 16 bits

7.1.1. NOR/PSRAM 1:

NOR/PSRAM control:	
Memory type	SRAM
Bank	Bank 1 NOR/PSRAM 1
Write operation	**Enabled ***
Extended mode	**Enabled ***
NOR/PSRAM timing:	
Address setup time in HCLK clock cycles	15
Data setup time in HCLK clock cycles	**46 ***
Bus turn around time in HCLK clock cycles	**1 ***
Access mode	A
NOR/PSRAM timing for write accesses:	
Extended address setup time	15
Extended data setup time	**15 ***
Extended bus turn around time	**1 ***
Extended access mode	A

7.2. GPIO

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:	
VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.5. USART1

Mode: Asynchronous

7.5.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
FSMC	PF0	FSMC_A0	Alternate Function Push Pull	n/a	High	
	PF1	FSMC_A1	Alternate Function Push Pull	n/a	High	
	PF2	FSMC_A2	Alternate Function Push Pull	n/a	High	
	PF3	FSMC_A3	Alternate Function Push Pull	n/a	High	
	PF4	FSMC_A4	Alternate Function Push Pull	n/a	High	
	PF5	FSMC_A5	Alternate Function Push Pull	n/a	High	
	PF12	FSMC_A6	Alternate Function Push Pull	n/a	High	
	PF13	FSMC_A7	Alternate Function Push Pull	n/a	High	
	PF14	FSMC_A8	Alternate Function Push Pull	n/a	High	
	PF15	FSMC_A9	Alternate Function Push Pull	n/a	High	
	PG0	FSMC_A10	Alternate Function Push Pull	n/a	High	
	PG1	FSMC_A11	Alternate Function Push Pull	n/a	High	
	PE7	FSMC_D4	Alternate Function Push Pull	n/a	High	
	PE8	FSMC_D5	Alternate Function Push Pull	n/a	High	
	PE9	FSMC_D6	Alternate Function Push Pull	n/a	High	
	PE10	FSMC_D7	Alternate Function Push Pull	n/a	High	
	PE11	FSMC_D8	Alternate Function Push Pull	n/a	High	
	PE12	FSMC_D9	Alternate Function Push Pull	n/a	High	
	PE13	FSMC_D10	Alternate Function Push Pull	n/a	High	
	PE14	FSMC_D11	Alternate Function Push Pull	n/a	High	
	PE15	FSMC_D12	Alternate Function Push Pull	n/a	High	
	PD8	FSMC_D13	Alternate Function Push Pull	n/a	High	
	PD9	FSMC_D14	Alternate Function Push Pull	n/a	High	
	PD10	FSMC_D15	Alternate Function Push Pull	n/a	High	
	PD11	FSMC_A16	Alternate Function Push Pull	n/a	High	
	PD12	FSMC_A17	Alternate Function Push Pull	n/a	High	
	PD13	FSMC_A18	Alternate Function Push Pull	n/a	High	
	PD14	FSMC_D0	Alternate Function Push Pull	n/a	High	
	PD15	FSMC_D1	Alternate Function Push Pull	n/a	High	
	PG2	FSMC_A12	Alternate Function Push Pull	n/a	High	
	PG3	FSMC_A13	Alternate Function Push Pull	n/a	High	
	PG4	FSMC_A14	Alternate Function Push Pull	n/a	High	
	PG5	FSMC_A15	Alternate Function Push Pull	n/a	High	
	PD0	FSMC_D2	Alternate Function Push Pull	n/a	High	
	PD1	FSMC_D3	Alternate Function Push Pull	n/a	High	
	PD4	FSMC_NOE	Alternate Function Push Pull	n/a	High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD5	FSMC_NWE	Alternate Function Push Pull	n/a	High	
	PD7	FSMC_NE1	Alternate Function Push Pull	n/a	High	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	n/a	**High ***	
	PA10	USART1_RX	Input mode	No pull-up and no pull-down	**n/a**	

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
USART1 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	true	true	false
Hard fault interrupt	true	true	false
Memory management fault	true	true	false
Prefetch fault, memory access fault	true	true	false
Undefined instruction or illegal state	true	true	false
System service call via SWI instruction	true	true	false
Debug monitor	true	true	false
Pendable request for system service	true	true	false
System tick timer	true	true	true
USART1 global interrupt	true	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current