内核笔记

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内存管理

1.1 虚拟地址转换

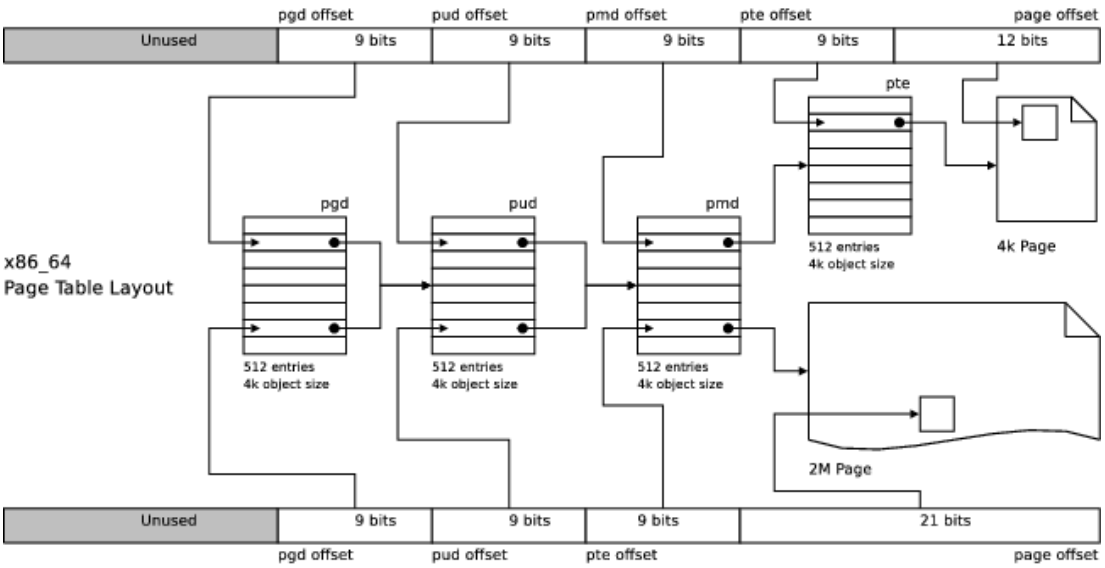

Figure 1.1: 虚拟地址转换 [1]

1.2 页表结构

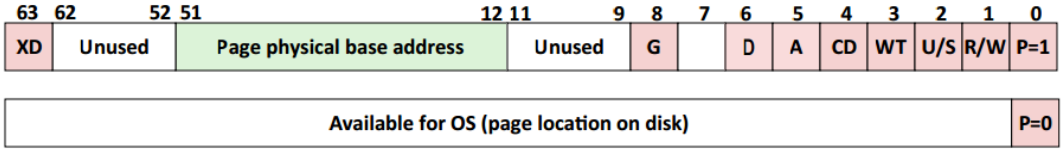

Figure 1.2: Core i7 Level 4 Page Table Entries

- **P: Child page is present in memory (1)or not(0)**
- **R/W: Read-only or read-write access permission for child page**
- **U/S: User or supervisor mode access**
- **WT: Write-through or write-back cache policy for this page**
- **CD: Cache disabled (1) or enabled (0)**
- **A: Reference bit (set by MMU on reads and writes, cleared by sohware)**
- **D: Dirty bit (set by MMU on writes, cleared by sohware)**
- **G: Global page (don’ t evict from TLB on task switch)**
- **Page physical base address: 40 most significant bits of physical page address (forces pages to be 4KB aligned)**

参考文献

[1] http://linux-mm.org/PageTableStructure. 1