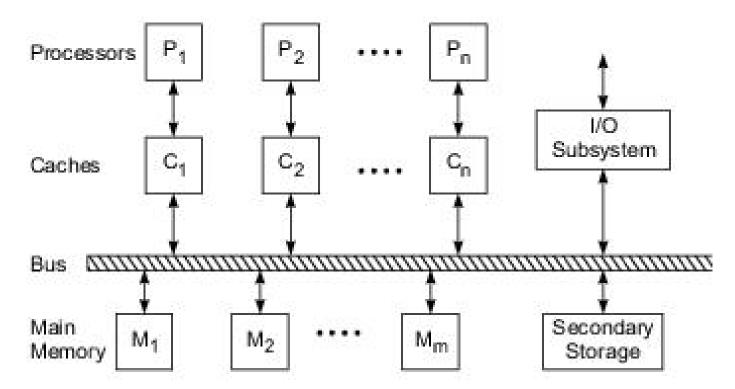
Dynamic Connection Networks

- Include bus systems, multistage interconnection networks (MIN) and crossbar switch networks
- > attributed to the cost of the wires, switches, arbiters, and connectors required
- ➤ Performance is indicated by the network bandwidth, data transfer rate, network latency, and communication patterns supported
- Networks are
 - Digital buses
 - Switch Modules
 - ➤ Multistage Interconnection Network
 - Omega Network
 - Baseline Network
 - Crossbar Network

Digital Buses:

- Essentially a collection of wires and connectors for data transactions among processors, memory modules, and peripheral devices attached to the bus
- > Bus is used for only one transaction at a time between source and destination
- In case of multiple requests, the bus arbitration logic must be able to allocate or decallocate the bus, servicing the requests one at a time
- > Also called contention bus or a time-sharing bus among multiple functional modules
- > Bus system has a lower cost and provides a limited bandwidth



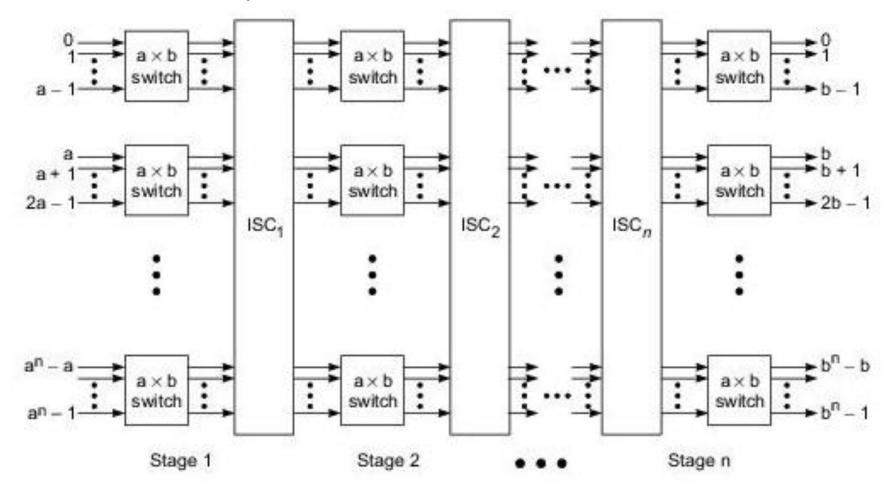
Switch Modules:

- \triangleright a \times b switch module has a inputs and b outputs
- \triangleright A binary switch corresponds to a 2 × 2 switch module in which a = b = 2
- Theoretically, a and b do not have to be equal
- In practice, a and b are often chosen as integer powers of 2; i.e., $a = b = 2^k$ for some $k \ge 1$
- > Each input can be connected to one or more of the outputs
- Conflicts must be avoided at the output terminals
- ➤ One-to-one and one-to-many mappings are allowed; but many-to—one mappings are not allowed due to conflicts at the output terminal
- > When only one-to-one mappings (permutations) are allowed, we call the module an n × n crossbar switch
- > a 2 × 2 crossbar switch can connect two possible patterns: straight or crossover
- In general, an n × n crossbar can achieve n! permutations
- commonly used switch module sizes:

Module Size	Legitimate States	Permutation Connections 2 24	
2×2	4		
4×4	256		
8×8	16,777,216 40,320		
$n \times n$	n ⁿ	n!	

Multistage Interconnection Networks (MINs):

➤ Used in both MIMD and SIMD computers



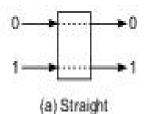
A generalized structure of a multistage interconnection network (MIN) built with a \times b switch modules and interstage connection patterns ISC₁, ISC₂, ..., ISC_n

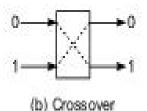
Multistage Interconnection Networks (MINs):

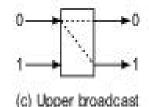
- \triangleright Number of $a \times b$ switches are used in each stage
- Fixed inter-stage connections are used between the switches in adjacent stages
- > Switches can be dynamically set to establish the desired connections between the inputs and outputs
- > Different classes of MINs differ in the switch modules used as kind of interstage connection (ISC) patterns used
- \triangleright Simplest switch module would be the 2 × 2 switches
- > ISC patterns often used include perfect shuffle, butterfly, multiway shuffle, crossbar, cube connection, etc.

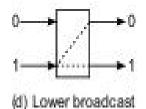
Omega Network:

 \triangleright Four possible connections of 2×2 switches used in constructing the Omega network



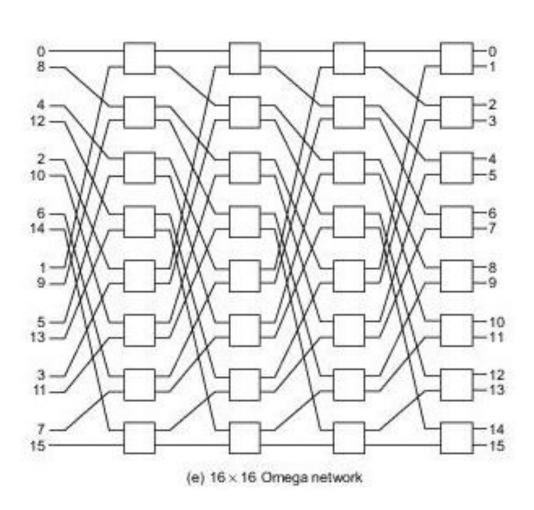






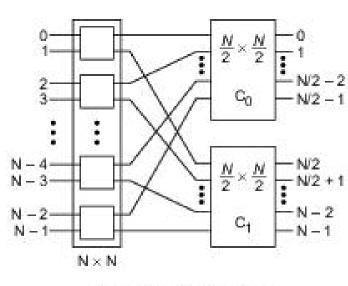


- ➤ 16 inputs on the left and 16 outputs on the right
- ➤ ISC pattern is the *perfect shuffle* over 16 objects
- \triangleright an *n*-input Omega network requires $log_n 2$ stages of 2 × 2 switches
- \triangleright Each stage requires n/2 switch modules
- \triangleright In total, the network uses $nlog_n 2$ switches
- > Each switch module is individually controlled
- ➤ Various combinations of the switch states implement different permutations, broadcast, or other connections front the inputs to the outputs

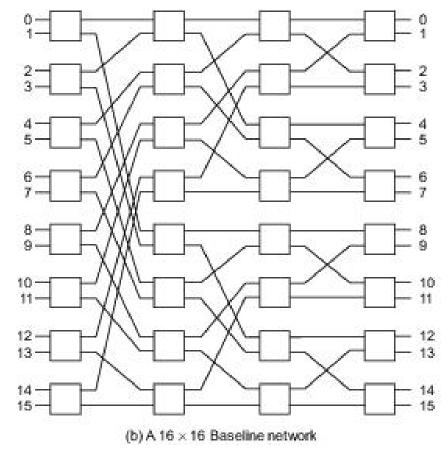


Baseline Network:

- > A Baseline network can be generated recursively"
 - \triangleright The first stage contains one $N \times N$ block, and
 - ightharpoonup Second stage contains two $\left(\frac{N}{2}\right) \times \left(\frac{N}{2}\right)$ subblocks, labeled C_0 and C_1
 - \triangleright Construction process can be recursively applied to the subblocks until N/2 subblocks of size 2×2 are reached
- \triangleright The building blocks of subblocks are 2 \times 2 switches; each with two states: straight and crossover

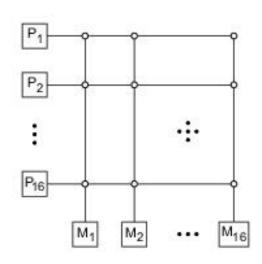


(a) Recursive construction

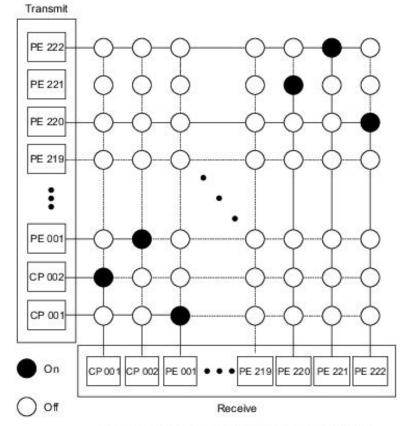


Crossbar Network:

- ➤ Highest bandwidth and interconnection and routing capability
- visualized as a single-stage switch network
- Like a telephone switchboard, the cross-point switches dynamic connections between source, destination pairs
- Provides a dedicated connection path between a pair
- > Switch can be set ON or OFF dynamically upon program demand



 (a) Interprocessor-memory crossbar network built in the C.mmp multiprocessor at Carnegie-Mellon University (1972)



 (b) The interprocessor crossbar network built in the Fujitsu VPP 500 vector parallel processor (1992)

Crossbar Network:

- > To build a shared-memory multiprocessor, one can use a crossbar network between the processors and memory modules
- > Essentially a memory-access network
- > Each memory module can satisfy only one processor request at a time
- > When multiple requests arrive at the some memory module simultaneously, the crossbar must resolve the conflicts
- > Behaviour of crossbar is similar to that of a bus
- ➤ Processor can generate a sequence of addresses to access multiple memory modules simultaneously, only one crosspoint switch can be set on in each column
- > Several crosspoint switches can be set on simultaneously in order to support parallel (or interleaved) memory accesses
- \triangleright Large crossbar [224 \times 224) was actually built in a vector parallel processor (VPP500) by Fujitsu Inc. (1992)
- > PEs are processors with attached memory
- > CPs stand for control processors which are used to supervise the entire system operation, including the crossbar networks
- > At one time only one crosspoint switch can be set on in each row and each column
- > Interprocessor crossbar provides permutation connections among the processors
- Only one-to-one connections are provided
- \triangleright The $n \times n$ crossbar connects at most n source, destination pairs at a time
- \triangleright Crossbar switch is the most expensive one to build, due to the fact that its hardware complexity increases to n^2
- For a small network size, it is the desired choice

Summary of Dynamic Connection Networks

Network Characteristics	Bus System	Multistage Network	Crossbar Switch
Minimum latency for unit data transfer	Constant	$O(\log_k n)$	Constant
Bandwidth per processor	O(w/n) to $O(w)$	O(w) to O(nw)	O(w) to O(nw)
Wiring Complexity	O(w)	$O(nw \log_k n)$	$O(n^2 w)$
Switching Complexity	O(n)	$O(n \log_k n)$	$O(n^2)$
Connectivity and routing capability	Only one to one at a time.	Some permutations and broadcast, if network unblocked	All permutations one at a time.
Early representative computers	Symmetry S-1, Encore Multimax	BBN TC-2000, IBM RP3	Cray Y-MP/816, Fujitsu VPP500
Remarks	Assume n processors on the bus; bus width is w bits.	$n \times n$ MIN using $k \times k$ switches with line width of w bits.	Assume $n \times n$ crossbar with line width of w bits.