USB PD and other fast charging protocol power receiving chip CH224

Chinese

manual

version: 1G http://wch.cn

1. Overview

CH224 single chip integrates multiple fast charging protocols such as USB PD, supports PD3.0/2.0, BC1.2 and other boost fast charging protocols, and automatically detects VCONN and analog E-Mark chip, supports up to 100W power, built-in PD communication module, high integration, and simplified peripherals. Integrated output power It has a voltage detection function and provides over-temperature and over-voltage protection. It can be widely used in various electronic devices to expand high-power input such as wireless charging. Electric toothbrushes, rechargeable shavers, lithium battery power tools and other applications.

2. Features

ÿSupport 4V to 22V input voltage

ÿSupport PD3.0/2.0, BC1.2 and other fast charging protocols

ÿSupport USB Type-C PD, support forward and reverse plug detection and automatic switching

ÿSupport E-Mark simulation, automatic detection of VCONN, support 100W PD request

ÿThe requested voltage can be adjusted dynamically through various methods

ÿSingle chip has high integration, simple periphery and low cost

ÿBuilt -in overvoltage protection module OVA, over-temperature protection module OTA

3. Application

Wireless charger

Laptop charging cable

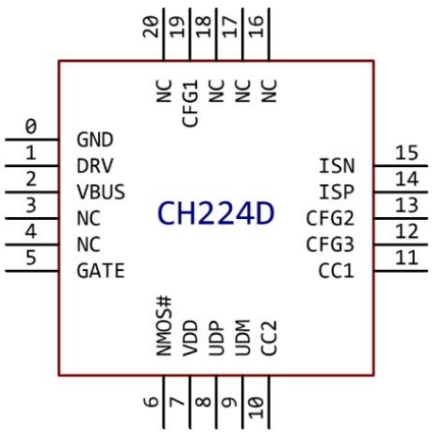
ÿLithium battery small appliances

ÿLithium battery power tools

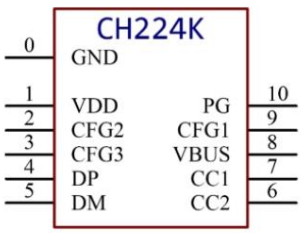
ÿMobile power supply

4. Pins

4.1.CH224 Package Pin Arrangement



QFN20-3*3



ESSOP-10

SOT23-6L

4.2.CH221K pin function description

Pin Number	Pin Name Type		Pin Description
1	VDD		Power supply input, external 1uF decoupling capacitor, series resistor to VBUS
2	GND		Power supply working power common ground terminal
3	PG open-drain output default Power Good indication, low level valid, customizable function		
4,5	CC1, CC2 Bidirectional		Type-C CC bus
6	CFG Analog Input		Power range configuration input

4.3.CH224K pin function description

Pin Number	Pin Name Type		Pin Description
0	GND		Power supply common ground terminal, heat dissipation base plate
1	VDD		Power supply input, external 1uF decoupling capacitor, series resistor to VBUS
4,5	DP,DM bidirectional		USB bus
6,7	CC1, CC2 Bidirectional		Type-C CC bus
2,3,9	CFG1,CFG2, CFG3	Analog Input	Power range configuration input
8	VBUS analog input voltage detection input, requires series resistor to external input VBUS		
10	PG open-drain output default Power Good indication, low level valid, customizable function		

4.4.CH224D pin function description

Pin Number CH224D	Pin Name Type		Pin Description
0	GND	Power	Common ground terminal, heat sink
2	VBUS	supply	Working power input
7	VDD	Power supply	Internal regulator output, external 1uF decoupling capacitor
8ÿ9 10ÿ	DP,DM bidirectional		USB bus
11 19ÿ13ÿ	CC1, CC2 Bidirectional		Type-C CC bus
12	CFG1~3 input CFG1 is analog input, CFG2, 3 are digital inputs with built-in pull-down		
1	DRV Analog Output		Weak drive output for driving configuration resistors
14ÿ15	ISP,ISN differential input		Used to detect working current, customized function
5	GATE high voltage output		Used to drive high-side power path NMOS, customized functions
6	NMOS# Digital Input		GATE pin drives NMOS enable, low level is effective

5. Functional Description

5.1. Overview

CH224 is a protocol power receiving IC that supports PD3.0/2.0, BC1.2 and other boost fast charging protocol inputs, and supports power supply in the range of 4 to 22V. The voltage level requested can be dynamically configured in a variety of ways.

CH221K only supports PD3.0/2.0 protocol.

CH224K/CH224D provide single resistor configuration and level configuration. CH221K only provides single resistor configuration.

5.2. CH224K/CH224D voltage range configuration

5.2.1 Single resistor configuration

Applicable to applications where different requested voltages can be achieved on the same PCB by modifying the resistance value.

CFG1 connects a resistor to GND, and different resistance values correspond to different voltage request levels. When using a single resistor configuration, CFG2 and CFG3 pins Can be left floating. The resistor-required voltage comparison table is as follows.

CFG1 resistance	Request voltage
6.8Kÿ	9V
24Kÿ	12V
56Kÿ	15V
NC	20V

5.2.2 Level Configuration

It is suitable for applications where the MCU dynamically adjusts the requested voltage or the PCB circuit has a fixed requested voltage.

CFG1, CFG2, CFG3 are directly connected to the IO port of the external MCU, or directly connected to the VDD/GND pin of the CH224K/CH224D chip. The level configures the requested voltage. The truth table is as follows.

CFG1	CFG2	CFG3	Request voltage
1	.	.	5V
0	0	0	9V
0	0	1	12V
0	1	1	15V
0	1	0	20V

When using the level configuration method, you need to pay attention to the IO port voltage and default status used.

For CH224K, the input voltage of CFG2/CFG3 pin cannot be higher than 3.7V. For CH224D, the input voltage of CFG2/CFG3 pin cannot be higher than 3.7V. The voltage cannot be higher than 5V.

If the MCU and other backend circuits start up slowly, or the MCU pins have specific default states, CFG1 may be in a floating state or IO configuration mode, it is possible to request 20V at this time. If the system cannot withstand 20V input, a configuration resistor should be added to the CFG1 pin to Ensure that before the MCU starts, CH224K/CH224D can request the appropriate voltage through resistor configuration.

5.3. CH221K voltage range configuration

CFG connects a resistor to VDD, and different resistance values correspond to different voltage request levels. The resistor-request voltage comparison table is as follows.

CFG to VDD resistance	Request voltage
10Kÿ	5V
20Kÿ	9V
47Kÿ	12V
100Kÿ	15V
200Kÿ	20V

5.4. Simulate E-Mark function

To use the analog E-Mark function to request an output greater than 20V or greater than 60W, you must use a Type-C male connector and connect it to the CC2 Connect a 1Kÿ resistor to the GND pin. (Please consult our technical support)

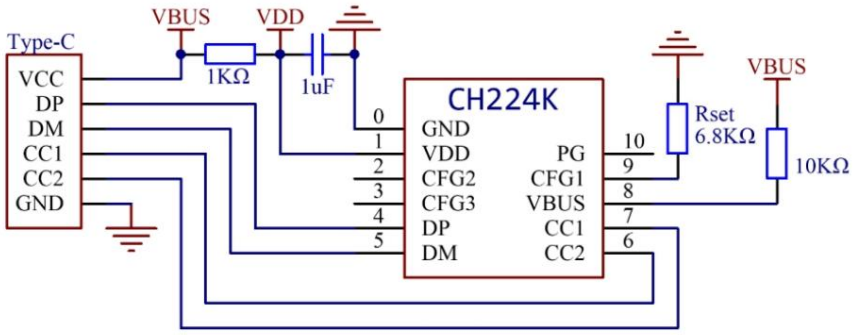
5.5. Use PD protocol only

If you do not need to use the A-port protocol (various protocols implemented by DP and DM communications), you can choose the CH221K model.

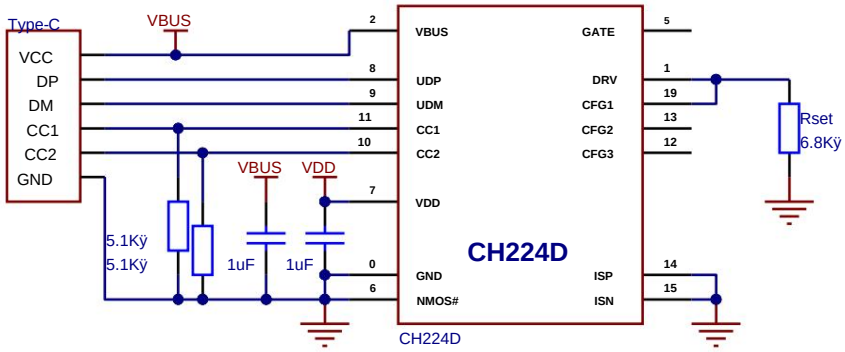
If you want to block these protocols on CH224K/CH224D, you need to disconnect the DP/DM pins of CH224K/CH224D from the Type-C interface. DP/DM connection, and short DP and DM on the CH224K/CH224D side. For CH224K, the VBUS pin can be NC at this time.

6. Reference Schematic

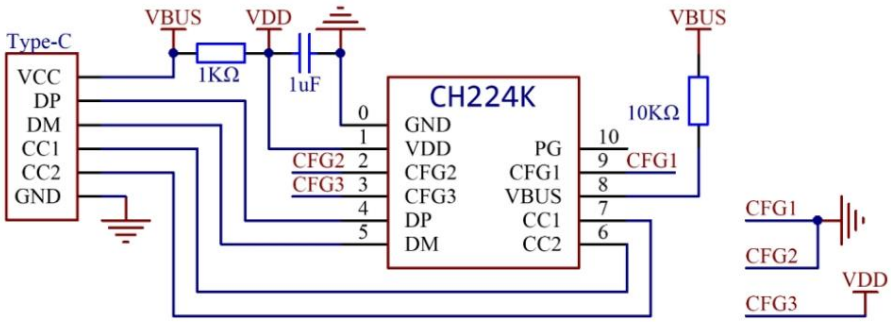
6.1.CH224K/CH224D uses Type-C female port, single resistor configuration 9/12/15/20V (resistor configuration 6.8Kÿ is 9v in the figure)



Rset resistance request voltage	
6.8Kÿ	9V
24Kÿ	12V
56Kÿ	15V
NC	20V

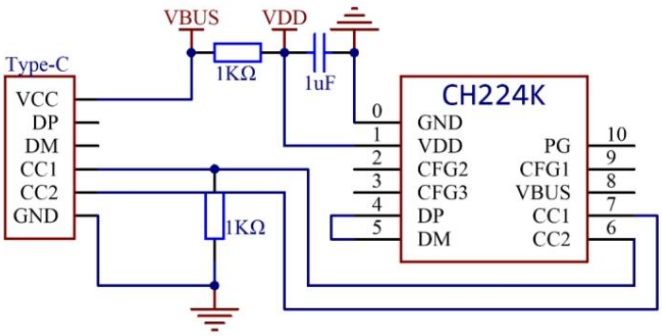


6.2.CH224K uses Type-C female port, level configuration 5/9/12/15/20V (level configuration in the figure is 12v)

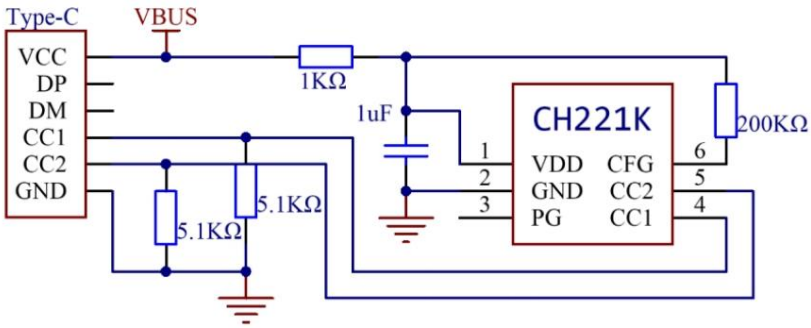


CFG1	CFG2	CFG3	ask Voltage
1			5V
0	0	0	9V
0	0	1	12V
0	1	1	15V
0	1	0	20V

6.3.CH224K uses Type-C male port, only uses PD protocol and E-Mark simulation function (resistor configuration NC is 20v in the figure)



6.4.CH221K uses Type-C female port, single resistor configuration 20V



7. Parameters

7.1. Absolute Maximum Ratings of CH221K Chip

(Critical or exceeding the absolute maximum value may cause the chip to malfunction or even be damaged)

name	Parameter Description	Minimum	Maximum	Unit
FACING	Ambient temperature during	-40	105	ÿ
TS	operation Ambient temperature	-55	150	ÿ
VDD	during storage Operating power supply voltage (VDD pin connected to power supply,	-0.5	5.8	V
VODHP	GND pin connected to ground) Voltage on high-voltage open-drain output pin PG	-0.5	13.5	V
VIOCC	Voltage on CC1, CC2 pins	-0.5	8	V
VIOUX	Voltage on CFG pin	-0.5	VDD+0.5	V
PD	Maximum power consumption of the whole chip (VDD voltage*current)		250	mW

7.2. Absolute Maximum Ratings of CH224K Chip

(Critical or exceeding the absolute maximum value may cause the chip to malfunction or even be damaged)

name	Parameter Description	Minimum	Maximum	Unit
FACING	Ambient temperature during	-40	90	ÿ
TS	operation Ambient temperature	-55	105	ÿ
VDD	during storage Operating power supply voltage (VDD pin connected to power	3.0	3.6	V
VIOHV	supply, GND pin connected to ground) Voltage on pins supporting high voltage (CFG, VBUS)	-0.5	13.5	V
VIOCC	Voltage on CC1, CC2, CFG1 pins	-0.5	8	V
VIOUX	Voltage on DP, DM, CFG, CFG2, CFG3 pins	-0.5	VDD+0.5	V
VIOLV	Voltage on CFGHV pin		0.8	V
PD	Maximum power consumption of the entire chip (VDD voltage*current)		400	mW

7.3. Absolute Maximum Ratings of CH224D Chip

(Critical or exceeding the absolute maximum value may cause the chip to malfunction or even be damaged)

name	Parameter Description	Minimum	Maximum	Unit
FACING	Ambient temperature during operation	-40	100 ÿ	
TS	Storage ambient temperature	-55	125 ÿ	
VDD	Working power supply voltage (VDD pin connected to power supply, GND pin connected to ground)	-0.5	6	V
VIOHV	Voltage on VBUS pin	-0.5	24	V
VIOCC	Voltage on CC1, CC2 pins	-0.5	20	V
VIOUX	Voltage on DP,DM,CFG1,CFG2,CFG3,DRV,NMOS#,ISP,ISN pins -0.5 VDD+0.5			V
VIOHX	Voltage on the GATE pin	-0.5 VIOHV+6.5 V		
PD	Maximum power consumption of the entire chip (VDD voltage*current)		300	mW

7.4.CH221K chip electrical parameters (test conditions: TA = 25°C)

name	Parameter Description	Min	Typ	Max	Unit
VLDOK	CH221K Internal power regulator VDD shunt voltage	3.0	3.3	3.6	V
IN LINE	regulation Internal power regulator VDD shunt current	0		30	mA
VR	absorption capability Power supply power-on reset voltage threshold	2.2	2.4	2.6	V

7.5.CH224K chip electrical parameters (test conditions: TA=25ÿ)

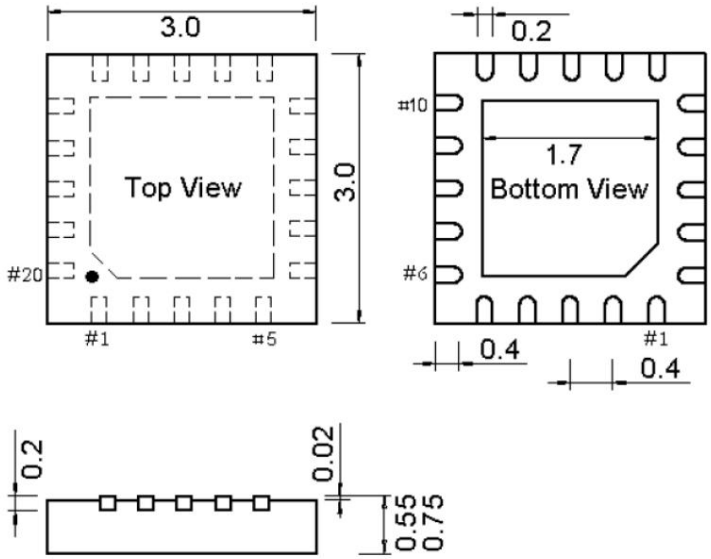
name	Parameter Description	Min	Typ	Max	Unit
VLDOK	CH224K Internal power regulator VDD parallel voltage regulation	3.24	3.3	3.36	V
IN LINE	Internal power regulator VDD parallel current absorption capability	0		30	mA
ALL	Over temperature protection module OTA reference	90	105	120 ÿ	
VR	threshold temperature Power supply power-on reset voltage threshold	2.2	2.4	2.6	V

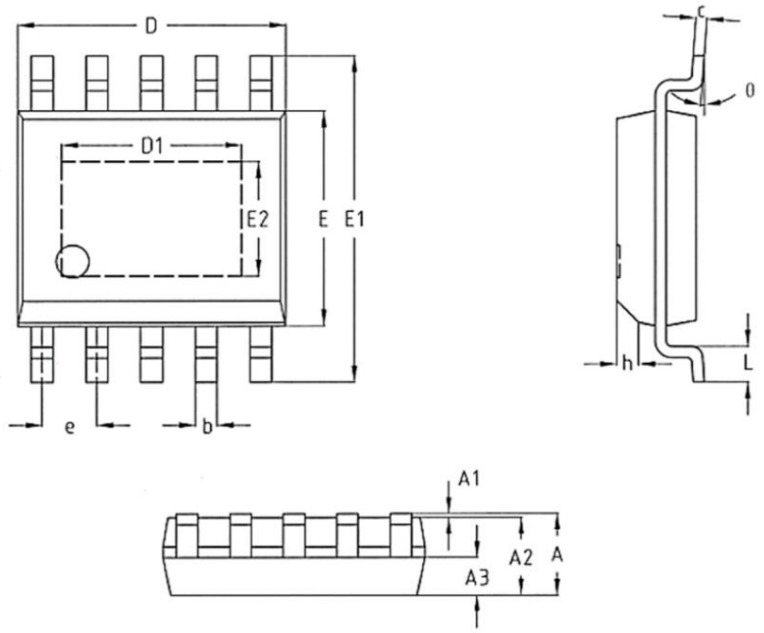
7.6. Electrical parameters of **CH224D chip (test conditions: TA=25ÿ)**

name	Parameter Description	Min	Typ	Max	Unit
VLDO	Internal power regulator VDD output voltage	4.65	4.7	4.75	V
IN LINE	Internal power regulator VDD external load capacity			10	mA
VR	Power supply power-on reset voltage threshold	2.2	2.4	2.6	V

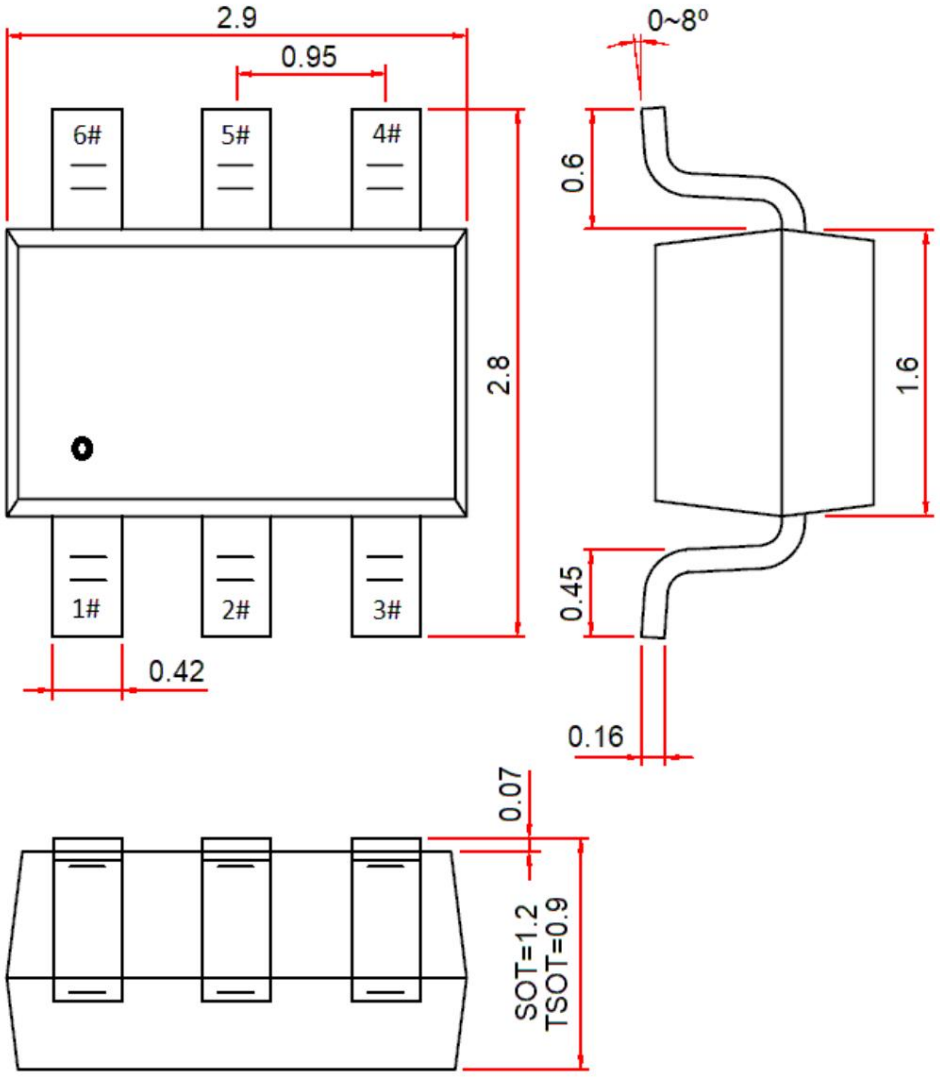
8. Packaging information

Package	Body Width		Pin spacing		Package	Order Model
QFN20	3*3mm	118mil	Description 0.40mm 15.7mil Quad Flat No Lead Package CH224D 39mil Narrow			
ESSOP10	3.9mm	150mil	1.00mm	Pitch 10-pin SMD with Base Plate CH224K Small 6-pin SMD		
SOT23-6L	1.6mm	63mil	0.95mm	37mil		CH221K





符号	标称值
A	1.6
A2	1.45
D	4.9
D1	3.3
E	3.9
E1	6.0
E2	2.1
b	0.4
e	1.00BSC
c	0.2



Note: The unit marked in the package information diagram is mm (millimeter).