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S1R72U16
USB2.0 PCB Design Guide

SEIKO EPSON CORPORATION

Rev.1.00

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Scope

This document applies to the S1R72U16 IDE device - USB 2.0 host bridge LSI.

Table of Contents

1. Purpose

This document is intended to serve as a guide to USB 2.0 transceiver macro peripheral components when designing circuit boards. The details described here focus on implementing USB 2.0 functions, omitting discussion of precautionary points related to general circuit board design.

The circuits, components, and parameters described in this document are intended for reference purposes only. They do not represent a guarantee of performance. The user is solely responsible for selecting the circuit configurations appropriate for the systems in question. For detailed information on component specifications and usage instructions, contact the component manufacturer. For detailed information on circuit board specifications, contact the circuit board manufacturer.

Refer to the following pertinent documents(※) published by the USB Implementers Forum (USB-IF) in conjunction with this document.

※ The documents listed below are subject to change without notice.

Related document:

High Speed USB Platform Design Guidelines Rev.1.0 (Apr 01)

http://www.usb.org/developers/docs/

2. Board Design Guidelines

2.1 DP/DM Signal Routing

The DP/DM signal must be routed to account for the following:

- The signal line differential impedance should be 90 Ω. Take special care to match the characteristic impedance when incorporating other connectors or cables between the LSI and receptacle A.
- The inner layer immediately below the signal lines must be a GND plane with no separation.
- The signal lines must be of short length to ensure that signal propagation delays do not exceed 3 ns between the LSI's pin and the receptacle A's pin.
- The signal lines must be of equal length and arranged in parallel to prevent skew and to stabilize differential impedance.
- Signal reflections must be minimized.
  - Signal line branching must be kept to a minimum (Refer to "3.3 Signal Line Layout").
  - Implement curve routing if the signal lines are laid out at the corner.

- Other signal lines must be kept separate to prevent interference with the signal line differential impedance. In particular, the following signal lines must be kept at an adequate distance from the DP/DM signal lines.
  - Clock signal line
  - High-speed signal line
  - VBUS line

2.1.1 Basic Routing

This is a typical routing configuration for the DP/DM signal between the LSI and receptacle A, based on manufacturing experience with the Seiko Epson Evaluation Board (manufactured by Kyoden Co., Ltd.). This example is intended to show a basic routing layout. It omits layout and routing for components added between the LSI and receptacle A.

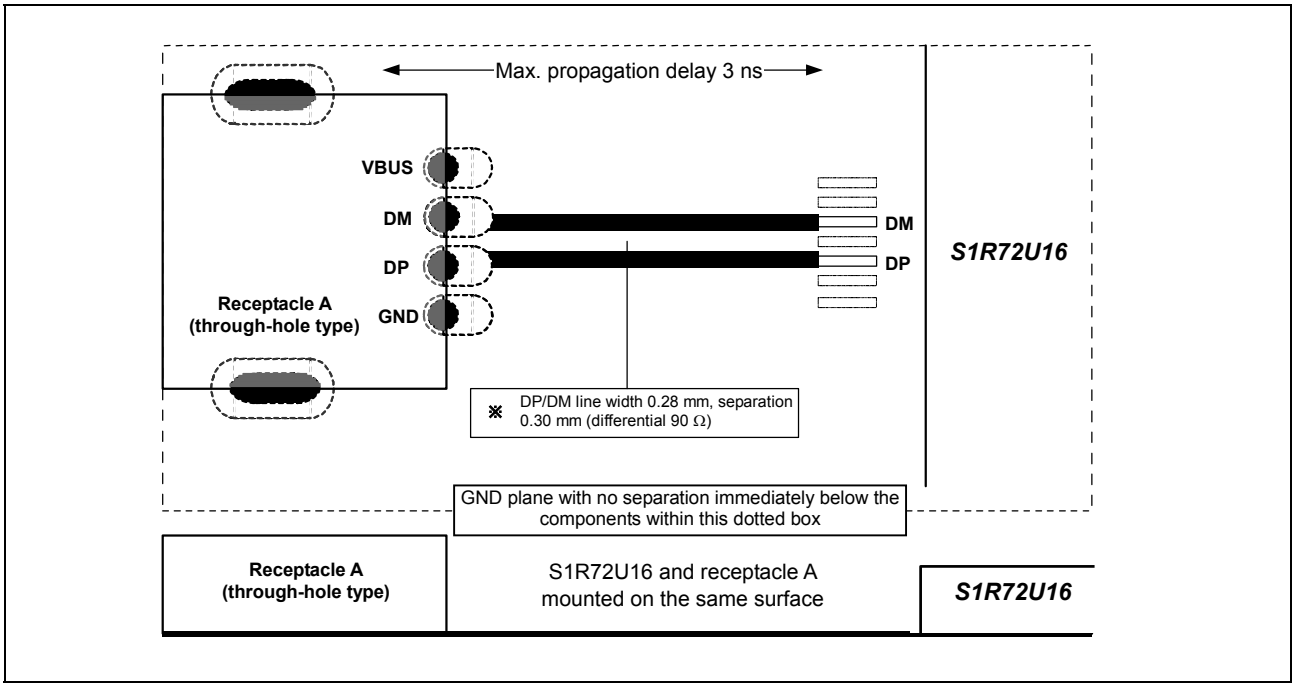


Figure 2-1 DP/DM signal line routing example

2.1.2 Circuit Board Layer Configuration

The diagrams below show typical layer configurations for printed circuit boards of 1.6 mm in thickness consisting of four and six layers, based on manufacturing experience with the Seiko Epson Evaluation Board (manufactured by Kyoden Co., Ltd.).

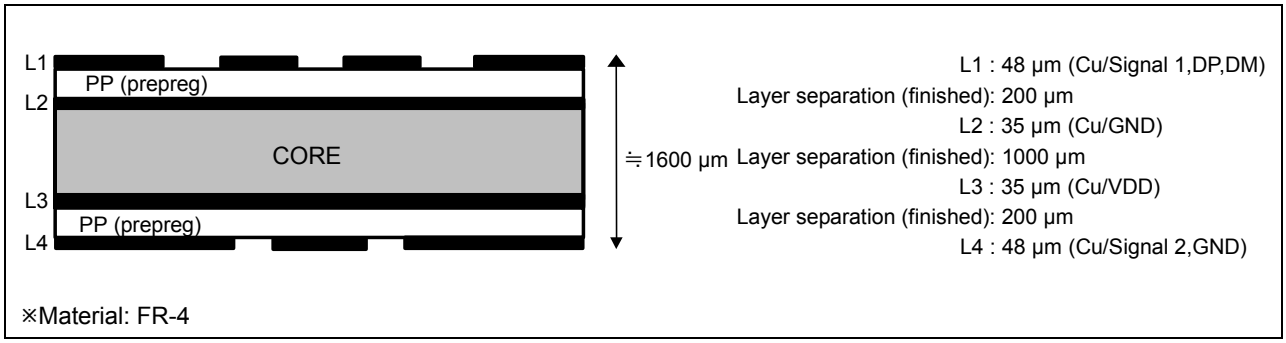


Figure 2-2 Four-layer printed circuit board layer configuration

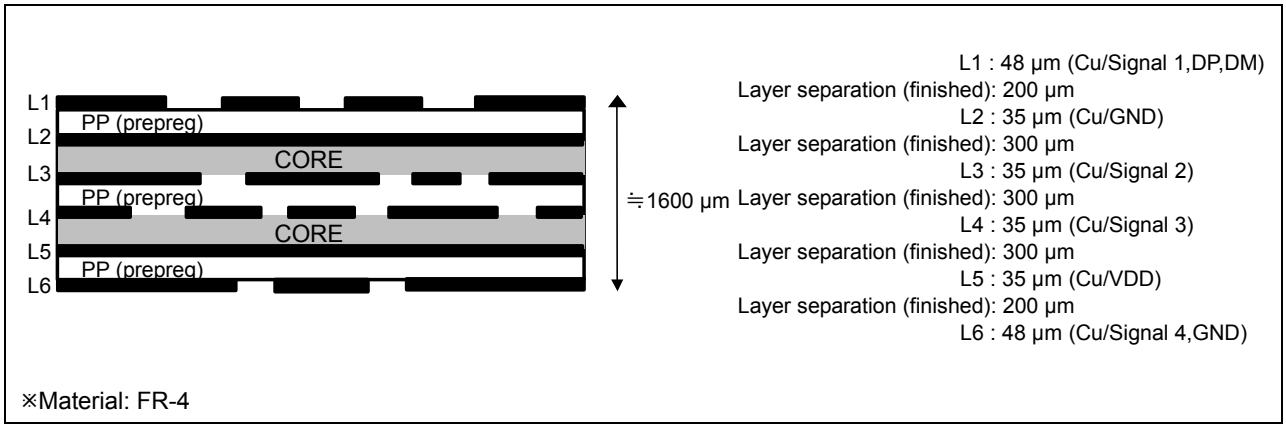


Figure 2-3 Six-layer printed circuit board layer configuration

2.2 USB Block Circuits

Consider the following issues with this LSI's USB block circuits.

- Locate the 6.2 kΩ ±1% resistor connected to R1 pin as close as possible to R1 pin.
- Connect the VSS pins (see Figures 2-4 and 2-5) belong to the USB 2.0 transceiver macro block to the shared GND with no separation using a low impedance configuration.
- Locate the decoupling capacitors close to the corresponding power supply pins.

2.2.1 QFP14-80 Package

The figure below illustrates the typical USB block circuits for the QFP14-80 package.

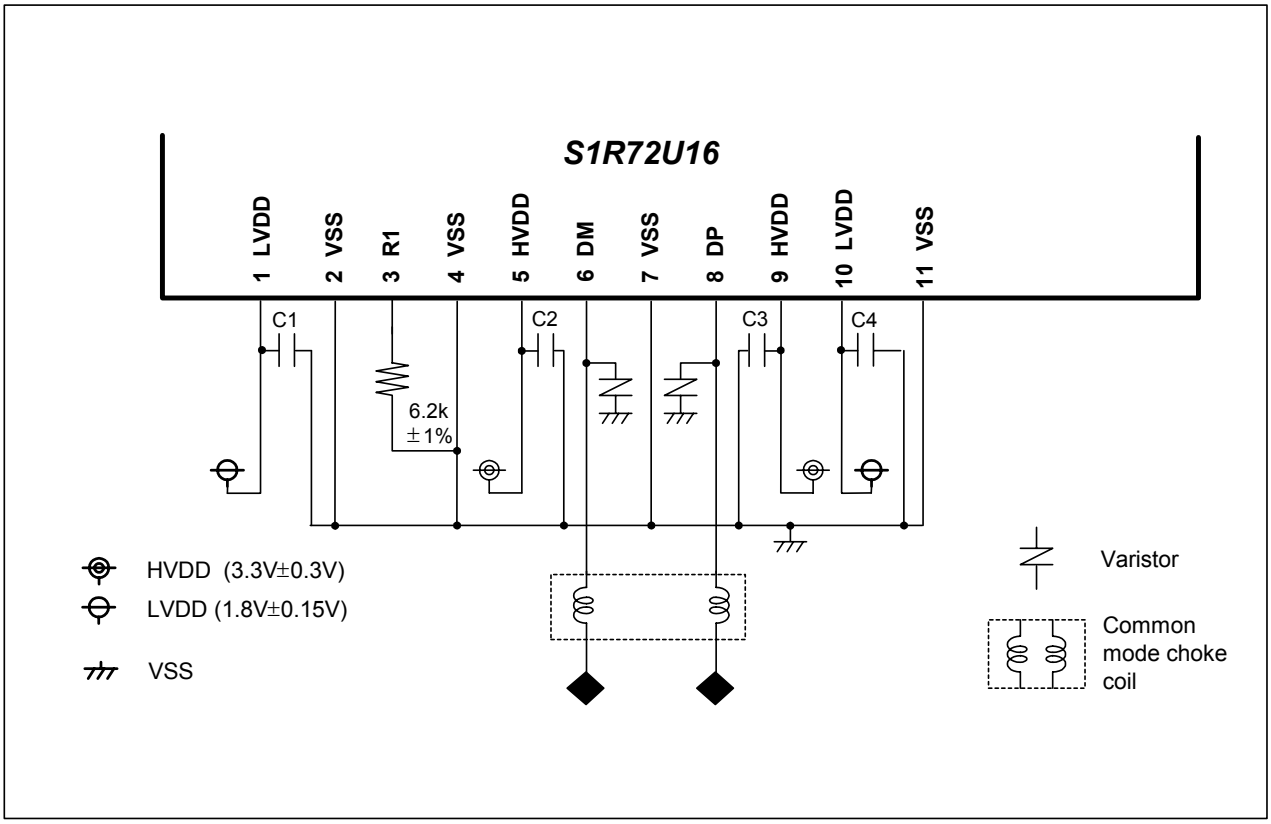


Figure 2-4 QFP14-80 package USB block circuits

2.2.2 PFBGA8UX81 Package

The figure below illustrates the typical USB block circuits for the PFBGA8UX81 package.

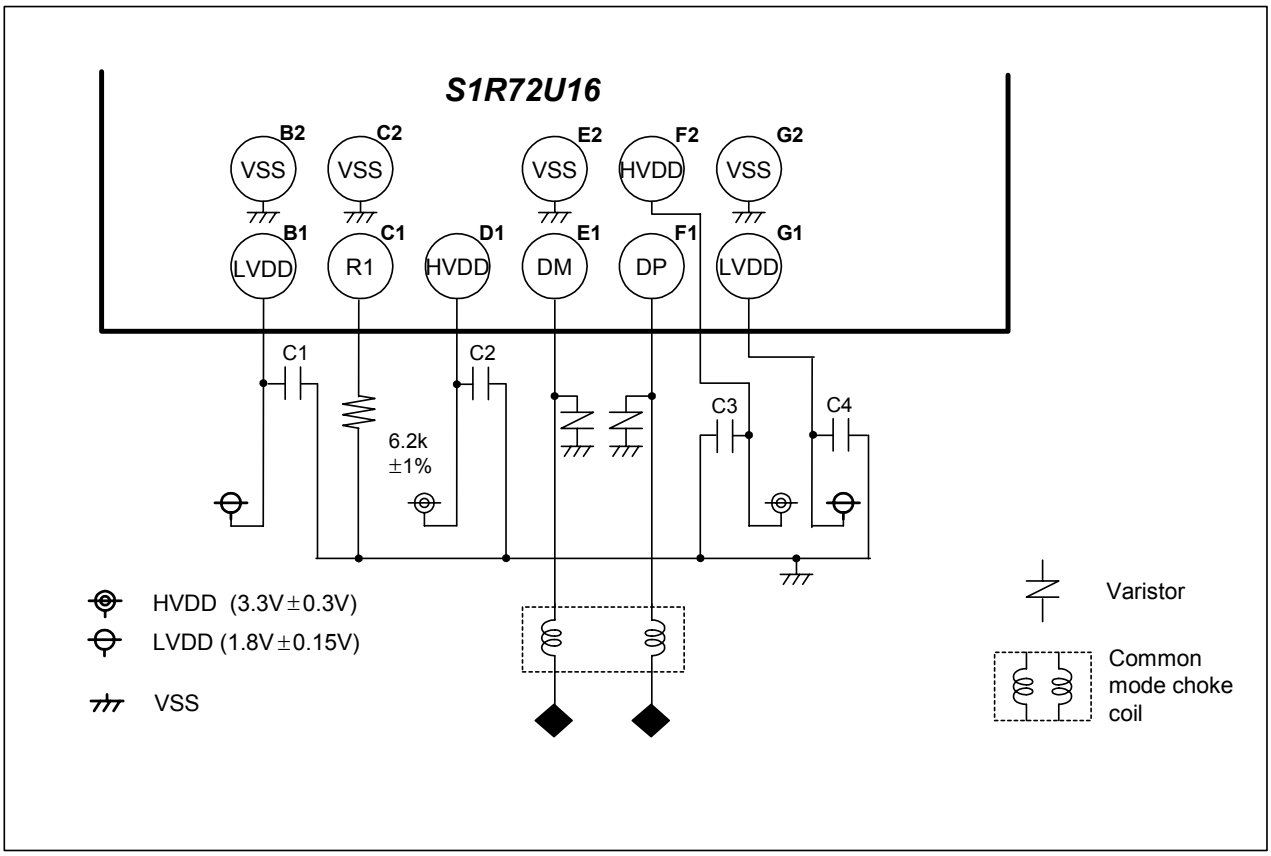


Figure 2-5 PFBGA8UX81 package USB block circuits

2.2.3 Decoupling Capacitor and VDD-GND Plane between Power Supplies

The table below shows typical capacitance values for the decoupling capacitor between the power supplies.

Depending on the printed circuit board configuration, it may be possible to improve USB signal jitter by adding a capacitor of higher capacitance than C2 and C3 between HVDD pin and VSS. If so, C2 and C3 must be located immediately the corresponding HVDD pins.

Table 2-1 Power supply decoupling capacitor capacitance values

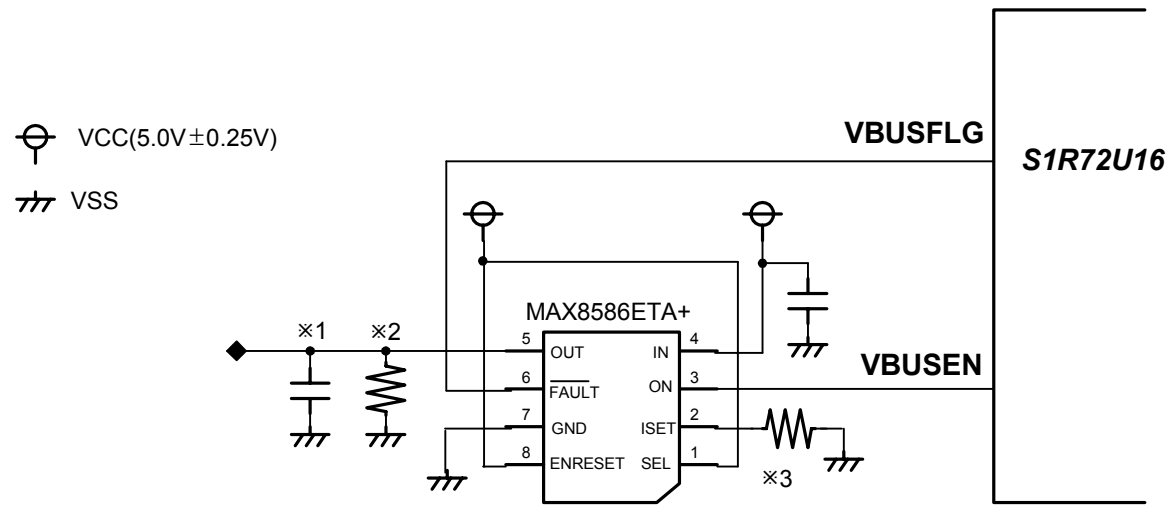
Capacitor (Figs. 2-4, 2-5)	C1 (uF)	C2, C3 (uF)	C4 (uF)
Reference value	1	0.1	1

Inadequate VDD/GND plane characteristics will affect differential signal characteristics for example increasing jitter. If using a switching regulator, design the printed circuit board to ensure the lowest possible switching noise.

2.2.4 VBUS Supply Control Circuits

The figure below illustrates a typical control circuit for the VBUS power supply (+5 V). The example shown here uses a Maxim MAX8586ETA+ as the USB power switch IC, with overcurrent protection and reverse current protection(※) features.

※ If the OUT pin's side voltage exceeds the IN pin's side voltage, watch for a reverse current that may flow from the OUT pin's side to the IN pin's side with USB power switch ICs that don't have reverse current protection features.



※1: Section 7.2.4 of the USB 2.0 standards stipulates the following: "USB downstream port VBUS lines must be bypassed by a capacitor of at least 120 µF." The Seiko Epson Evaluation Board uses a capacitor equivalent to 122 µF.

※2: Resistor for discharging the load stored in a capacitor exceeding the 120 µF described above.
The Seiko Epson Evaluation Board uses a 100 kΩ resistor.

※3: Resistor for determining the overcurrent detection value. For detailed information, refer to the USB power switch IC specifications.

Figure 2-6 VBUS supply control circuits

2.2.5 Oscillator Circuits

Select a crystal oscillator oscillation frequency of 24 MHz or 12 MHz. While the high-speed data rate is nominally 480.00 Mb/s with a required bit rate accuracy of ±500 ppm, we recommend a crystal oscillator with oscillation frequency accurate to within ±100 ppm to ensure satisfactory waveform quality.

Since oscillator clock fluctuations due to noise may cause malfunctions, consider the following for layouts.

- XI and XO signals must be routed with the shortest possible routes.
- Large-current signals or high-speed operation signal lines must be located at the proper distance from oscillator circuits.

Figure 2-7 illustrates a typical crystal oscillator connection circuits. Table 2-1 shows typical circuit constants for a Seiko Epson Evaluation Board using an Epson Toyocom crystal oscillator.

Confirm circuit constants using the oscillator by manufacturer's matching evaluations. Oscillation characteristics will vary with actual implementation conditions, including actual components and circuit board patterns.

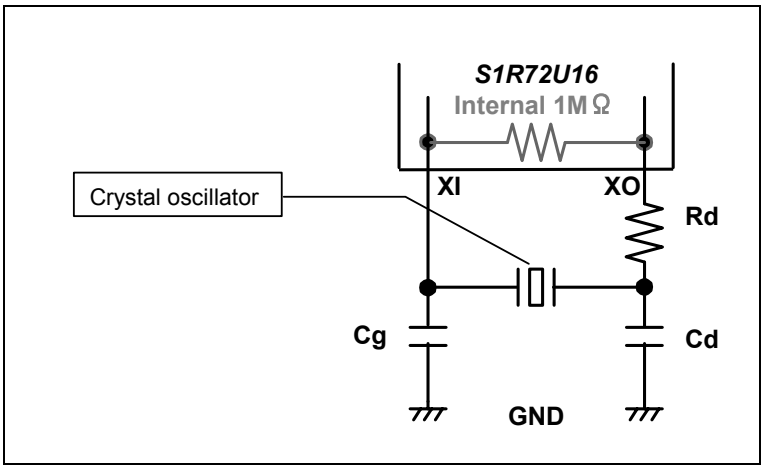


Figure 2-7 Crystal oscillator connection circuits

Table 2-2 Seiko Epson Evaluation Board circuit parameters

Epson Toyocom crystal oscillator	Oscillation frequency (MHz)	Circuit parameters		
		Cg (pF)	Cd (pF)	Rd (Ω)
FA-128 (CL=10pF±50ppm)	24	9	9	1000
FA-238V (CL=10pF±50ppm)	12	15	15	470

Note that the CLKSEL pin must be set to match the oscillation frequency of the crystal oscillator. For detailed information on the CLKSEL pin settings, refer to "6. Pin Functions" in the *S1R72U16 Data Sheet*.

3. Components Used on DP/DM Signal Lines

This section describes the components used on DP/DM signal lines.

3.1 Common Mode Choke Coil

Using a common mode choke coil on DP/DM signal lines will improve skew and reduce unwanted radiated noise. Some common mode choke coils are listed below. With common mode choke coils, we recommend locating common mode choke coils in line with DP/DM signal lines. For detailed information on typical routing layouts, refer to "3.3 Signal Line Layout."

[TDK ACM2012-900-2P]

[Murata DLW21SN900SQ2]

[TOKO 985BH－1007]

3.2 Chip Varistor

Using a chip varistor on the DP/DM signal lines protects this LSI's DP/DM pins against static electricity and surges. Examples of chip varistors supporting USB 2.0 High-Speed are listed below. With chip varistors, we recommend deploying the shortest possible branch lines from the DP/DM signal lines to the chip varistors. For detailed information on typical routing layouts, refer to "3.3 Signal Line Layout."

[TDK AVR Series]

[Matsushita Electric EZJZ Series]

3.3 Signal Line Layout

The figure below illustrates a typical routing layout for the above components on DP/DM signal lines with the shortest possible signal line branches.

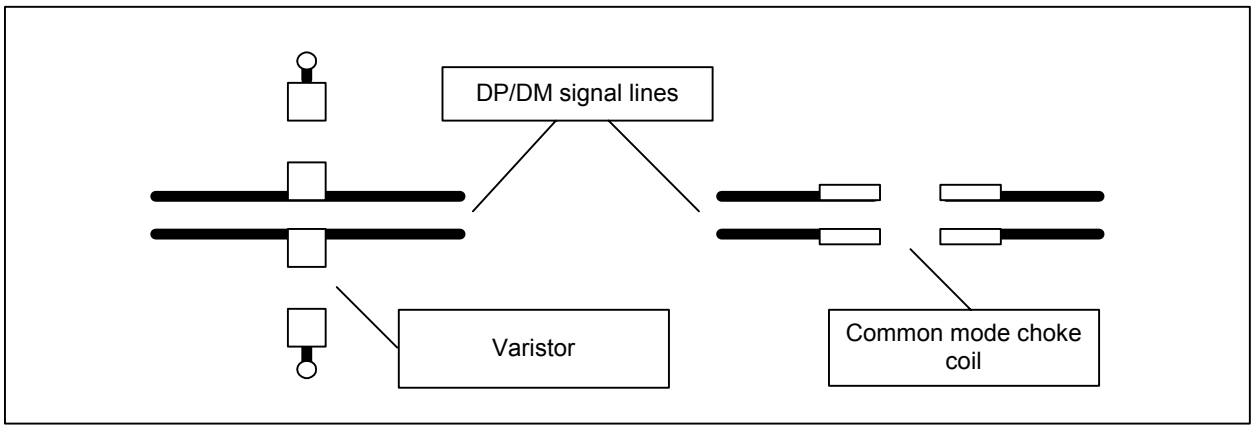


Figure 3-1 Signal line routing

3.4 Effect on High-Speed Transmission Waveform Rising and Falling Characteristics

Adding components with capacitance in DP/DM signal lines will increase the capacitance of the signal lines, and especially moderate rising and falling characteristics (T_{HSR}/T_{HSF}) of the High-Speed transmission waveform. Caution is required to ensure that the eye pattern is not treated as "fail."

3.5 Receptacles/Connectors/Cables

Use of receptacles, connectors, or cables that are not USB-certified may degrade DP/DM differential signal characteristics. We recommend using USB-certified receptacles, connectors, and cables, since differential signal characteristic degradation will adversely affect eye pattern quality.

4. Sample Differential Signal Characteristics

The figure below illustrates Hi-Speed eye pattern waveforms for a Seiko Epson Evaluation Board designed in accordance with this document. The board has passed USB-IF Embedded Host Compliance Test.

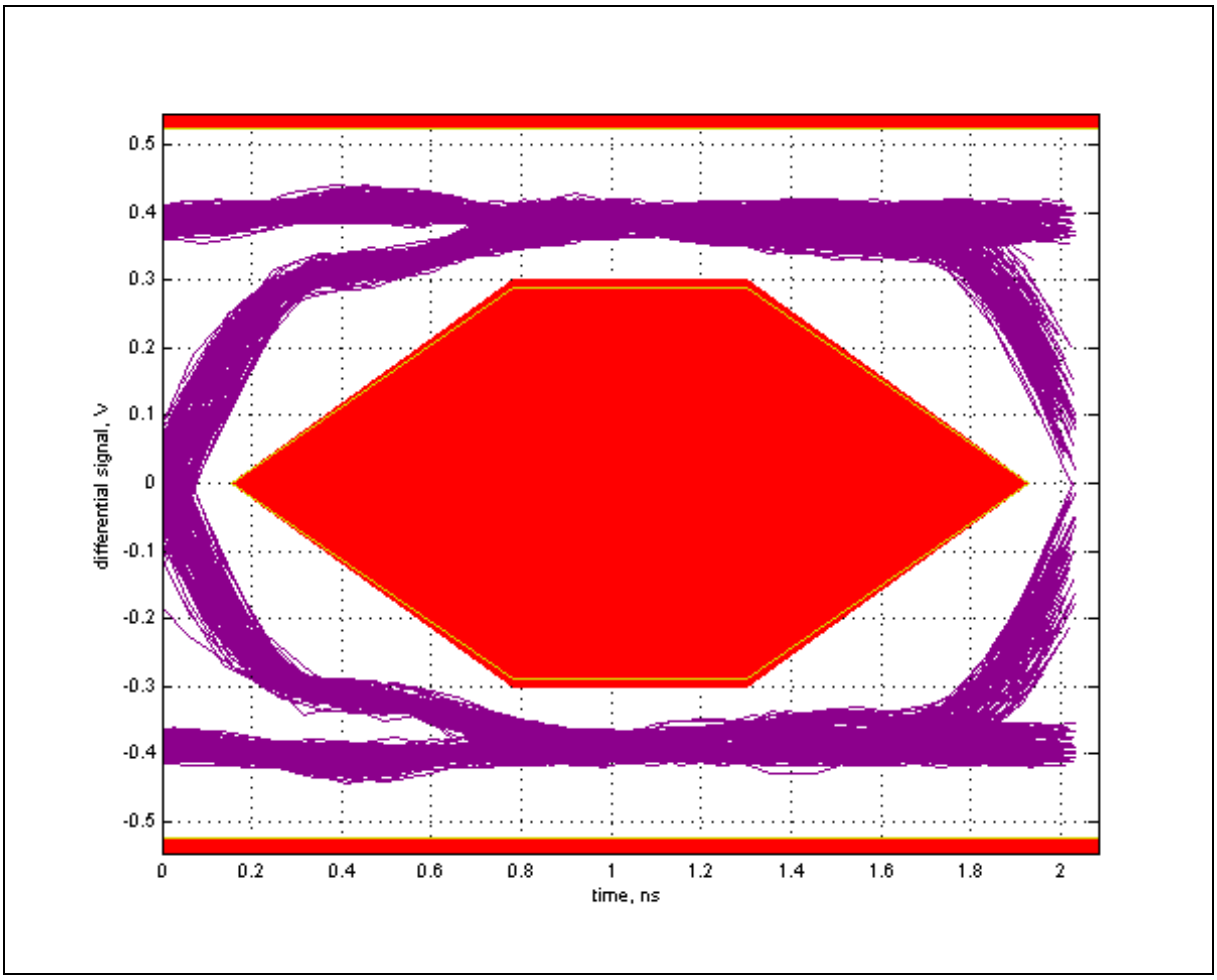


Figure 4-1 Hi-Speed eye pattern waveform

※ The eye pattern waveform observed will vary depending on transfer circuit characteristics, power supply characteristics, and measurement environment on circuit board.

Revision History

Date	Revision details			
	Rev.	Page	Type	Details
06/01/2007	0.79	All	New	Newly established
07/01/2007	1.00	2.2.5	Correct	Corrected circuit constant values for FA-128.
		2.2.5	Correct	Added circuit constant values for FA-238V.
		4	Correct	Added descriptions of passing compliance test.

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Document Code: 411137700
First Issue July 2007
Printed August 2007 in JAPAN