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S1R72U16
Embedded Host Compliance Guide

SEIKO EPSON CORPORATION

Rev.1.00

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Scope

This document applies to the S1R72U16 IDE device - USB 2.0 host bridge LSI.

Table of Contents

1. Purpose

This document is intended to guide users using the S1R72U16 in performing Embedded Host Compliance Testing.

In conjunction with this document, refer to the following documents(※) published by the USB Implementers Forum (USB-IF).

※ The documents listed below are subject to change without notice.

Related documents:

USB-IF Embedded Host Compliance Plan Rev 1.0 (Aug 06)

http://www.usb.org/developers/docs/

Embedded High-speed Host Electrical Test Procedure Rev 1.01 (May 06)

http://www.usb.org/developers/onthego/

USB-IF Full and Low Speed Electrical and Interoperability Compliance Test Procedure (Feb 04)

http://www.usb.org/developers/docs/

Host High-Speed Electrical Test Procedure

http://www.usb.org/developers/docs/

High-Speed Electrical Test Specification Rev 1.03 (Jan 05)

http://www.usb.org/developers/docs/

On-The-Go Supplement to the USB 2.0 Specification Rev 1.3 (Dec 06)

http://www.usb.org/developers/onthego/

USB On-The-Go Compliance Plan for the USB 2.0 Specification Rev 1.2 (Apr 06)

http://www.usb.org/developers/onthego/

2. Terminology and Abbreviations

The terminology and abbreviations used in this document are defined below.

USB-IF

USB Implementers Forum

TPL

Target Peripheral List

NSF

No Silent Failure

HS

High-speed

FS

Full-speed

LS

Low-speed

SOF

Start of Field

EOP

End of Packet

Embedded Host

Limited-function host intended for use with built-in systems, not full-function hosts such as PCs.

Standard-A receptacle

Connector used with the USB host (downstream) port.

The USB 2.0 standards explicitly categorize board connectors as receptacles and cable connectors as plugs.

Mini-AB receptacle

Board connector used as an On-The-Go (OTG) port.

Can be mated with both Mini-A and Mini-B plugs.

Test Fixture

HS Electrical Testing measurement board provided by measuring instrument manufacturers approved by the USB-IF.

Test mode

Operating mode used in HS Electrical Testing. It is mandatory for HS-compliant systems.

EL_

Electrical standards for HS compliance. Details are given in *High-Speed Electrical Test Specifications*.

USB Electrical analysis tool

Analysis tool provided by the USB-IF.

Far End

5 m from the wave-measuring system.

Near End

Close to the wave-measuring system.

Captive USB cable

USB cable provided with Test Fixture.

Load board

A VBUS Load board used for Drop/Droop Testing and released by the USB-IF as the OTG Electrical Tester (OET).

Interpacket gap

Interval between packets.

Test lab

Company approved by the USB-IF to perform conformance testing.

3. Embedded Host System

This LSI can be used to easily implement an embedded host system.

The details of embedded host systems are outlined below. The compliance offered by this LSI is described in "4.1 Introduction (Summary)."

- Limited host functions (does not require a full-function host such as a PC)
  - Full support for HS, FS, and LS is not required.
  - Only support for control transfer is mandatory. Support for all other transfer types is optional.
  - Support for USB Suspend is optional.
  - The VBUS supply current need only be 8 mA or higher.
  - The range of devices supported can be restricted.
  - Hub support is optional.
  - Features allow user notification of errors detected by the USB function.
- There is at least one host (downstream) port with a Standard-A receptacle.
  - Support for USB On-The-Go Compliance Testing is required if it has a Mini-AB receptacle.
- The implementation of device (upstream) ports is optional.
  - If implemented, these ports must pass the USB Peripheral Compliance Test to ensure Embedded Host compliance.

4. Embedded Host Compliance Plan

The *USB-IF Embedded Host Compliance Plan* contains rules and requirements for achieving embedded host compliance.

This section describes the corresponding LSI specifications and the compliance of the embedded host system (referred to here simply as "the system") using this LSI, based on rules stipulated in the Embedded Host Compliance Plan.

The Embedded Host Compliance Plan is arranged as shown below.

- Introduction (Summary)
  - Mandatory and optional items for achieving compliance
- Regulations
  - USB Certified Logo Qualification
  - Checklists
  - Target Peripheral List (TPL)
- Compliance Program
  - Test items
    - Test details are also given in the following documents:
      Embedded High-speed Host Electrical Test Procedure
      USB-IF Full and Low Speed Electrical and Interoperability Compliance Test Procedure
      Host High-Speed Electrical Test Procedure
      High-Speed Electrical Test Specifications
- Record Results
  - Test report items
- Target Peripheral List (TPL) Form
  - TPL items listed

4.1 Introduction (Summary)

Specifies the mandatory and optional items for achieving compliance. Details related to the LSI specifications are shown below.

4.1.1 Transfer Speed

Full support is not required for HS, FS, and LS. Table 4-1 lists the transfer speed combinations approved for host (downstream) ports.

This LSI supports HS and FS transfer speeds.

The system is allowed using either pattern B or C for selection of the supported devices.

Table 4-1 Transfer speed combinations

	LS	FS	HS
Pattern A	○	○	○
Pattern B	×	○	○
Pattern C	×	○	×
Pattern D	○	○	×
Pattern E	○	×	×

4.1.2 Transfer Type

Support for control transfer is mandatory. Support for other transfer types is optional.

In addition to control transfers, this LSI supports bulk and interrupt transfers.

The system can support storage devices and hubs.

4.1.3 USB Suspend

Support for USB Suspend is optional. However, support for Resume Signaling is mandatory if USB Suspend support is provided.

This LSI supports USB Suspend. For detailed information, refer to “2.6 Power Management” in the *S1R72U16 Technical Manual*.

The system can support USB Suspend when necessary.

4.1.4 VBUS Supply Current

The rules covering VBUS supply current are given below:

- The VBUS supply current for a Low-Power Embedded Host may be within the range of 8 mA to 100 mA.
- The VBUS supply current for a High-Power Embedded Host(※) must be at least 500 mA.
- In either case, sufficient power supply capacity is required to operate the supported devices specified in the TPL.

※: Embedded Host capable of providing current exceeding 100 mA.

This LSI includes functions for controlling the VBUS supply, but the supply current depends on the VBUS supply control circuit selected for the system.

The VBUS supply control circuit for the system should be designed based on the rules described above.

4.1.5 Target Peripheral List

An embedded host makes it possible to restrict the devices supported. The supported devices must be found on the Target Peripheral List (TPL) and submitted to the USB-IF to achieve compliance. The supported devices must be listed in accordance with the following rules:

- Devices must be listed as individual products, not just as class.
  - ➢ Individual products must be listed, even if support applies to a class.
- Only hubs may be listed as hub class devices.

An example TPL for submission is shown below.

Table 4-2 TPL

Manufacture	Model	VenderID	ProductID	Description	Transport (Bulk, Int, Isoch)	Speed
BUFFALO	RUF-C32ML	0x0EA0	0x6828	USB Memory	Bulk	FS
Maxtor	USB2120NEP001	0x0D49	0x3000	USB HDD	Bulk	HS
Hub Class	HUB	-	-	USB Hub	Int	FS/HS

The TPL must be retained as data within the system as well as submitted as a list.

By default, this LSI retains the Mass Storage Class Bulk Only Transport protocol and Hub class TPL data. TPL data can also be set using the download function. For detailed information on TPL data setting methods, refer to “2.8.4 TPL” in the *S1R72U16 Technical Manual*.

Submit the TPL to the USB-IF as a list when seeking to achieve compliance. Additionally, set TPL data in the LSI as necessary, regardless of compliance.

4.1.6 Hub Support

Hub support is optional.

By default, this LSI supports hubs and retains Hub class TPL data.

The system can support hubs without the need for additional TPL data setting in the LSI.

4.1.7 No Silent Failure (NSF)

A method for notifying the user of errors detected by the USB function is mandatory. This concept is known as No Silent Failure (NSF). However, specific wording or indication methods are not specified.

This LSI is capable of providing the following notification using the Port 14 to 17 pins. For detailed information on the NSF function, refer to "2.8.5 NSF" in the *S1R72U16 Technical Manual*.

- Unsupported Device
  - Occurs when an unsupported USB device is detected. May be checked via the Port 14 pin of the LSI.
- Too many Devices
  - Occurs when a third or subsequent storage device is detected. May be checked via the Port 15 pin of the LSI.
- Too many Hubs
  - Occurs when a fourth or subsequent USB hub is detected. May be checked via the Port 16 pin of the LSI.
- VBUS Over Current
  - Occurs when an overcurrent is detected in the VBUS. May be checked via the Port 17 pin of the LSI.

The system should provide a way to issue the notifications described above.

4.1.8 Implementation of Multiple Host (Downstream) Ports

Multiple host (downstream) ports may be implemented. However, in this case, the following rules apply.

- All downstream ports must be able to operate simultaneously and independently.
- All downstream ports must have the same supply current capacity to the VBUS.
- All downstream ports must support the same transfer speeds.
- All downstream ports must support the same devices.
- Mini-A receptacles must not be used.

This LSI supports one host (downstream) port.

The rules above do not apply if the system features only one host (downstream) port. They do apply if multiple host (downstream) ports are provided.

4.1.9 Implementation of Device (Upstream) Ports

Device (upstream) ports are optional. However, any device (upstream) ports must pass the USB Peripheral Compliance Test to achieve Embedded Host compliance.

This LSI does not support device (upstream) ports.

The rules above do not apply if the system lacks device (upstream) ports. They do apply if device (upstream) ports are provided.

4.2 Regulations

Embedded Host compliance requires the following regulations to be satisfied:

4.2.1 USB Certified Logo Qualification

The following rules apply to logos displayed by an Embedded Host system.

- Logos that can be displayed by an Embedded Host without device (upstream) ports
  - Host (downstream) port supports speeds up to HS: High-speed Version
  - Host (downstream) port supports speeds other than HS: Basic-speed Version
- Logos that can be displayed by an Embedded Host with device (upstream) ports
  - Device (upstream) port supports speeds up to HS: High-speed Version
    - Display High-speed Version even if host (downstream) port does not support speeds up to HS.
  - Device (upstream) port supports speeds other than HS: Basic-speed Version
    - Display Basic-speed Version Host even if host (downstream) port supports speeds up to HS.

The host (downstream) port is able to support speeds up to HS using this LSI. Note the rules given above. The logos that can be displayed depend on the user's system.

The system logo cannot be displayed unless compliance certification has been obtained.

4.2.2 Checklists

Submit the "USB Compliance Checklist for System" to the USB-IF to obtain certification for Embedded Host compliance. This checklist can be obtained from the site given below. For detailed information on the items that must be listed, contact the test lab responsible for performing the compliance testing.

http://www.usb.org/developers/compliance/systems_high/

4.2.3 Target Peripheral List (TPL)

The TPL must be submitted to the USB-IF to obtain certification for Embedded Host compliance. Table 4-2 gives the format. For detailed information on preparing and submitting the list, contact the test lab responsible for performing the compliance testing.

4.3 Compliance Program

Describes compliance testing specifics. Compliance test includes Electrical (to confirm compliance with electrical standards) and Interoperability (to confirm connectability). For detailed information on compliance testing of an Embedded Host system using this LSI, refer to "5. Embedded Host Compliance Test."

Refer also to the following documents provided by the USB-IF.

- *Embedded High-speed Host Electrical Test Procedure*
- *USB-IF Full and Low Speed Electrical and Interoperability Compliance Test Procedure*
- *Host High-Speed Electrical Test Procedure*
- *High-Speed Electrical Test Specification*

4.4 Record Results

Specifies the format for recording test results. Since compliance test results are recorded by the test lab, this is not an issue for users.

4.5 Target Peripheral List (TPL) Form

The information stipulated here is submitted to the test lab when undergoing compliance testing. Note that the test lab may use a different format based on this form. Contact the test lab performing compliance testing for details.

It is also currently being considered whether the submission of E.1 Host Information should also be required in addition to the TPL when obtaining Embedded Host compliance for the USB-IF. Customers should confirm the latest requirements with the test lab performing compliance testing.

5. Embedded Host Compliance Test

This compliance test stipulated in the Compliance Plan consists of an Electrical Test and an Interoperability Test. All items must be passed to achieve compliance for the embedded host system (referred to here simply as “the system”).

5.1 Electrical Test

This test confirms compliance with electrical standards. The procedures are described below, using the LSI’s USB logo certification support function for each test item.

5.1.1 Full-Speed Downstream Signal Quality

Measures the FS transmission wave eye pattern. This measurement is made if the system supports FS devices. Figure 5-1 shows the testing configuration.

- Measurement details
  - ➢ The downstream signal quality is measured at the Far End.
- Procedure
  1. Connect as shown in Figure 5-1.
  2. Select “USB analog test” on the control PC.
     - This allows switching to Test mode.
  3. Select “Host FS Signal Quality” on the control PC.
     - Switches to the mode used to issue a Get Device Descriptor request to the FS device.
  4. Select “Single Step” on the control PC.
     - A Get Device Descriptor request is issued only once, then FS SOF packet is issued continuously.
  5. The Downstream Signal Quality is measured by capturing the FS SOF packet on an oscilloscope.
  6. Select “Quit” on the control PC.
     - Exits test mode.
- Criteria
  - ➢ The USB Electrical Analysis Tool automatically determines whether the eye pattern falls within the acceptance criteria.

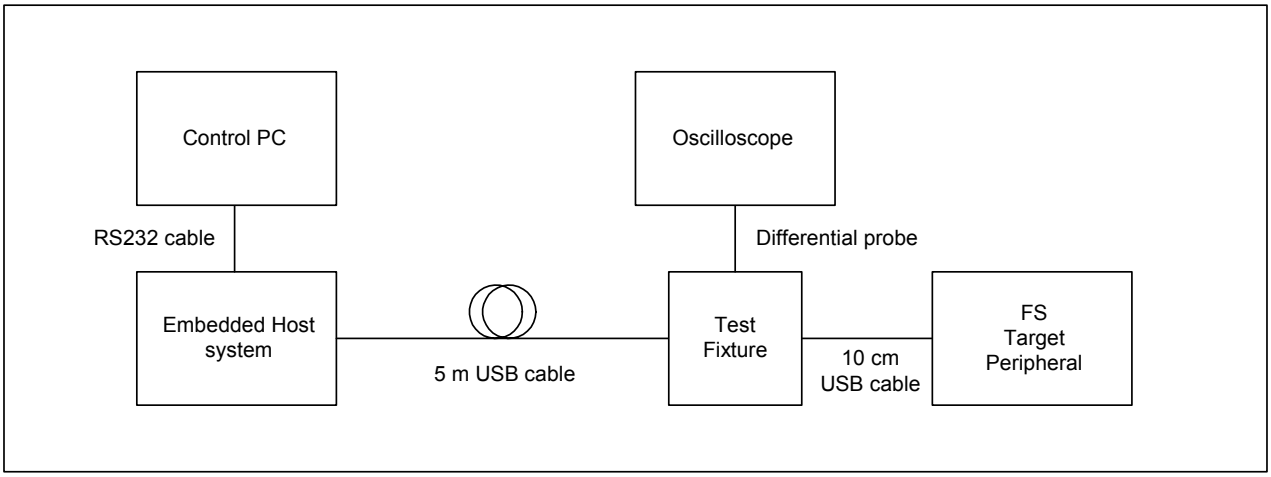

Figure 5-1 Full-speed downstream signal quality testing configuration

5.1.2 Low-Speed Downstream Signal Quality

Measures the LS transmission wave eye pattern. This measurement is made if the system supports LS devices. No discussion is provided here, since this LSI does not support LS.

5.1.3 Drop

This measures the voltage between VBUS and GND when a steady load is applied to the VBUS supplied by the system. Figure 5-2 shows the testing configuration.

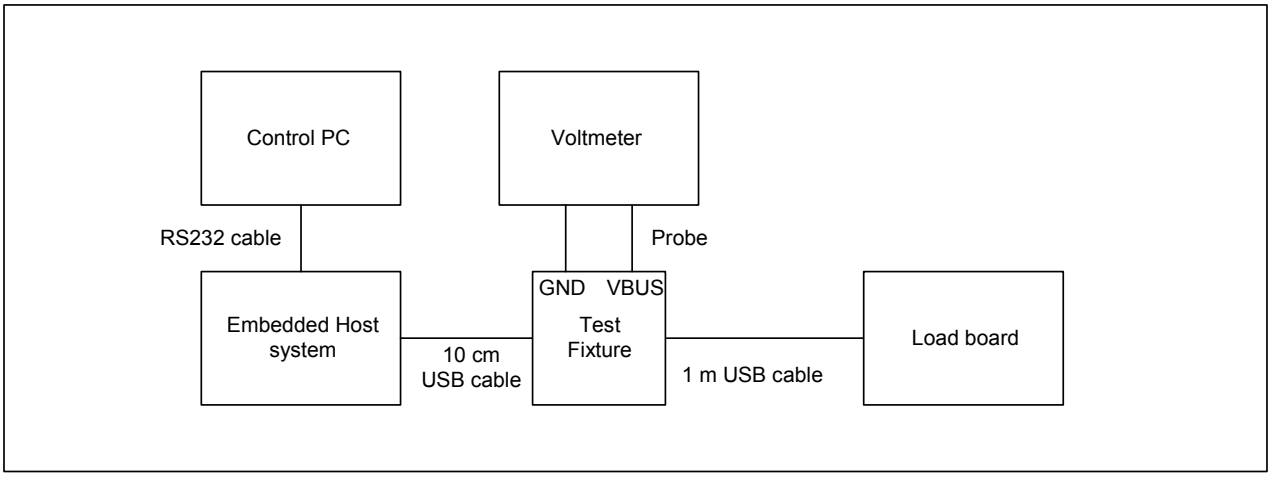

Figure 5-2 Drop testing configuration

5.1.3.1 High Power Embedded Host

This is measured if the system is a High-Power Embedded Host.

- Measurement details
  - The VBUS voltage is measured under no load.
  - The VBUS voltage is measured at a load of 500 mA.
- Procedure
  1. Connect as shown in Figure 5-2.
  2. Select “USB analog test” on the control PC.
     - This allows switching to Test mode.
  3. Select “Drop/Droop” on the control PC.
     - Power is supplied to the VBUS.
  4. Remove the load board. Measure the VBUS voltage using the voltmeter with the VBUS under no load.
  5. Add the load board. Measure the VBUS voltage using the voltmeter with the load set to 500 mA.
  6. Select “Quit” on the control PC.
     - Exits test mode.
- Criteria
  - The VBUS voltage must be within the range of 4.75 V to 5.25 V.

5.1.3.2 Low Power Embedded Host

This is measured if the system is a Low-Power Embedded Host.

- Measurement details
  - The VBUS voltage is measured at a load of 8 mA and at the maximum specification load.
  - Confirm that an indication is given in the form of LED illumination or a "VBUS Over Current" message if the VBUS voltage falls below 4.4 V.
- Procedure
  1. Connect as shown in Figure 5-2.
  2. Select "USB analog test" on the control PC.
     - This allows switching to Test mode.
  3. Select "Drop/Droop" on the control PC.
     - Power is supplied to the VBUS.
  4. Set the load board to a load of 8 mA. Measure the VBUS voltage using the voltmeter.
  5. Set the load board to the maximum system specification load. Measure the VBUS voltage using the voltmeter.
  6. Set the load board to a load of 100 mA. Measure the VBUS voltage using the voltmeter.
     - Confirm that an indication is given by the NSF function in the form of LED illumination or a "VBUS Over Current" message if the voltage falls below 4.4 V.
  7. Select "Quit" on the control PC.
     - Exits test mode.
- Criteria
  - The VBUS voltage must be within the range of 4.4 V to 5.25 V at a load of 8 mA and at the maximum specification load.
  - LED illumination or a "VBUS Over Current" message must be issued if the VBUS voltage falls below 4.4 V.

5.1.4 Droop

This is measured if the system has multiple downstream ports. The target port VBUS voltage drop is measured when a device is connected to a port other than the target port. This item is not discussed here, since this LSI has a single downstream port.

5.1.5 High-Speed Downstream Signal Quality (EL_2, EL_3, EL_6, EL_7)

Measures the HS transmission wave eye pattern. This measurement is made if the system supports HS devices. Figure 5-3 shows the testing configuration.

- Measurement details
  - ➢ The downstream signal quality is measured at the Near End.
- Procedure
  1. Connect as shown in Figure 5-3.
  2. Select “USB analog test” on the control PC.
     - This allows switching to Test mode.
  3. Select “Host HS Signal Quality” on the control PC.
     - Switches to the Test_Packet issuing mode and repeatedly issues Test_Packet.
  4. The Downstream Signal Quality is measured by capturing the Test_Packet on an oscilloscope.
  5. Select “Quit” on the control PC.
     - Exits test mode.
- Criteria
  - ➢ The USB Electrical Analysis Tool automatically determines whether the eye pattern falls within the acceptance criteria.

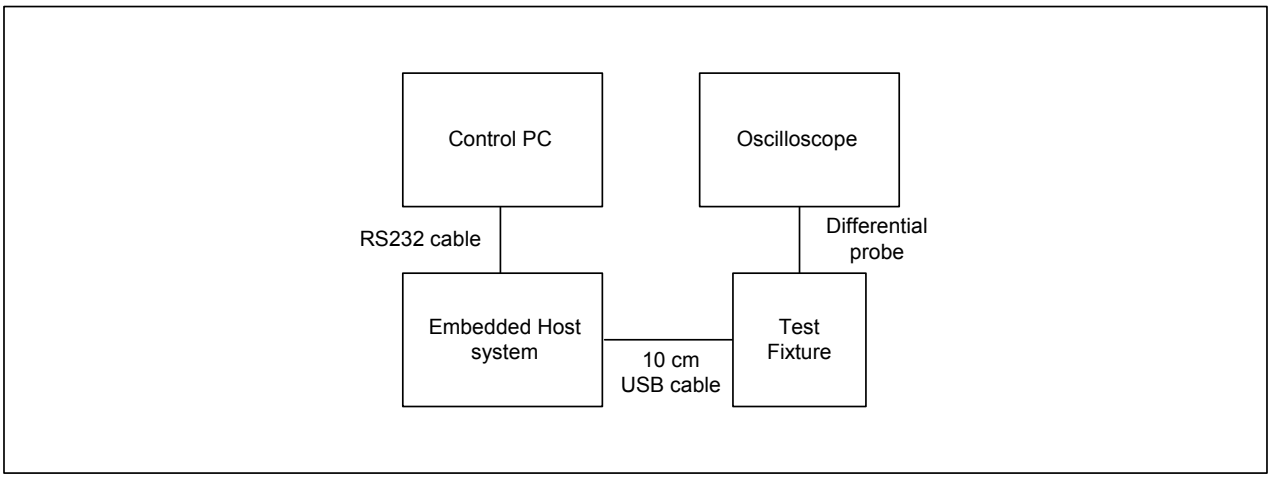

Figure 5-3 High-speed downstream signal quality testing configuration

5.1.6 Host Controller Packet Parameters (EL_21, EL_22, EL_23, EL_25, EL_55)

Measures HS transmission packet waveform timing. This measurement is made if the system supports HS devices. Figure 5-4 shows the testing configuration.

- Measurement details
  - Measures SETUP packet and transmission DATA packet 32-bit SYNC fields. (EL_21)
  - Measures the transmission DATA packet 8-bit EOP field. (EL_25)
  - Measures the interpacket gap for two continuous transmission packets. (EL_23)
  - Measures the interpacket gap for the packet received from the device and the packet sent by the system in response. (EL_22)
  - Measures the HS SOF packet 40-bit EOP field. (EL_55)
- Procedure
  1. Connect as shown in Figure 5-4.
  2. Select “USB analog test” on the control PC.
     - This allows switching to Test mode.
  3. Select “Single Step Get Descriptor test” on the control PC.
     - Switches to the mode for issuing Get Descriptor Test requests divided into individual stages (Setup/Data/Status).
     - Pressing the “Return” key runs Setup stage.
  4. Measure EL_21, EL_25, and EL_23 by capturing the Setup stage packets on an oscilloscope.
  5. Press the “Return” key again.
     - Runs the Data stage.
  6. Measure EL_22 by capturing the Data stage packets on an oscilloscope.
  7. Press the “Return” key again.
     - Runs the Status stage. Only HS SOF packets are issued continuously thereafter.
  8. Measure EL_55 by capturing the HS SOF packets on an oscilloscope.
  9. Select “Quit” on the control PC.
     - Exits test mode.

- Criteria
  - 31 bit < EL_21 < 33 bit
  - 7 bit < EL_25 < 9 bit
  - 88 bit ≤ EL_23 < 192 bit
  - 8 bit ≤ EL_22 < 192 bit
  - 39 bit < EL_55 < 41 bit

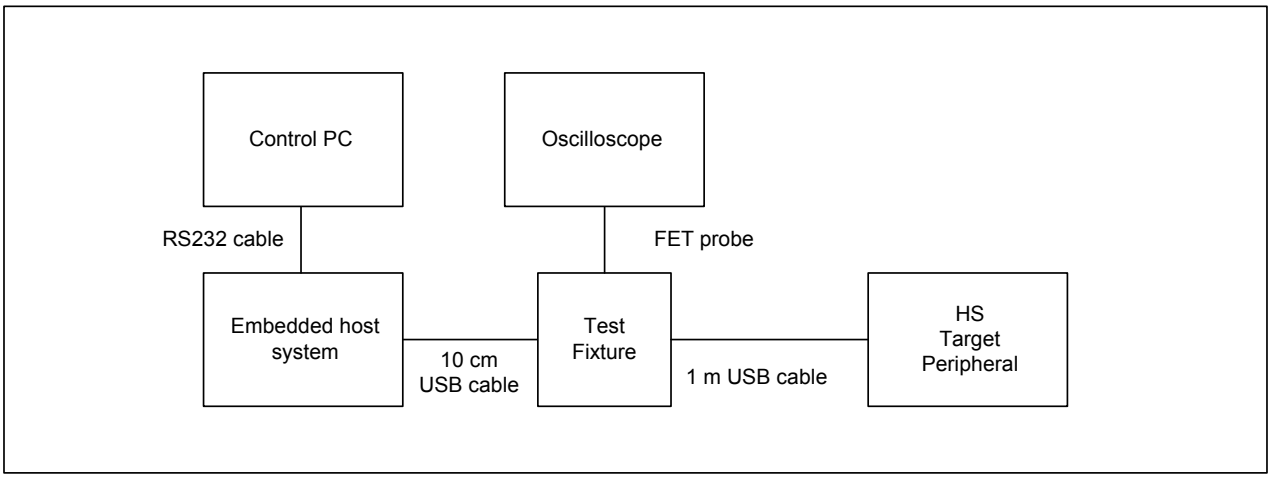

Figure 5-4 Host controller packet parameter testing configuration

5.1.7 Host Chirp Timing (EL_33, EL_34, EL_35)

Measures HS chirp timing. This measurement is made if the system supports HS devices. Figure 5-5 shows the testing configuration.

- Measurement details
  - The interval measured is from the end of the device chirp K to the start of the system chirp. (EL_33)
  - Times are measured for the chirp K and J issued by the system. (EL_23)
  - The interval measured is from the end of the chirp issued by the system until the first HS SOF packet is issued. (EL_35)
- Procedure
  1. Connect as shown in Figure 5-5.
  2. Select “USB analog test” on the control PC.
     - This allows switching to Test mode.
  3. Select “Host CHIRP Timing” on the control PC.
     - Switches to the mode for executing USB Reset.
     - Press the “Return” key to execute a USB Reset. The system will issue a chirp in response to the device chirp.
  4. Measure EL_33 and EL_34 by capturing on an oscilloscope the point at which the device stops chirping and the system starts chirping.
  5. Select “Quit” on the control PC.
     - Exits test mode.
  6. Select “Host CHIRP Timing” on the control PC.
     - Switches to the mode for executing USB Reset.
     - Press the “Return” key to execute a USB Reset. The system will issue a chirp in response to the device chirp.
  7. Measure EL_35 by capturing on an oscilloscope the point at which the system issues the first SOF packet after chirping ends.
  8. Select “Quit” on the control PC.
     - Exits test mode.
- Criteria
  - EL_33 < 100 us
  - 40 us ≤ EL_34 ≤ 60 us

- 100 us < EL_35 ≤ 500 us

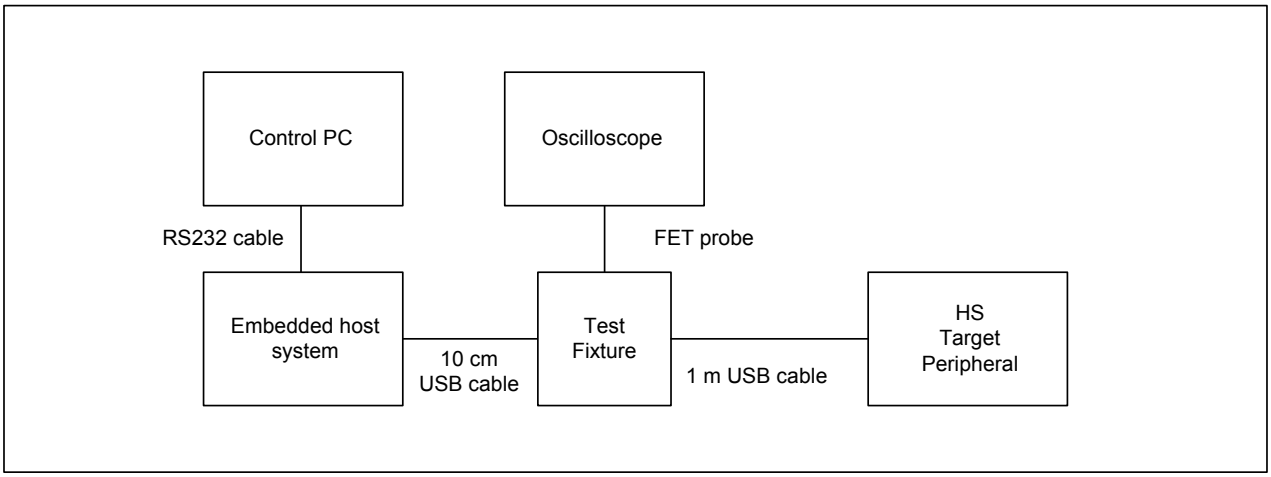

Figure 5-5 Host chirp timing testing configuration

5.1.8 Host Suspend/Resume (EL_39, EL_41)

Measured if the system supports HS devices and USB Suspend. Measures USB Suspend and USB Resume timing. Figure 5-6 shows the testing configuration.

- Measurement details
  - Checks whether the system is able to switch a device to, and maintain, the Suspend state. (EL_39)
  - The interval measured is from the end of the USB Resume issued by the system until the first SOF packet is issued. (EL_41)
- Procedure
  1. Connect as shown in Figure 5-6.
  2. Select “USB analog test” on the control PC.
     - This allows switching to Test mode.
  3. Select “Host Suspend/Resume Timing” on the control PC.
     - Switches to the mode for executing USB Suspend/Resume.
     - Press the “Return” key to execute a USB Suspend.
  4. Measure EL_39 by capturing on an oscilloscope the point at which the system stops issuing an SOF packet and the device switches to Suspend. Measures the interval from the last SOF packet issued to the FS J_State (Suspend), which depends on the specific device. The time measured indicates whether devices switch correctly to Suspend. The results report indicates only “Pass” or “Fail.”
  5. Press the “Return” key again.
     - A USB Resume is issued. HS SOF packets are issued continuously after completion of the USB Resume.
  6. Measure EL_41 by capturing on an oscilloscope the point at which the system stops issuing the USB Resume and issues the first HS SOF packet.
  7. Select “Quit” on the control PC.
     - Exits test mode.
- Criteria
  - EL_39: Suspend state (FS J_state) is measurable
  - EL_41 ≤ 3 ms

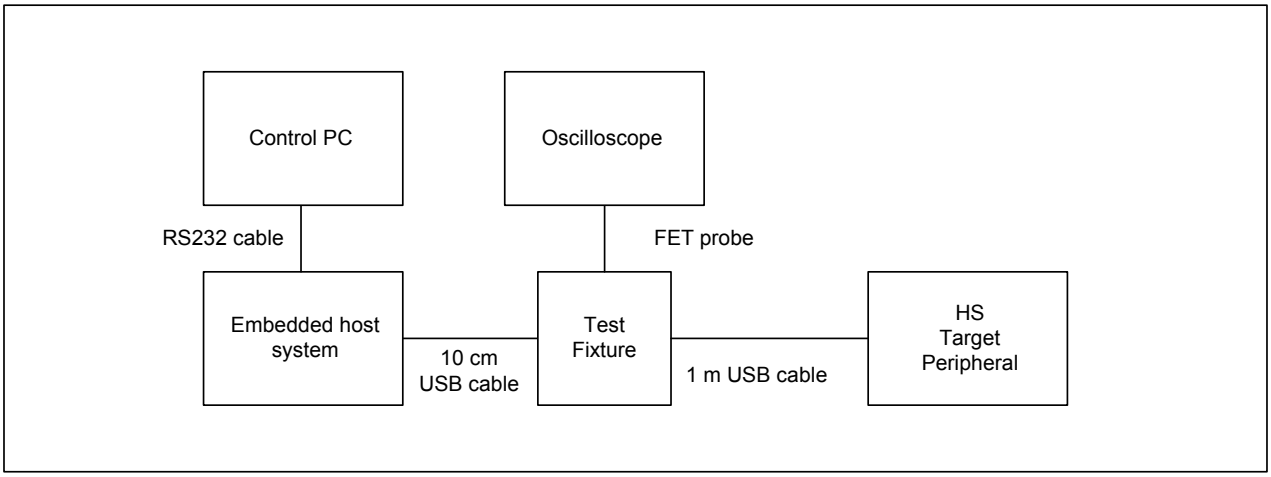

Figure 5-6 Host Suspend/Resume testing configuration

5.1.9 Host Test_J/K, SE0_NAK (EL_8, EL_9)

Measures the HS driver DC drive capacity. This measurement is made if the system supports HS devices. Figure 5-7 shows the testing configuration.

- Measurement details
  - Measures voltage between DP and GND and between DM and GND while the system is in HS J_state drive. (EL_8, EL_9)
  - Measures voltage between DP and GND and between DM and GND while the system is in HS K_state drive. (EL_8, EL_9)
  - Measures voltage between DP and GND and between DM and GND while the system is in HS SE0_state drive. (EL_8, EL_9)
- Procedure
  1. Connect as shown in Figure 5-7.
  2. Select “USB analog test” on the control PC.
     - This allows switching to Test mode.
  3. Select “Host Test_J/K, SE0_NAK” on the control PC.
     - Switches to the mode for executing Host Test_J/K, SE0_NAK.
  4. Select “Test J” and press the “Return” key.
     - Starts HS J_state drive.
  5. Measure the voltage between DP and GND and between DM and GND. (EL_8, EL_9)
  6. Press the “Return” key.
     - Stops the HS J_state drive.
  7. Select “Test K” and press the “Return” key.
     - Starts HS K_state drive.
  8. Measure the voltage between DP and GND and between DM and GND. (EL_8, EL_9)
  9. Press the “Return” key.
     - Stops the HS K_state drive.
  10. Select “Test SE0_NAK” and press the “Return” key.
      - Starts HS SE0_state drive.
  11. Measure the voltage between DP and GND and between DM and GND. (EL_8, EL_9)

12. Press the “Return” key.
    - Stops the HS SE0_state drive.
13. Select “Quit” on the control PC.
    - Exits test mode.

- Criteria
  - Test_J : 360 mV ≤ DP ≤ 440 mV, -10 mV ≤ DM ≤ 10 mV
  - Test_K : -10 mV ≤ DP ≤ 10 mV, 360 mV ≤ DM ≤ 440 mV
  - Test_SE0 : -10 mV ≤ DP ≤ 10 mV, -10 mV ≤ DM ≤ 10 mV

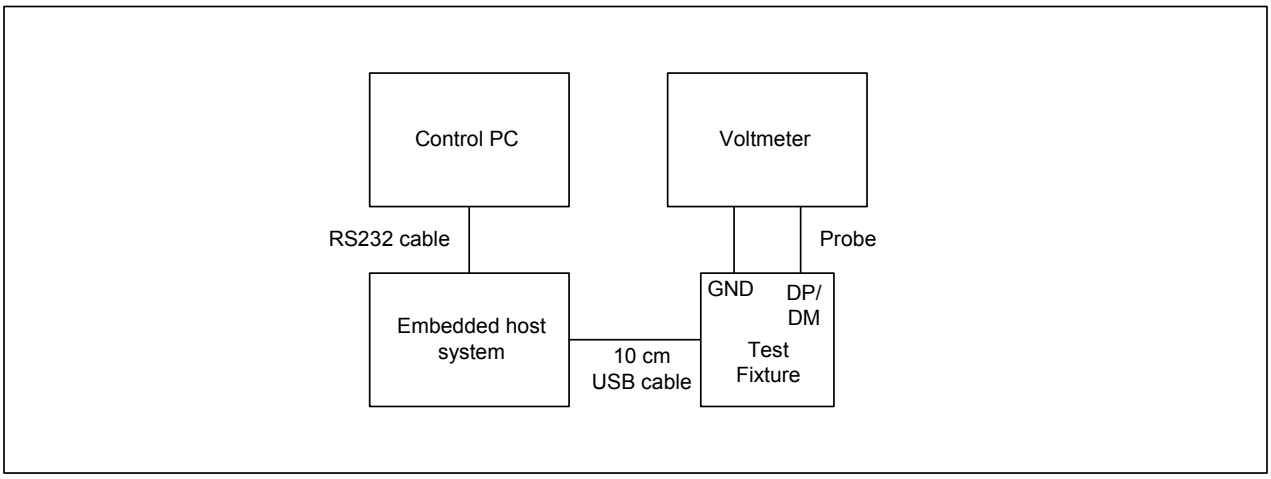

Figure 5-7 Host Test_J/K, SE0_NAK testing configuration

5.2 Interoperability Test

This test checks connectability with all supported devices provided to the test lab. The system must run in the mode in which it will actually be used once released on the market, not in test mode.

5.2.1 Enumeration

Confirms correct function of the system Enumeration and Operation. Test specifics are described below.

a. A-plug Attach Test

Confirms that the system functions correctly when the USB cable is connected to the system with the supported device already connected to the USB cable.

b. B-plug Attach Test

Confirms that the system functions correctly when the USB cable is connected to the supported device with the USB cable already connected to the system.

The test is omitted for supported devices that have non-detachable cables or do not use cables.

c. Power-on Host Test

Confirms that the system functions correctly when the system power is turned on after connecting a supported device to the system with power turned off.

d. Reset Host Test

Confirms that the system functions correctly after resetting the system with a supported device connected.

e. Power-on Peripheral Test

Confirms that the system functions correctly after power is turned on for a supported device after connecting the supported device to the system with power turned off.

f. Dynamic Attach Test

Confirms that the system functions correctly when a supported device is disconnected, then reconnected, after initially connecting the supported device to the system and completing Enumeration.

g. Topology Change Test (Option)

This test applies to systems with at least two host (downstream) ports. Confirms that the system functions correctly when a supported device is connected to a different port.

This test is omitted for systems with only one host (downstream) port.

5.2.2 Operation

Confirms that the system functions correctly in accordance with specifications. Test specifics are described below.

a. Peripheral Operation Test

Confirms that the system can control supported devices in accordance with specifications.

b. Host Suspend/Resume Test (Option)

This test applies only when the system supports USB Suspend. The test confirms that the system can control supported devices in accordance with specifications after executing a USB Suspend followed by a USB Resume with a supported device connected to the system.

This test is omitted for systems that do not support USB Suspend.

c. Suspend-Disconnect Test (Option)

This test applies only when the system supports USB Suspend. The test confirms that the system does not malfunction (e.g., by executing a USB Resume) when a supported device is disconnected from the system after executing a USB Suspend with the supported device connected to the system.

This test is omitted for systems that do not support USB Suspend.

d. Suspend-Attach Test (Option)

This test applies only when the system supports USB Suspend. The test confirms that the system can control supported devices in accordance with specifications when the system executes a USB Resume after disconnecting, then reconnecting the supported device in the **c. Suspend-Disconnect Test**.

This test is omitted for systems that do not support USB Suspend.

e. Peripheral remote wakeup Test (Option)

This test applies only when the system supports USB Suspend and remote-wakeup. The test confirms that the system can control supported devices in accordance with specifications when the supported device executes a USB Resume after executing a USB Suspend with the supported device connected to the system.

This test is omitted for systems that use this LSI, since the LSI does not support remote-wakeup.

f. Topology Change Test (Option)

This test applies only for systems with at least two host (downstream) ports and that support USB Suspend. The test confirms that the system can control supported devices in accordance with specifications when the system executes a USB Resume after disconnecting the supported device in the **c. Suspend-Disconnect Test**, then reconnecting to a different system port.

This test is omitted for systems that have only one host (downstream) port or that do not support USB Suspend.

g. Concurrent Downstream Operation (Option)

This test applies only for systems with at least two host (downstream) ports. Confirms that the system can control supported devices connected to all ports simultaneously and independently.

This test is omitted for systems that have only one host (downstream) port.

5.2.3 Hubs

The test details are as shown below if the system supports hubs. These tests apply to this LSI, since it supports hubs.

a. Maximum Tier Test

If the number of tiers supported is five or less, this test confirms that a notification in the form of messages or LED indication is given by the NSF function when the hub connected exceeds the number of tiers supported. The test method consists of connecting a 5-tier hub to produce a message, then gradually reducing the number of tiers to check that the message or LED indication is no longer given within the number of tiers supported.

The NSF function on this LSI issues a “Too Many Hubs” indication if a 5- or 4-tier hub is connected.

b. Peripheral Operation Test

Confirms that the system can control supported devices in accordance with specifications when a supported device is connected to a hub representing the maximum supported number of tiers. The test is conducted for this LSI by connecting a supported device to the third-tier hub.

5.2.4 Messaging (No Silent Failure)

This test checks that message or LED indications are provided by the NSF function. The test details are as shown below.

a. Unsupported Device Message

Confirms that message or LED indications are issued to indicate a lack of support when an unsupported device is connected to the system.

In this case, the NSF function on this LSI issues an “Unsupported Device” indication.

b. Message (Option) for Non-support of Hubs

Confirms that message or LED indications are issued to indicate a lack of support for hubs when the hub connected to the system does not support hubs. Ideally, this should be distinct from the indication given for “Unsupported Device.”

This item does not apply to this LSI, since it supports hubs.

6. Independent Test Labs

For detailed information on test labs, refer to the following site.

http://www.usb.org/developers/compliance/labs/

Revision History

Date	Revision details			
	Rev.	Page	Type	Details
06/01/2007	0.79	All	New	Newly established
07/01/2007	1.00	4.1.5	Correct	Added “Transport” column in Table 4-2 TPL.
		4.5	Correct	Added information regarding E.1 Host Information
		5.1.1	Correct	Changed “Single” to “Single Step”.
			Correct	Changed “Captive USB cable” to “10 cm USB cable” in Figure 5-1.
		5.1.3	Correct	Changed “Captive USB cable” to “10 cm USB cable” in Figure 5-2.
		5.1.5	Correct	Changed “Test_Packet packet” to “Test_Packet”.
			Correct	Changed “Captive USB cable” to “10 cm USB cable” in Figure 5-3.
		5.1.6	Correct	Changed “Get Descriptor Test request” to “Get Descriptor request”.
			Correct	Changed “Captive USB cable” to “10 cm USB cable” in Figure 5-4.
		5.1.7	Correct	Changed steps 5 to 8.
			Correct	Changed “500 bit” to “500 us”.
			Correct	Changed “Captive USB cable” to “10 cm USB cable” in Figure 5-5.
			Correct	Changed “Differential probe” to “FET probe” in Figure 5-5.
		5.1.8	Correct	Changed “Resum” to “Resume”.
			Correct	Changed “Captive USB cable” to “10 cm USB cable” in Figure 5-6.
			Correct	Changed “Differential probe” to “FET probe” in Figure 5-6.
		5.1.9	Correct	Changed “Test_J” to “Test J”.
			Correct	Changed “Test_K” to “Test K”.
			Correct	Changed “Test_SE0_NAK” to “Test SE0_NAK”.
			Correct	Changed “Captive USB cable” to “10 cm USB cable” in Figure 5-7.

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