Hardware Design in the 21st Century with the Object-Oriented and Functional Language Chisel

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This is a proposal for a tutorial at DATE 2020 on Chisel. It will include hands-on lab exercises with FPGA boards.

Title: Hardware Design in the 21st Century with the Object Oriented and Functional Language Chisel

Organizer(s): Martin Schoeberl, Technical University of Denmark, masca@dtu.dk

Reference person: Martin Schoeberl, Technical University of Denmark, masca@dtu.dk

Speaker(s): Martin Schoeberl, Technical University of Denmark, masca@dtu.dk

Preferred slot: PM

DATE Track / Topic reference: Track D: Design Methods and Tools

Motivation: To develop future more complex digital circuits in less time we need a better hardware description language than VHDL or Verilog. Chisel is a hardware construction language intended to speed up the development of digital hardware and hardware generators.

Intended audience: Hardware designers with a background on VHDL or Verilog, but also software developers interested to learn hardware design with an object-oriented language.

Objectives: Learn to describe simple circuits in Chisel, write test benches to test them, and implement them in an FPGA.

Abstract: Chisel is a hardware construction language implemented as a domain specific language in Scala. Therefore, the full power of a modern programming language is available to describe hardware and, more important, hardware generators. Chisel has been developed at UC Berkeley and successfully used for several tape outs of RISC-V. Google has developed a tensor processing unit for edge devices in Chisel. Here at the Technical University of Denmark we use Chisel in the T-CREST project and in teaching advanced computer architecture.

In this tutorial I will give an overview of Chisel to describe circuits at the RTL level, how to use the Chisel tester functionality to test and simulate digital circuits, present how to synthesize circuits for an FPGA, and present advanced functionality of Chisel for the description of circuit generators.

The aim of the course is to get a basic understanding of a modern hardware description language and be able to describe simple circuits in Chisel. This course will give a basis to explore more advanced concepts of circuit generators written in Chisel/Scala. The intended audience is hardware designers with some background in VHDL or Verilog, but Chisel is also a good entry language for software programmers entering into hardware design (e.g., porting software algorithms to FPGAs for speedup).

Besides lecturing we will have lab sessions to describe small circuits, test them in the Chisel simulation, and run them in an FPGA.

Necessary background: Knowledge of a hardware description language like VHDL of Verilog is beneficial, but Chisel is also approachable by software engineers with knowledge of an object-oriented language such as Java or C#.

References:

- Jonathan Bachrach, jackbackrack@gmail.com, Initial designer of Chisel (UC Berkeley)
- Thomas Preusser, thomas.preusser@xilinx.com, Tutorial Chair FPL 2018
- Charles Lo, University Of Toronto, locharl1@ece.utoronto.ca, participant of FPL 2018 Chisel tutorial

Has the same tutorial (or a similar one) been presented to other events (if yes, list when/where)? I have given this tutorial (or a variation of it) several times: in a two day format at University of Augsburg (about 10 attendees), several years in a course in advanced computer architecture at DTU (about 10 attendees), at DTU with industrial attendees (two half days), at the Danish engineering society (very short form, afternoon), at FPL 2018 one day tutorial (22 attendees), at FPL 2019 one day tutorial, at ESWEEK 2019 one day tutorial.

Has the same organizer proposed other tutorials (if yes, list when/where and on what topic)? No.

Tutorial material: I will provide a VM with all tools installed for download and with an USB stick. Furthermore, I will provide FPGA boards for the hands-on lab exercises.

The book "Digital Design with Chisel" accompanies the tutorial. It is available in open access.[1]

Tutorial plan: 13:30 Start of Tutorial (and Conference) Registration
13:30-14:00 Tutorial Welcome Coffee
14:00-15:30 Tutorials
14:00 - 14:45 Chisel overview
14:45 - 15:30 Chisel basic operations
15:30-16:00 Afternoon coffee break
16:00-18:00 Tutorials
16:00 - 17:00 A little bit of Scala and Chisel background
17:00 - 18:00 Customized circuit generation
18:00 - 21:00 DATE Welcome Reception & PhD Forum

Further Information

List of organizers and speakers: Assoc. Prof. Martin Schoeberl, Technical University of Denmark.

Martin Schoeberl received his PhD from the Vienna University of Technology in 2005. From 2005 to 2010 he has been Assistant Professor at the Institute of Computer Engineering. He is now Associate Professor at the Technical University of Denmark. His research interest is on hard real-time systems, time-predictable computer architecture, and real-time Java. Martin Schoeberl has been involved in a number of national and international research projects: JEOPARD, CJ4ES, T-CREST, RTEMP, the TACLe COST action, and PREDICT. He has been the technical lead of the EC funded project T-CREST. He has more then 100 publications in peer reviewed journals, conferences, and books.

Martin has been four times at UC Berkeley on three months research stays, where he has picked up Chisel and is in close contact with the developers of Chisel. He lead the research project T-CREST where most of the components have been written in Chisel.

Topics: Hardware design in a modern hardware construction language, object oriented and functional description of hardware, circuit generators.

Format: The tutorial will be a mix of lectures and hands-on labs. Participants shall have a laptop and I will provide instructions for software installation beforehand. Furthermore, at the tutorial I will provide USB sticks with virtual machine where all software is installed and a few FPGA boards for a hands-on real hardware experience.

[1] https://github.com/schoeberl/chisel-book