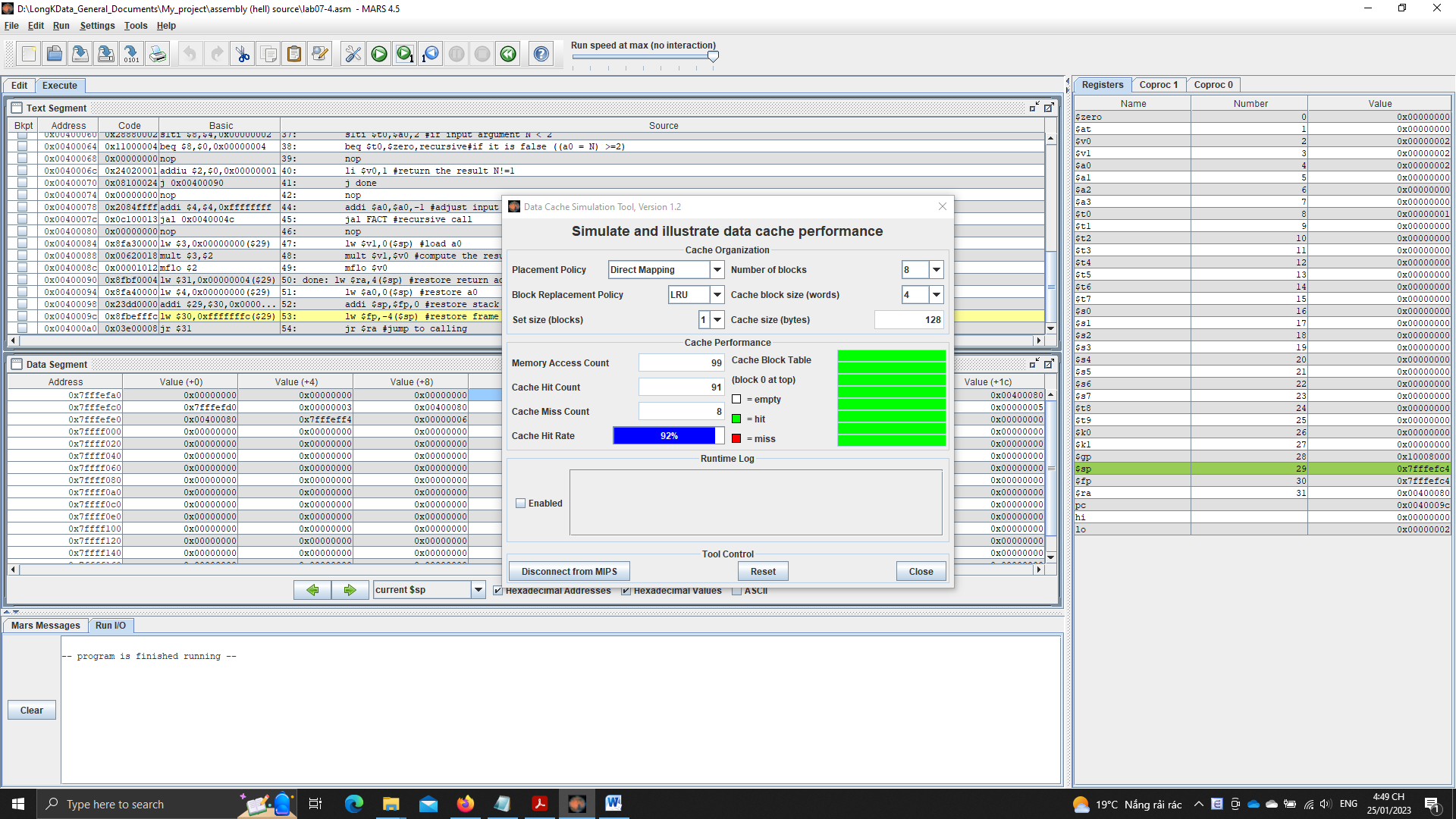
Lab Report 12

## Assignment 1:



## Assignment 2:

* A full 32-bit address in cache memory is used in some principles:
  + The least significant bits of the address are used to specify the byte within the block.
  + The next set of bits are used to specify the block number within the cache.
  + The remaining bits, known as the tag, are used to identify the main memory location of the block.
* When there is a cache miss, the processor must access the main memory to retrieve the requested data.
* When there is a cache hit, the processor can access the requested data from the cache, which is much faster than accessing the main memory.
* The block size is 4 words ~ 16 bytes.
* The tag is used to identify the main memory location of the block stored in the cache.

## Assignment 3:

* Answer the questions:
  + Cache size: total size of the cache (128 bytes)
  + Block size: size of each cache line (4 words = 16 bytes)
  + Set size: size of each set (apply for set associative placement policies) (1 block – no set split)
  + Write policy: the policy to determine which memory block should be placed in the cache (Direct, fully associative…)
  + Replacement policy: the policy to determine which cache line should be replaced when the cache is full (LRU, LFU, random, FIFO…)
* In the worst case, it is the number of iterations multiplies with number of memory requests (store/load). In best case, only number of memory requests of 1 loop.
* Some optimization ways:
  + Not use stack and recursion, since it will make a greater number of new calls that increase cache miss rate.
  + Use loop + store the temporary results (factorial computation temporary results, the respective n number (n <= N)) and initial results (results with base case N = 1, N = 0) in registers to store computation results to reduce requests to cache.