Project Ideas

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Types of Projects

DSLs and high-level libraries

Better programming models (magma++)

Compiler infrastructure (coreir, rigel)

Fast place and route

Debug and test

DSLs

Compile domain-specific languages to hardware

- Signal and image processing (Darkroom, Rigel)
- Finite-state machines
  - co-routines
  - waveforms to fsms
- Monte-Carlo and Metropolis-Hastings
- Deep learning and CNNs
- Processor DSL

Magma++

Experiment with programming models ...

Backends

- **Better mantle40 backend**
- **Altera port**

Full collection of peripherals

`logi2magma`

Coarse-Grain Recon Array (CGRA) overlay

Intermediate Repr

Implementing generators and optimization pass in `coreir/rigel`

Interface to `magma` **and** `FIRRTL`

Retiming

Optimal packing into LUT

Fast code generation (patch bitstream)

Incremental compiling and linking

Place and Route

DSLs with embedded PNR

- **Optimized placements of standard primitives**

Layout engine ala HTML Rendering

Support for location constraints in `arachne-pnr`

Programmed routing

Work on `SMT-PNR`

Debug and Test

Make it easier to display internal state

- **Connect internal state to J3 ...**

Automatic generation of unit tests

- **Compare to FPGA code to simulation**

Source-level debugger

- **Waveform viewers**

Floor planner