Lab Report 6: Edge-Triggered Flip-Flop

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Abstract

A Flip-Flop is a circuit device that has two stable states, in which information can be stored. This circuit can be triggered to change its state by applying one or more control inputs. For this reason, the Flip-Flop is a basic storage element, used in many sequential circuits. In this laboratory report, the design, layout and simulation of an Edge-Triggered D-Flip-Flop is created in Cadence Virtuoso Layout and Cadence Virtuoso Schematic Editor.

1 Initial Simulation and Results

The design for this experiment's Edge-Triggered D-Flip-Flop (DFF) is composed of standard gates: Inverter, 2-input NAND and 3-input NAND. Since the data can only be stored on a rising clock tick, the equation for the DFF is:

$$Q = \begin{cases} 1, & \text{Data if rising edge of Clock.} \\ 0, & \text{else keep previous data} \end{cases} \tag{1}$$

2 DFF's Device Characteristics

3 Layout Design and Physical Verification

4 Discussion and Conclusion