Lab Report 5: Design 2-to-1 Mux

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ECEC 471: Introduction to VLSI

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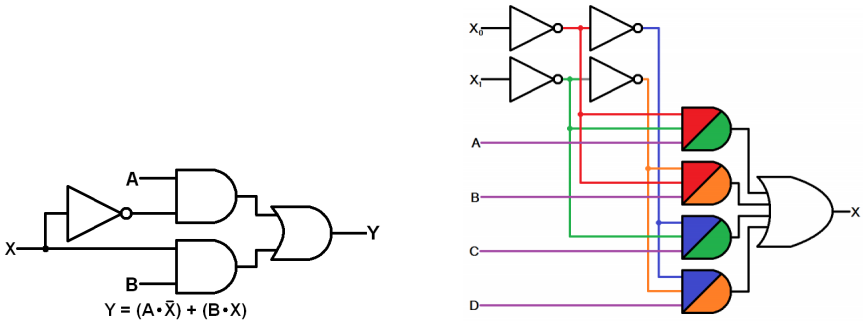
Abstract

A multiplexer (mux) is a common component used in many circuits. A mux is used when multiple data lines (input $a_1, a_2, ..., a_n$) share a single data line (output q), and the select bits (sel) are used to determine which inputs are chosen to connect to the output. In this laboratory, the schematic and layout design of the 2-to-1 mux (will only be refered as mux in the future) will be determined using Cadence Virtuoso and verified through tools such as DRC and LVS in the Cadence Interactive Toolbox.

1 Introduction

Multiplexer is a basic component which is mainly used as control gate in complex digital circuits. This lab's mux is comprised of 3 NAND logic gate and 1 inverter (INV) connected together and shown in Figure 1a below. As the number of input lines (N) increases, the number of select bits increase ($S = ceil(log_2(n))$). A 4-to-1 multiplexer will look like Figure 1b.



(a) 2-to-1 mux (b) 4-to-1 mux

Figure 1: Logic gate layout of multiplexers (https://learn.sparkfun.com/tutorials/logicblocks-experiment-guide/7-2-to-1-multiplexer)

2 Schematic Design

The following Figure 2 is the result of the mux layout in Cadence Virtuoso. The connections between the logic gates are similar to that of Figure 1a. The individual NAND gates and inverters are imported from previously symmetrically built components.

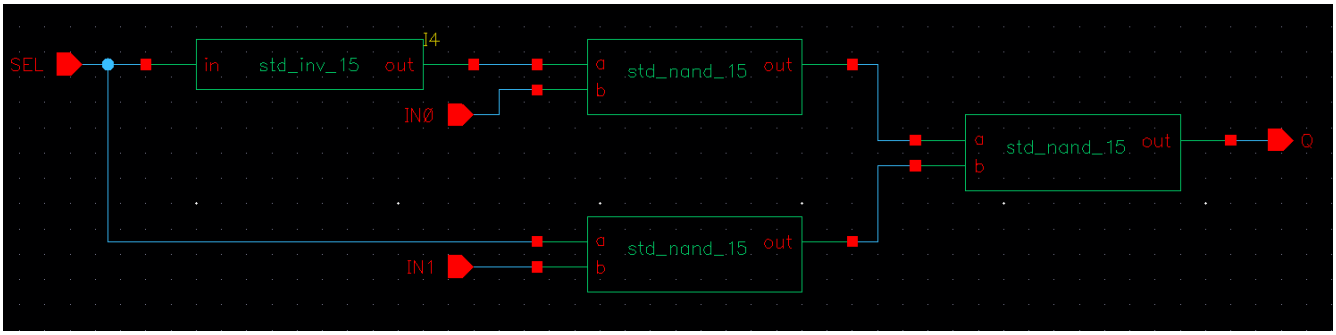


Figure 2: 2-to-1 mux's schematic layout

After the schematic is laid out, the symbol for the mux is created and the entire inner working of the circuitry is simulated with the layout in Figure 3 below.

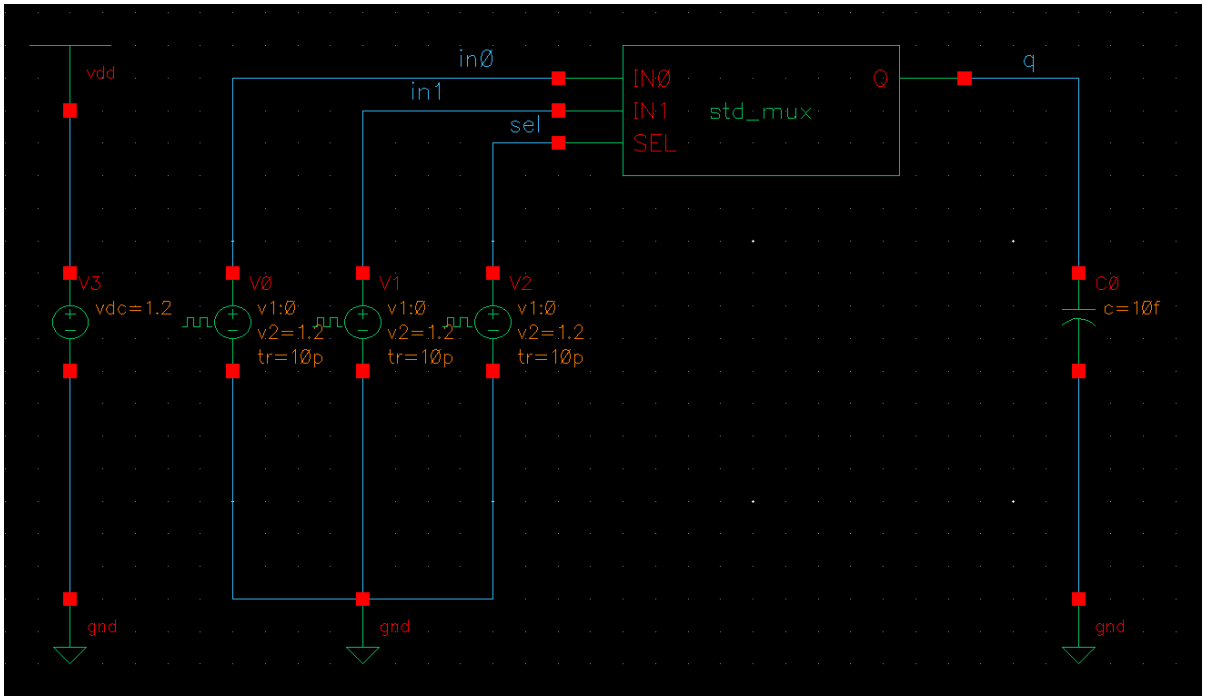


Figure 3: 2-to-1 mux's simulation layout

3 Schematic Simulation and Results

This section documents the simulation steps and their results. First, table 1 below shows the combinations of the inputs and their respective output values of the mux

IN0	IN1	SEL	Q
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0

Table 1: 2-to-1 mux's table of input to output combinations

From the simulation layout above, the transient analysis of this mux can be performed using ADE(L) simulation tool. The graph of this analysis is shown in Figure 4. Derived from the figure is the information of different delays, rise, and fall time characteristics.

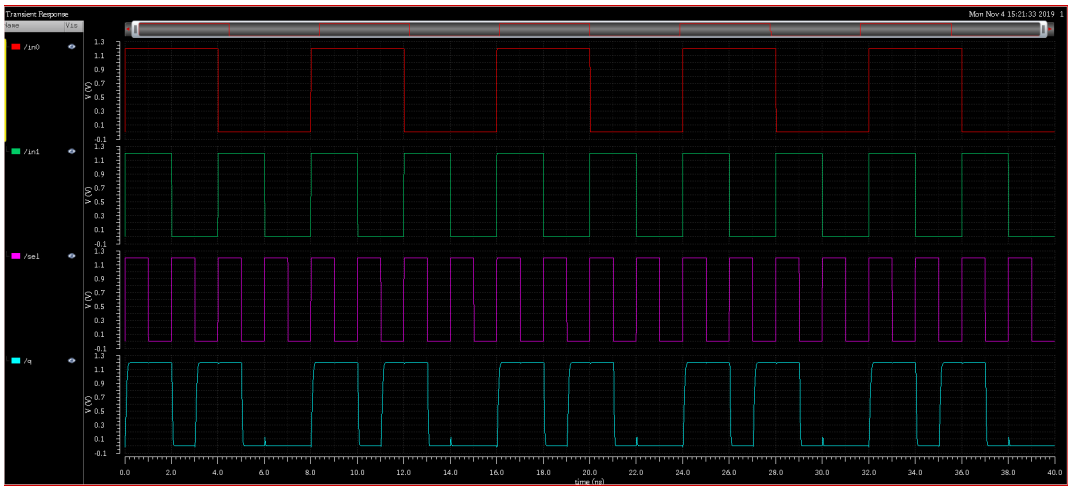


Figure 4: 2-to-1 mux's ADE(L) simulated transient plot

Since there are 4 cases - 4 different combinations of inputs, the delays for each case are calculated and documents in table 2.

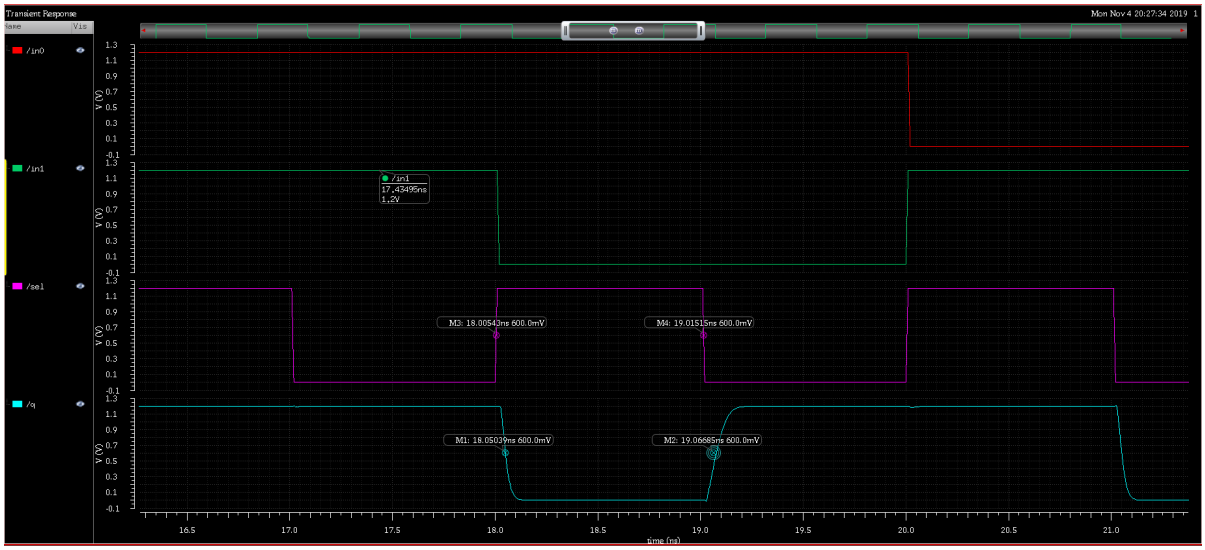
IN0	IN1	SEL	Q	Delay
0	1	0	0	0.03421
0	1	1	1	0.06057
1	0	0	1	0.05170
1	0	1	0	0.04496

Table 2: 2-to-1 mux's table of input to output combinations with their respective delays

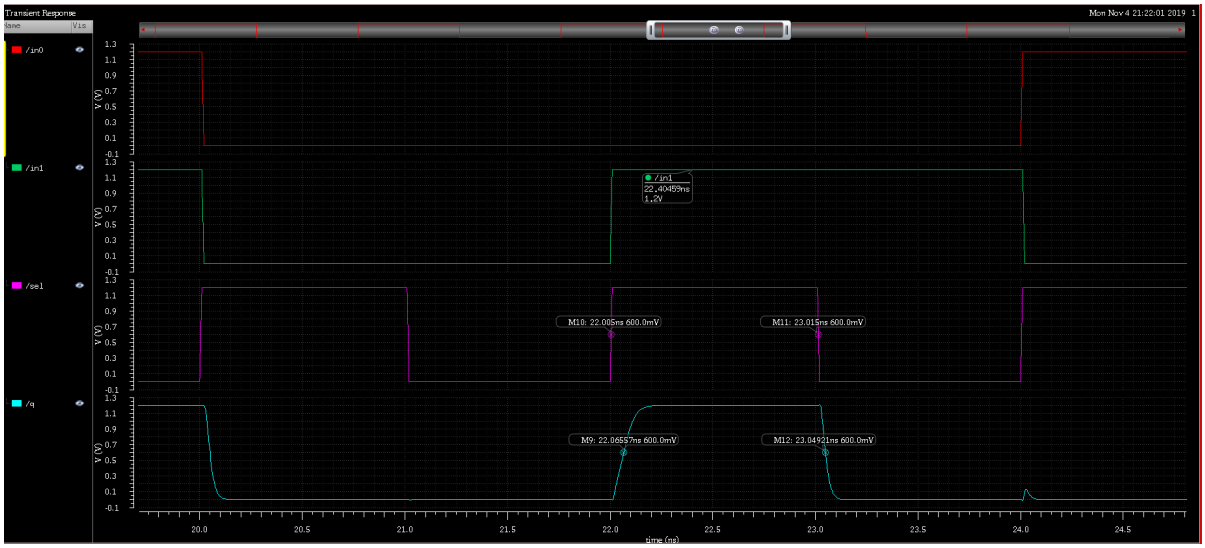
These calculations result from generating 2 configurations of the simulation schematic. In the first configuration, the IN1 has a delay of 0ns, and in the second configuration, the IN1 has a delay of 2ns (Figure 5a & 5b).

It is clear that the propagation rising and falling delays of the 2 cases are not equal. Hence, the worst-case propagation delay is the average of the worst-case rising propagation delay and the worst-case falling propagation delay. According to table 2, $t_{pdrworst} = 0.06057$, $t_{pdfworst} = 0.04496$, and $t_{pd} = \frac{0.06057+0.04496}{2} = 0.052765$.

In addition, the rise time and fall time of the mux can also be extracted from the simulation in Figure 6a & 6b.



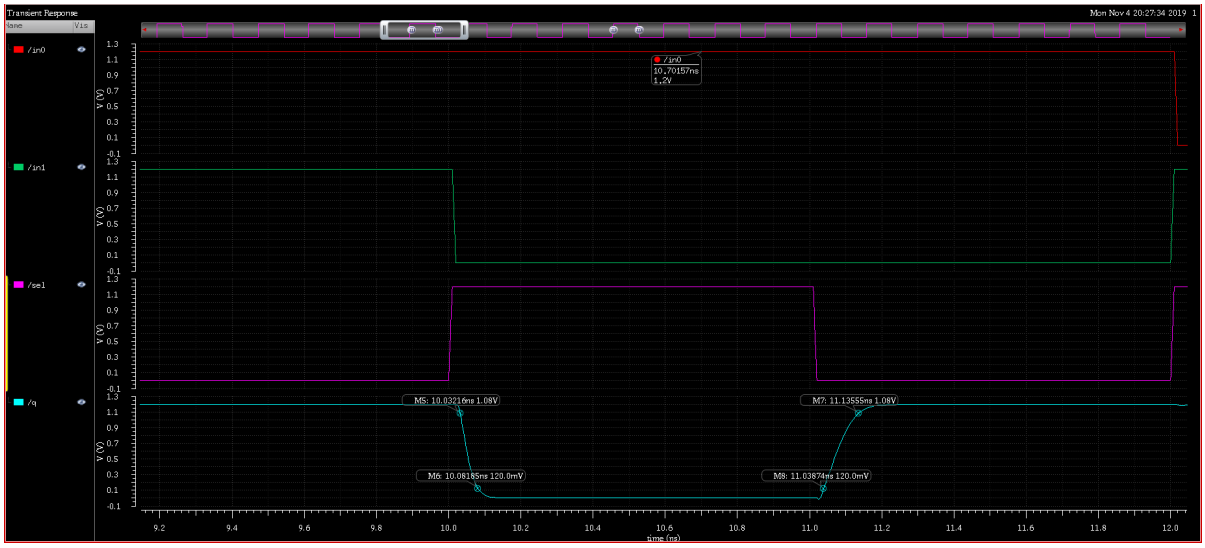
(a) First configuration's propagation delays



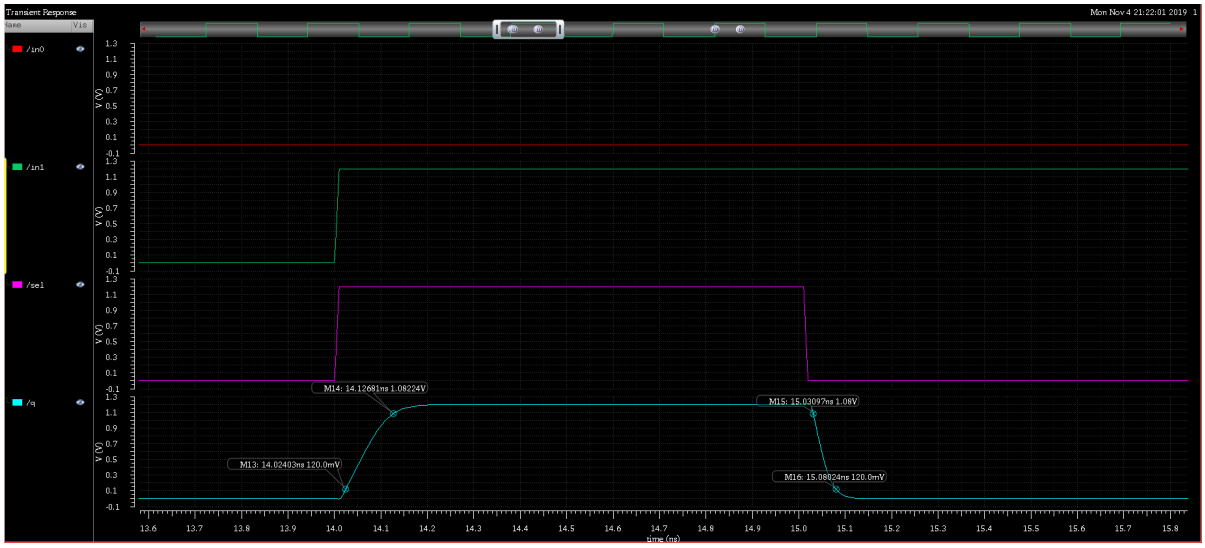
(b) Second configuration's propagation delays

Figure 5: Output propagation delays with respect to SEL input signal

From the 2 figures above, it can be concluded that the worst-case rising time is 0.10278 ($>$ 0.0968), which results from configuration 2 and the worst-case falling time is 0.0497 ($>$ 0.0493), which results from configuration 1.



(a) First configuration's rising and falling time



(b) Second configuration's rising and falling time

Figure 6: Rising and falling output time of the 2-to-1 mux

4 Layout Design and Verification Results

This section features the layout design (Figure 7) of the 2-to-1 mux and its verification results, done in the Virtuoso Layout Suite. The design shown below follows strictly the logic gate schematic connections in Figure 2. In addition, all inputs and output pins are connected to a higher metal layer, which is a good design consideration because the resulting mux layout will be easier to integrate into larger circuit.

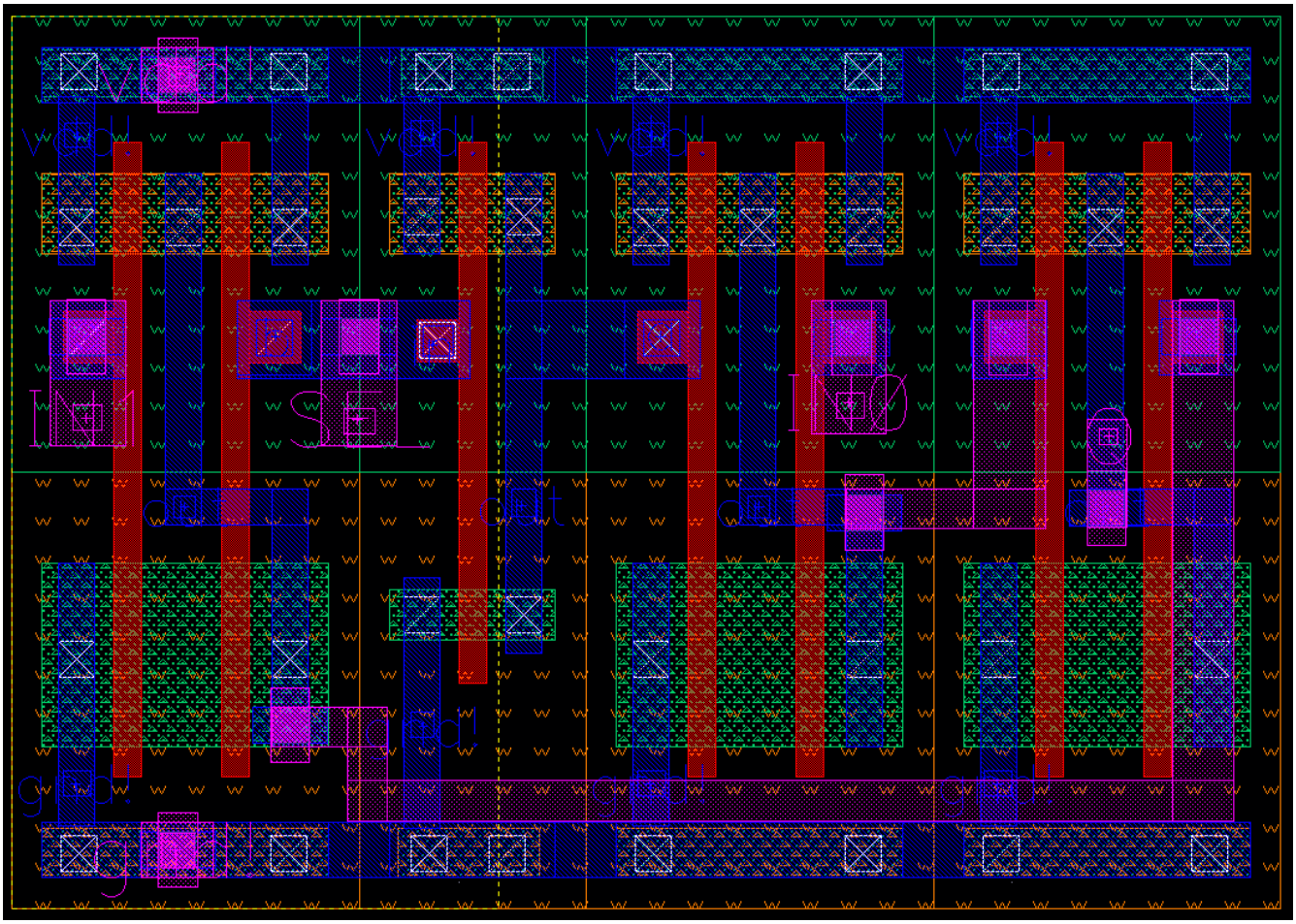
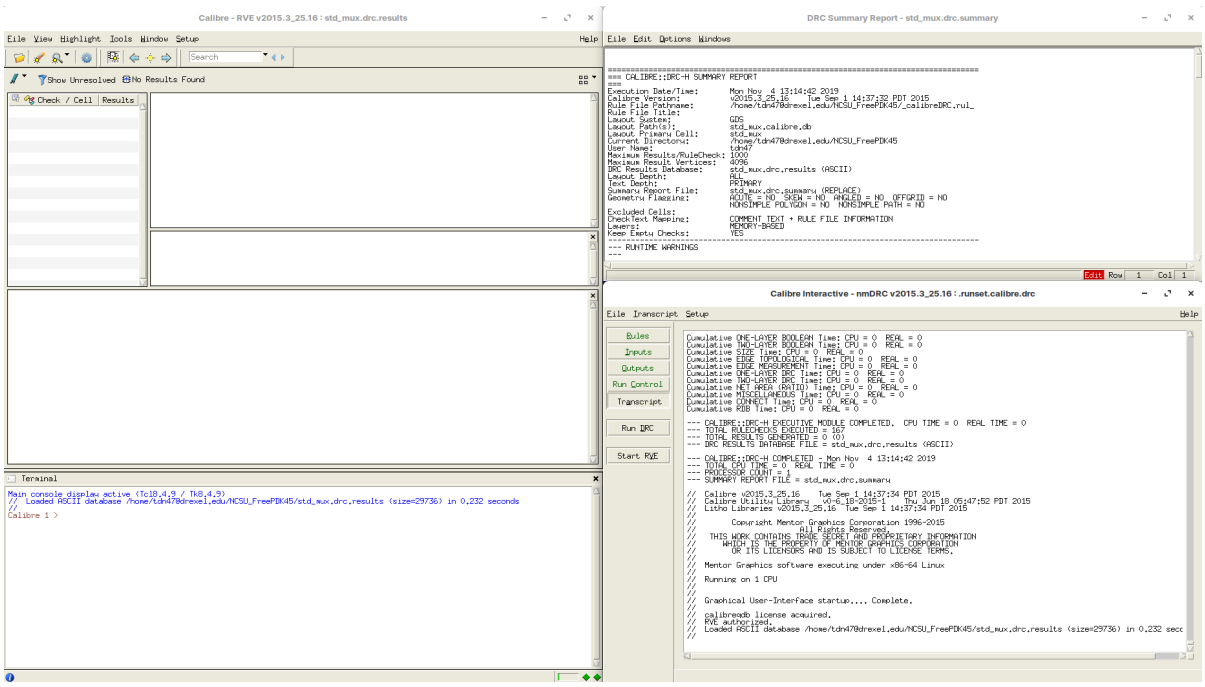
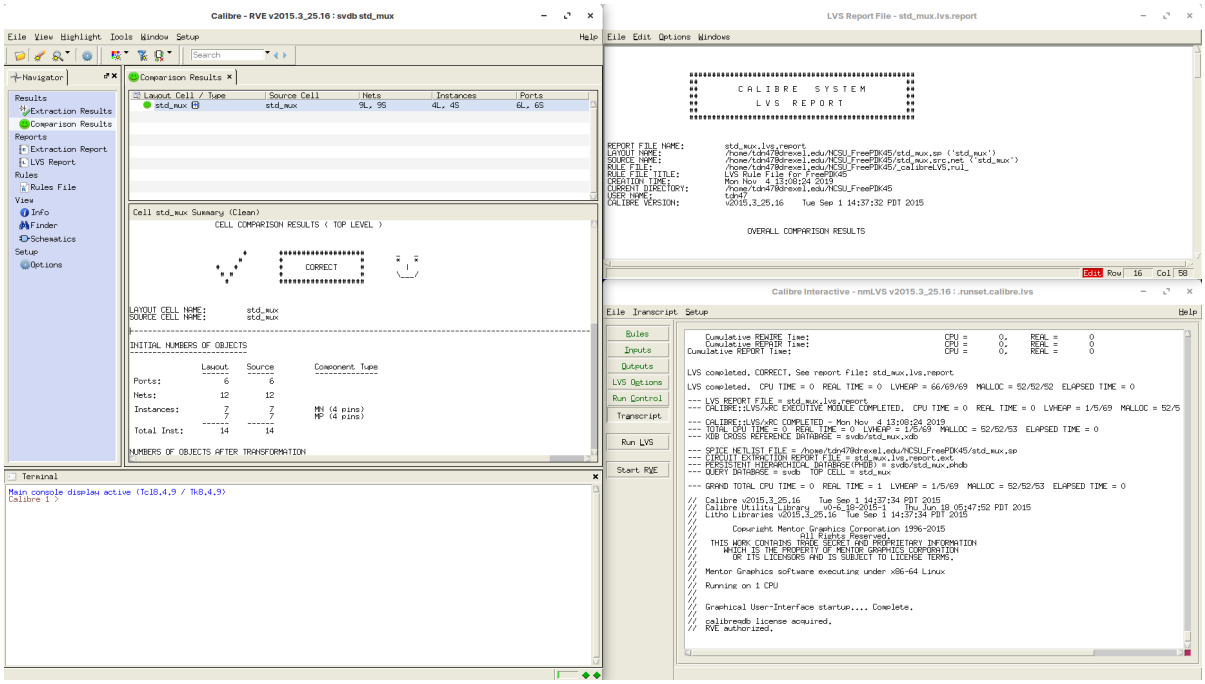


Figure 7: 2-to-1 mux layout in Virtuoso Layout Suite

With this design layout, the DRC and LVS physical verification results are shown below (Figure 8a & 8b).



(a) DRC Verification Results



(b) LVS Verification Results

Figure 8: 2-to-1 mux layout's verification results

5 Discussion and Conclusion

This laboratory explores the design and characteristic of such design for a 2-to-1 multiplexer. From the simulation results above, the mux's rising propagation delay is generally higher than its falling propagation delay. This phenomenon is due to the fact that when the output is 1, one of the two NAND gates has to be 1, which means that the network is trying to charge 4 PMOS, resulting in higher delay. When the

output is 0, both input NAND gates have to be 1, hence either path will only result in charging 2 PMOS. According to Table 2, the combination (IN0=0, IN1=1, SEL=1, Q=1) means that the output NAND is on, the upper input NAND is on and the inverter is on, which results in the network having to charge the PMOSes of 2 NAND gates and going through an inverter (whose PMOS capacitance does contribute to the output capacitance). Hence, that combination gives the highest delay. The reasoning for the resulting numbers from the other 3 cases follow the same pattern.