Lab Report 6: Edge-Triggered Flip-Flop

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ECEC 471: Introduction to VLSI

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Abstract

A Flip-Flop is a circuit device that has two stable states, in which information can be stored. This circuit can be triggered to change its state by applying one or more control inputs. For this reason, the Flip-Flop is a basic storage element, used in many sequential circuits. In this laboratory report, the design, layout and simulation of an Edge-Triggered D-Flip-Flop is created in Cadence Virtuoso Layout and Cadence Virtuoso Schematic Editor.

1 Initial Simulation and Results

The design for this experiment's Edge-Triggered D-Flip-Flop (DFF) is composed of standard gates: Inverter, 2-input NAND and 3-input NAND. Since the data can only be stored on a rising clock tick, the equation for the DFF is:

$$Q = \begin{cases} 1, & \text{Data if rising edge of Clock.} \\ 0, & \text{else keep previous data} \end{cases} \tag{1}$$

From this equation, a well known schematic for the D-Flip-Flip is shown in Figure 1:

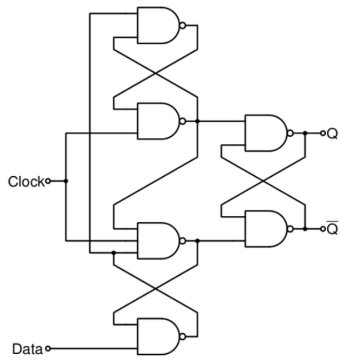


Figure 1: Schematic Illustration of the DFF

This exact schematic is simulated on Cadence's Virtuoso Schematic Editor (in Figure 2):

Since the DFF above contains inverters, 2-input NANDs and a 3-input NAND, 01 3-input NAND gate

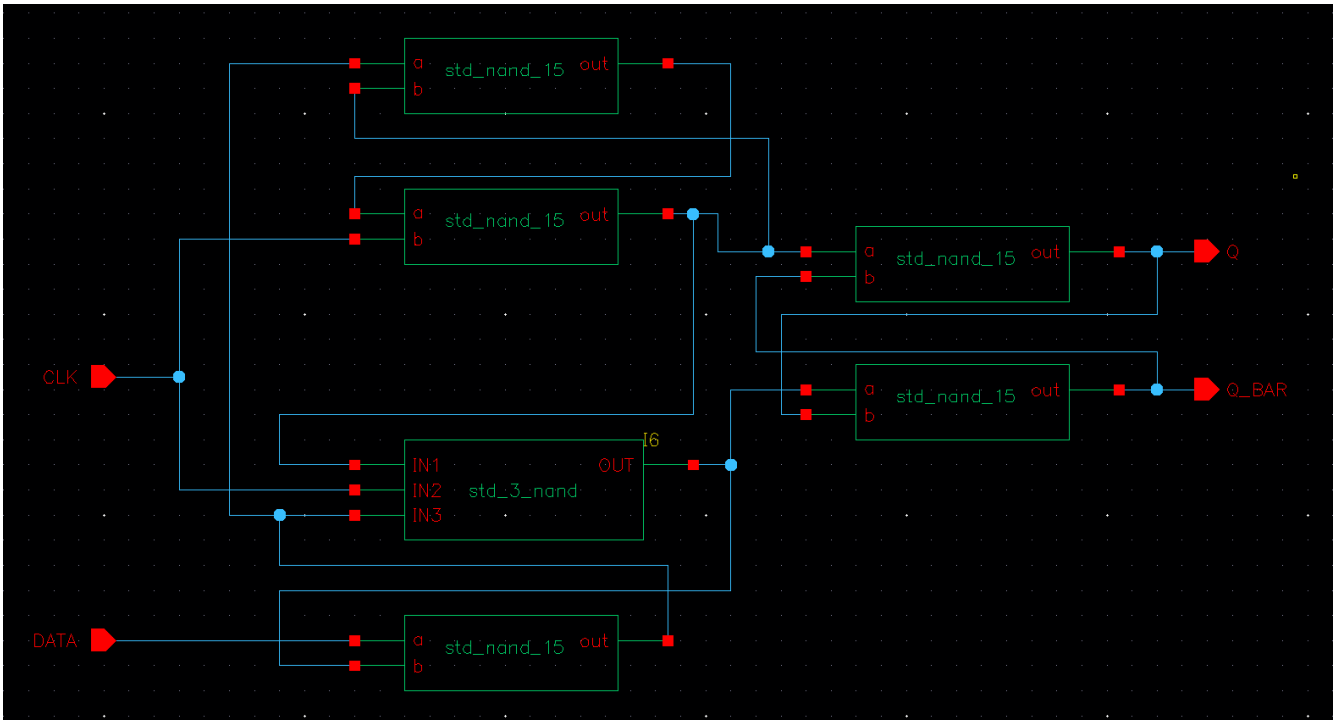
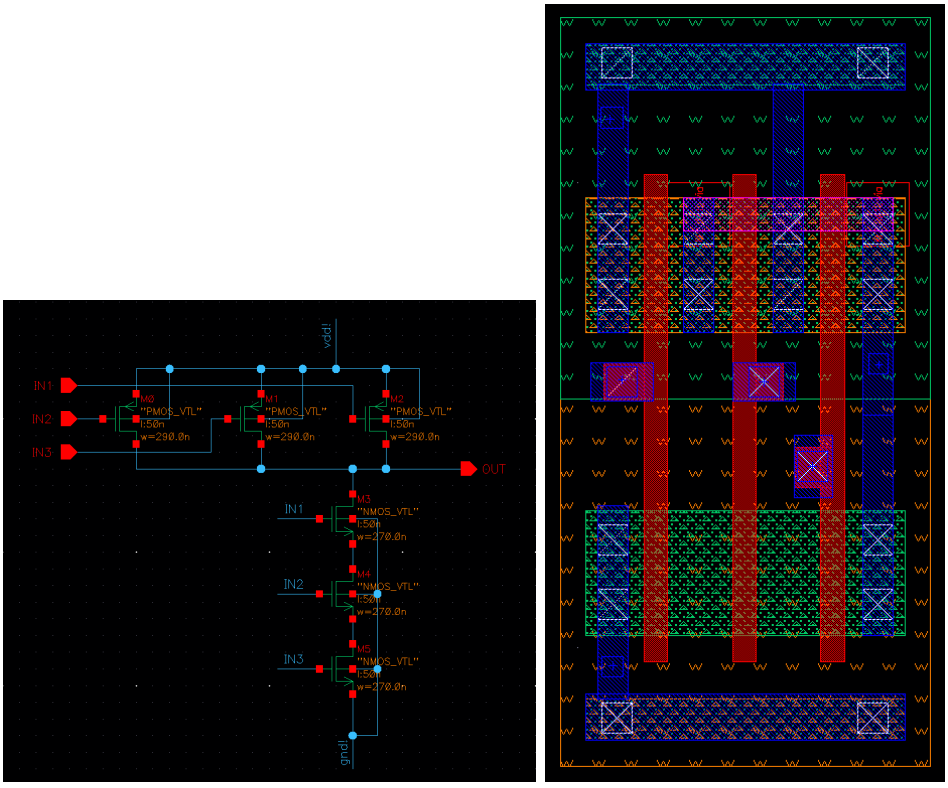


Figure 2: Schematic of the DFF in Cadence's Virtuoso Schematic Editor

had to be created (in addition to the 2-input NAND gate and the inverters in previous experiments) and simulated with Cadence (shown in Figure 3a and 3b).



(a) 3-input NAND gate schematics (b) 3-input NAND gate layout

Figure 3: 3-input NAND gate schematic and layout designs

The transient simulation results from the DFF above to verify the functionality of the D-flip-flop is shown below, in Figure 4

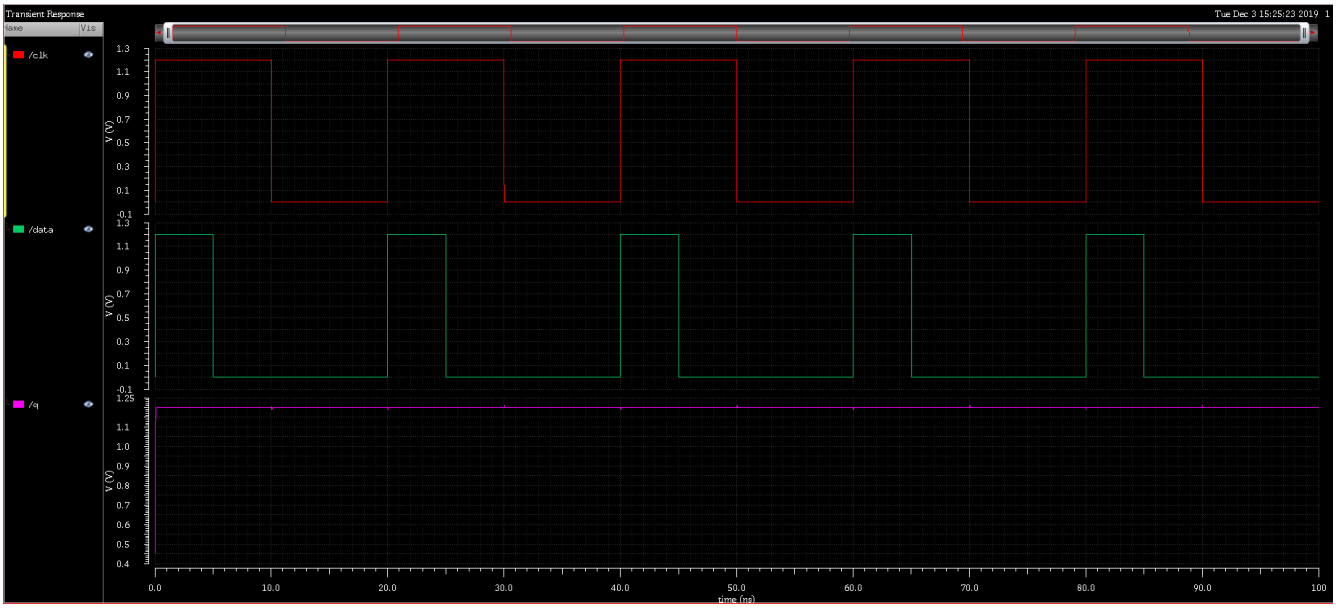


Figure 4: Initial transient simulation result of the DFF

2 DFF's Device Characteristics

In order to take a closer look at the DFF created above, its setup time, hold time, rise/fall time and propagation delay is measured. Measuring the device's setup time requires Cadence's Parameter Analysis Tool, which does a parameter sweep over the delay of the DATA signal. As discovered, this DFF has a negative setup time due to its own wiring (the clock signal is processed earlier than the data signal). Hence, the DATA signal is shifted to the right until the output cannot register a 1 – the shifted distance in time will be recorded as the setup time for this device (Figure 5)

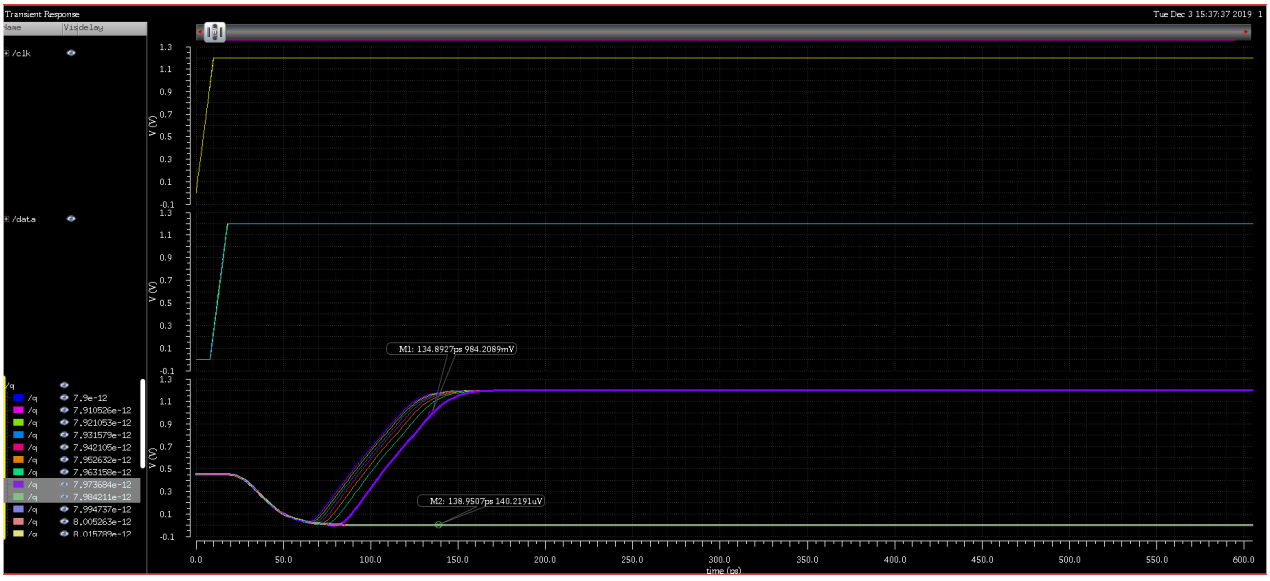


Figure 5: Parametric Sweep of the Delay to find DFF's Setup Time

From the simulation above, the setup time for the DFF is:

$t_{setup} = 7.973684e - 12 = 7.97ps$

Similarly, the hold time of this DFF is obtained by making the pulse width of the DATA signal smaller and smaller until the output cannot register a 1 – the smallest pulse width of the DATA signal is recorded as the hold time for this device (Figure 6)

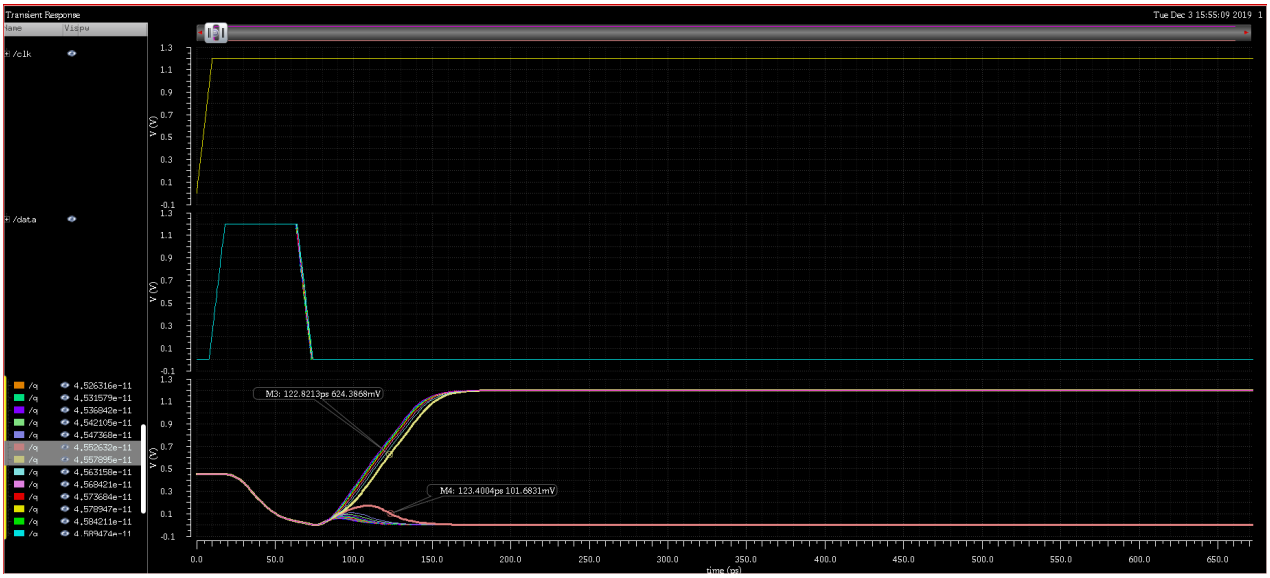


Figure 6: Parametric Sweep of the Delay to find DFF's Setup Time

From the figure above, the hold time for the DFF is:

$t_{hold} = 4.557895e - 11 = 45.58ps$

In addition, The rise time, fall time and propagation delay of the DFF can be obtained and shown in Figure 7a and 7b.

The rise time is:

$t_{rise} = 60.0626 - 60.0391 = 0.0235ns$

The fall time is:

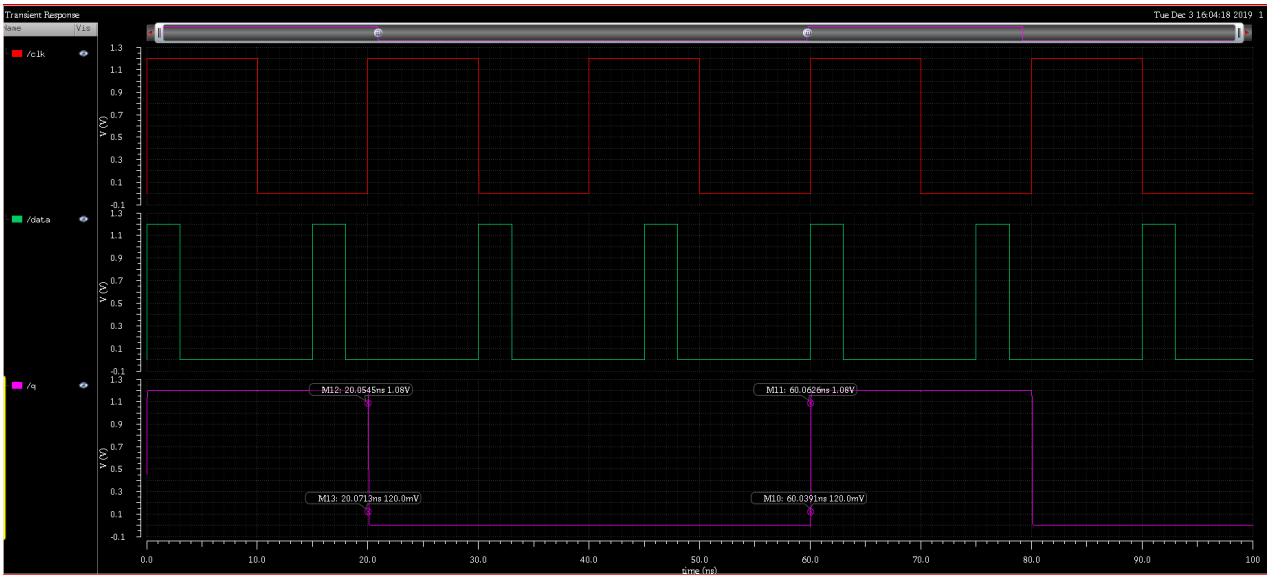
$t_{fall} = 20.0713 - 20.0545 = 0.0168ns$

The propagation delay is:

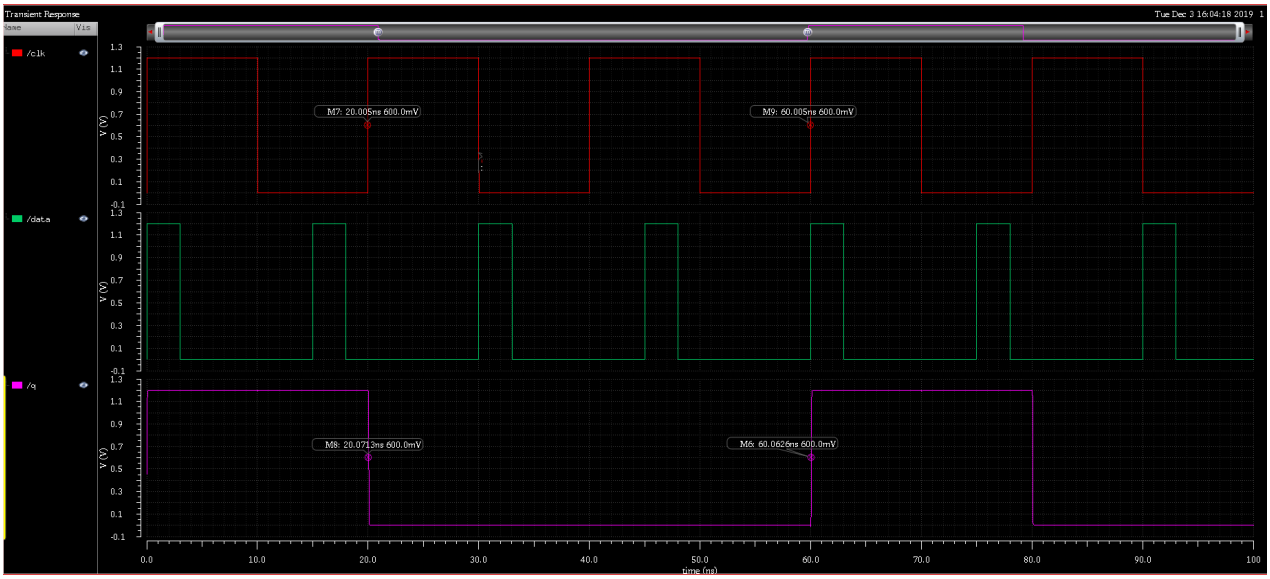
$t_{pdr} = 60.0626 - 60.005 = 0.0576ns$

$t_{pdf} = 20.0713 - 20.005 = 0.0663ns$

$t_{pd} = (0.0576 + 0.0663)/2 = 0.06195ns$



(a) DFF's rise and fall time



(b) DFF's propagation delay

Figure 7: Measurements of the DFF's rise/fall time and propagation delay

3 Layout Design and Physical Verification

The layout for the DFF is done with Cadence's Virtuoso Layout Suite and shown below in Figure 8: The DRC and LVS for this DFF is shown in Figure 9a and 9b:

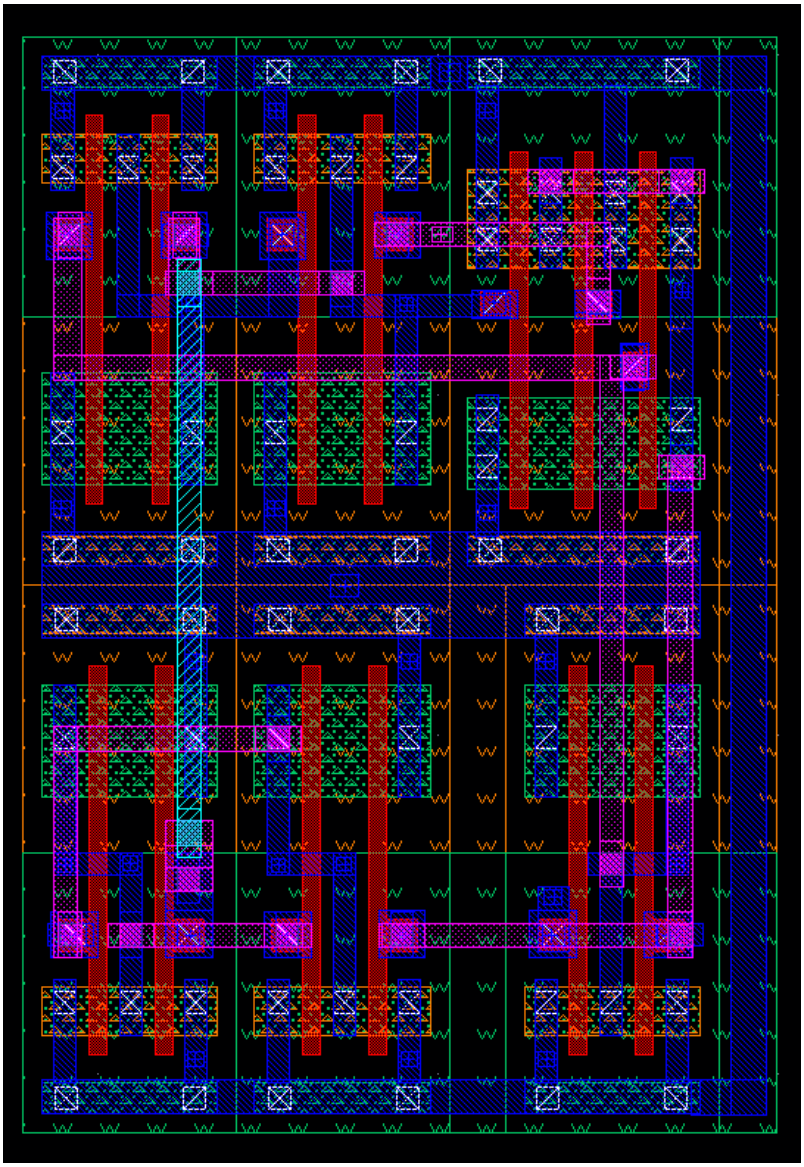
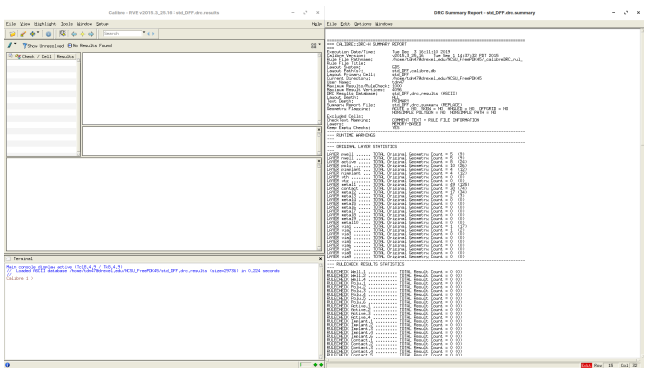
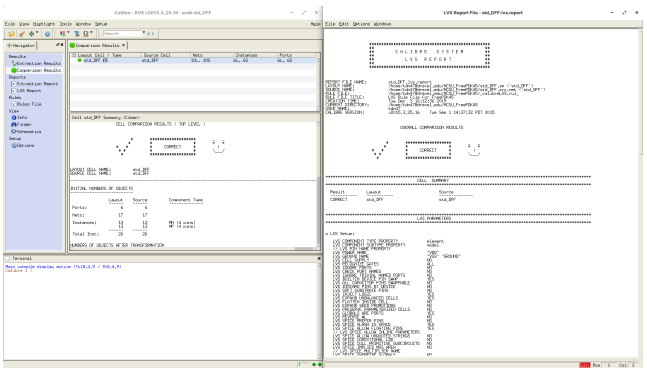


Figure 8: DFF's Layout in Cadence's Virtuoso Layout Suite



(a) DFF's rise and fall time



(b) DFF's propagation delay

Figure 9: Measurements of the DFF's rise/fall time and propagation delay

4 Discussion and Conclusion

The characteristic of the DFF created and simulated in this experiment is:

$t_{hold} = 4.557895e-11 = 45.58ps$

$t_{setup} = 7.973684e-12 = 7.97ps$

$t_{rise} = 60.0626 - 60.0391 = 0.0235ns$

$t_{fall} = 20.0713 - 20.0545 = 0.0168ns$

$t_{pd} = (0.0576 + 0.0663)/2 = 0.06195ns$

It is concluded that the setup time for this device is much smaller than its hold time, which means that the device needs the input DATA signal to be stable for much longer than it needs to be ready. The rise/fall time is not as symmetrical as it could be. This is due to the fact that the 3-input NAND gate in this design is not symmetrical. The propagation delay of the DFF is comparable to the 2-to-1 MUX in a previous experiment (0.06195ns vs. 0.06057ns).