# Lab Report 5: CMOS Inverter Chain and Ring Oscillator

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**Abstract**

In practical CMOS VLSI design, inverter chains are commonly used as buffers when the circuit needs to drive much higher load while maintaining good performance. With a specific input/output capacitance (load), an optimal chain of inverter can be built with good assumption about the parasitic capacitance. Hence, this laboratory experiment will feature the theoretical design along with a simulation of one such inverter chain. Also, in a different experiment, the simulation of a ring oscillator – a device which uses inverter chains to be able to handle the load of many gates – will be performed.

## 1 Experiment Introduction and Objectives

In the first of the 2 experiments detailed below, a chain of CMOS inverter is built with the input capacitance ($C_{in}$) of 0.1 fF, the output capacitance ($C_{out}$) of 5 fF, and the parasitic contribution of inverters ($p_{inv}$) is assumed to be 0.5. With this information, the stage effort, the number of stages and the sizing of individual inverters are calculated so that the chain has optimal performance. Using Cadence's Schematic and Layout Suite, along with its Analog Design Simulatior (ADE L) and Physical Verification Tools (DRC, LVS), the inverter chain will be created according to the above calculations. Then, the propagation delay (no parasitic contribution) is extracted and compared with that when parasitic capacitance is considered.

The second experiment, however, deals with a ring oscillator, which is made of 21 identically single sized inverters. The clock period and frequency are measured experimentally and theoretically.

# Part I

# Inverter Chain

## 2 Theoretical Calculations

Starting from a well known equation which calculate the path delay ($D$):

$$D = NF^{1/N} + P \tag{1}$$

In order to know how many stages (how many inverters should be added to the end of the chain) so that the path's stage effort is lowest, the derivative with respect to N of equation 1 is set to 0:

$$\frac{\partial D}{\partial N} = -F^{1/N} ln(F^{1/N}) + F^{1/N} + p_{inv} = 0 \tag{2}$$

Hence, the best stage effort $\rho = F^{1/N}$ is defined in the equation

$$\rho(1 - ln\rho) + p_{inv} = 0 \tag{3}$$

Using equation 3 and $p_{inv} = 0.5$, $\rho$ is numerically solved to be

$$\rho = 3.1809661 \tag{4}$$

From equation 4, the number of stages which gives the best stage effort is:

$$N = \frac{log(C_{out}/C_{in})}{log(\rho)} = \frac{log(50)}{log(3.1809661)} = 3.3806376 \tag{5}$$

Hence, two cases arise: $N = 3$ and $N = 4$. With $N = 3$, the minimum path delay is:

$$D_{N=3} = 3 * (50)^{1/3} + 3 = 14.05209\tau$$

With $N = 4$, the minimum path delay is:

$$D_{N=4} = 4 * (50)^{1/4} + 4 = 14.63659\tau$$

Since $D_{N=4} > D_{N=3}$, $N$ is chosen to be 3. Therefore, the sizing of the inverters are: $1C$, $50^{1/3}C = 3.68C$, $50^{2/3}C = 13.57C$, respectively.

Utilizing the symmetric inverter design from Lab 2, the PMOS/NMOS sizings of the individual inverters are: 145nm/90nm, 534nm/331nm, 1968nm/1221nm. Due to manufacturing constraint that all gate sizes must be fit on a 2.5nm grid, the PMOS/NMOS sizings are reconsidered accordingly to: **145nm/90nm, 535nm/330nm, 1970nm/1220nm**.

## 3 Schematic Simulation and Results

The schematic for the inverter chain is comprised of the 3 inverters with PMOS and NMOS sizing (Figure **??**) (found in the above section). The details regarding the schematics and the layouts for the individual inverters are given in the Appendix Section. Here, only the entire chain is focused and analyzed.

After the schematic is created, the entire chain is simulated in the ADE L tool (shown in Figure **??** and **??**).

The propagation delay of the inverter chain is measured in Figure **??**:

$t_{pdr} = 70.0395 - 70.015 = 0.02450ns$
$t_{pdf} = 60.0301 - 60.005 = 0.02510ns$
$t_{pd} = 0.02480ns$

The result above, however, does not take into account other factor affecting the delay, such as: intrinsic capacitance, long interconnects and real-parasitic contribution due to a particular layout design. Hence, the better approximation of the delay will come in the post-layout simulation, detailed in the Post-Layout Simulation and Results Section.

## 4 Layout Design and Verification Results

This section details the layout of the inverter chain. Similar to the schematic, the layout connects 3 inverters with increasing sizes (**145nm/90nm, 535nm/330nm, 1970nm/1220nm**). The final layout is shown in Figure **??** below:

The physical verifications of the layout above is shown in Figure **??** and **??**.

This layout will be used to generate the Post-Layout Simulation using Cadence Virtuoso Layout's PEX Calibre tool, which will account for all additional resistance and capacitance induced from this particular layout.

## 5 Post-Layout Simulation and Results

The PEX Calibre tool generates a Calibre View of the corresponding layout, which includes many parasitic resistors and parasitic capacitors (Figure **??**)

With the extracted view, the ADE L simulation is re-ran and the propagation delay is re-evaluated (Figure **??**)

The propagation delay of the Post-Layout Simulation is:

$t_{pdr} = 50.046 - 50.015 = 0.03100ns$
$t_{pdf} = 40.037 - 40.005 = 0.03200ns$
$t_{pd} = 0.03150ns$

## 6 Discussion and Conclusion

Considering the 2 propagation delay in Equation 3 and 5, it is clear that the delay of the post-layout simulation is larger than that of the pre-layout one ($0.03150 > 0.02480$). Although in Equation 3, the parasitic contribution is assumed to be 0.5, this number is just an estimation. Hence, the fact that when parasitic capacitance and resistance due to connecting wires is accounted, the propagation delay increases, is obvious.

# Part II

# Ring Oscillator

## 7 Schematic Simulation and Results

The Ring Oscillator featured in this laboratory composed of 21 identically single-sized inverters. Connecting all of the inverters create the schematic shown in Figure **??**.

The simulation for this schematic is done by injecting a stimulus to the system and recording the output's transient response (shown in Figure **??**).

From the figure above, the clock's period can be measured:

$$period = 5.558771 - 5.5345077 = 0.21369ns \tag{6}$$

And the frequency of the clock is:

$$f_{osc} = \frac{1}{0.21369 \times 10^{-9} s} = 4.67967 GHz \tag{7}$$

Knowing the approximation equation for the frequency of the oscillator:

$$f_{osc} = \frac{1}{2 \times N \times d} = \frac{1}{2 \times 21 \times 2 \times \tau} = \frac{1}{42 \times \tau} \tag{8}$$

From Equation 7 and 8, $\tau$ (the delay of 1 inverter) is: $5.08ps$.

And, the delay of 1 inverter measured from the simulation is $2.678997 - 2.673959 = 5.04ps$

## 8 Discussion and Conclusion

The results above show that the "theoretical" estimation is very close to the experimental measurements ($5.08ps$ and $5.04ps$). Hence, the ring oscillator behaves as expected.