ECEC–471\571 Introduction to VLSI Design

Lab Assignment #4
NAND and NOR CMOS Gates

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1 Objective

The goal of this assignment is to learn how to build a CMOS gate. This assignment will help build an understanding of:

- The basic principles of designing a *Nand* and a *Nor* CMOS gate.
- The characteristics of a *Nand* and a *Nor* CMOS gate.

Note, set the voltage level (*Vdd*) for SPICE simulation to 1.2 V. The same voltage level should be used for the input signals to both the NAND and NOR gates.

2 Assignments

Design, simulate and build the layout of a `Nand` and a `Nor` CMOS gate.

2.1 Design a `Nand` Gate

1. Design a two input `Nand` gate, where the inputs are labeled `a` and `b`, and the output is labeled `out`. The schematic of the `Nand` gate is shown in Figure 1.
2. Simulate the transient response of the symmetrical `Nand` gate and measure the worst-case propagation delay, rise, and fall times for a pulse input.

   Input pulse parameters:

   - time period: 2 ns
   - rise time: 5 ps
   - fall time: 5 ps
   - pulse width: 1 ns
3. Simulate the DC response of the `Nand` gate for the worst-case input scenario, and determine the transistor sizing for a symmetrical `Nand` gate
4. Create the layout view of the `Nand` gate
   - Make sure the total cell height is 1.5 μm

- Use 0.1 μm for the width of the `Vdd` and `Gnd` rails
- A reference for the layout is shown in Figure 2.

5. Perform DRC verification.
6. Perform LVS verification.

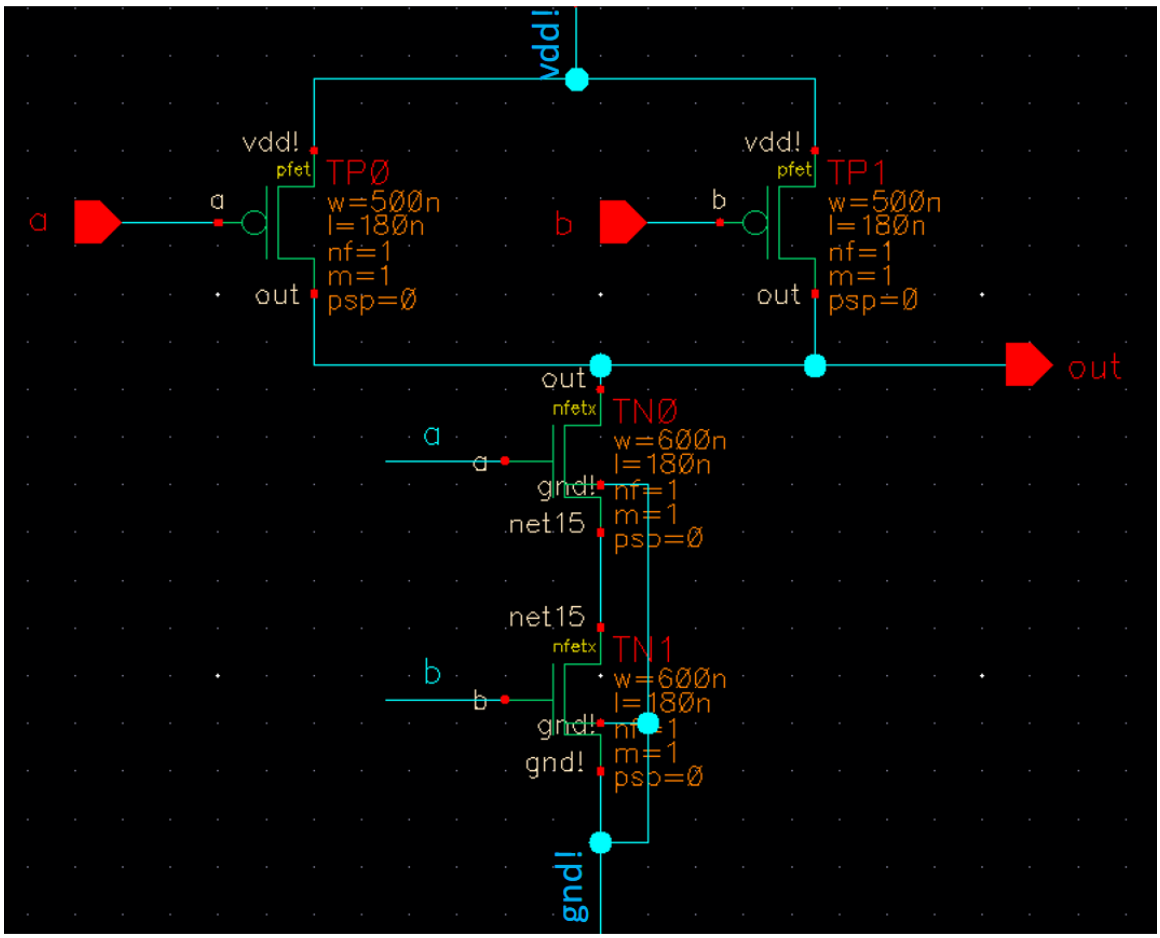

Figure 1: A schematic illustration of the *Nand* gate.

2.2 Design a `Nor` Gate

1. Design a two input `Nor` gate, where the inputs are labeled `a` and `b`, and the output is labeled `out`. The schematic of the `Nor` gate is shown in Figure 3.
2. Simulate the transient response of the symmetrical `Nor` gate and measure the worst-case propagation delay, rise, and fall times for a pulse input.

   Input pulse parameters:

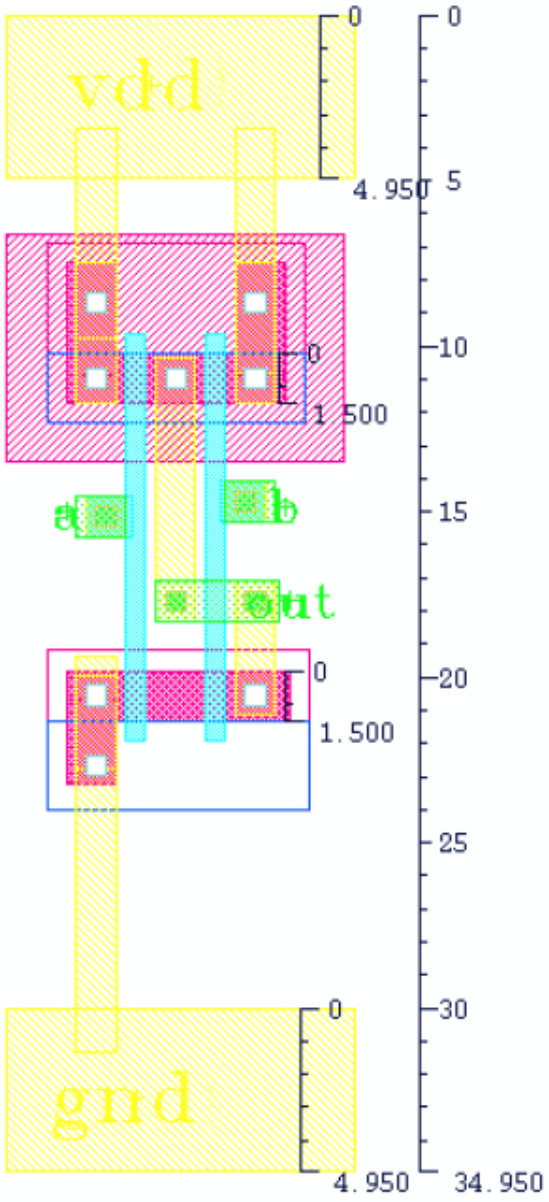

Figure 2: A layout reference of the *Nand* gate Note: This is a different CMOS technology

- time period: 2 ns
- rise time: 5 ps
- fall time: 5 ps
- pulse width: 1 ns

3. Simulate the DC response of the `Nor` gate for the worst-case input scenario, and determine the transistor sizing for a symmetrical `Nor` gate

4. Create the layout view of the `Nor` gate
    - Make sure the total cell height is 1.5 μm
    - Use 0.1 μm for the width of the `Vdd` and `Gnd` rails
5. Perform DRC verification.
6. Perform LVS verification.

2.3 Deliverables

Your report should include the following:

- The schematic view and the layout view of both the `Nand` gate and the `Nor` gate.
- Show DRC and LVS results for both the `Nand` gate and the `Nor` gate.
- Perform transient simulations on the `Nand` gate and the `Nor` gate to check the functionality, respectively.
- Measure the worst-case propagation delay, rise, and fall time for a pulse input for both the `Nand` and the `Nor` gates based on the simulation results.
- Perform a DC simulation on the schematic view of the `Nand` gate and the `Nor` gate to plot the V_{in} versus V_{out} curve. Use markers to show the switching threshold. Find the sizes of the transistors to make the symmetrical version of the Size the `Nand` and the `Nor` gate.

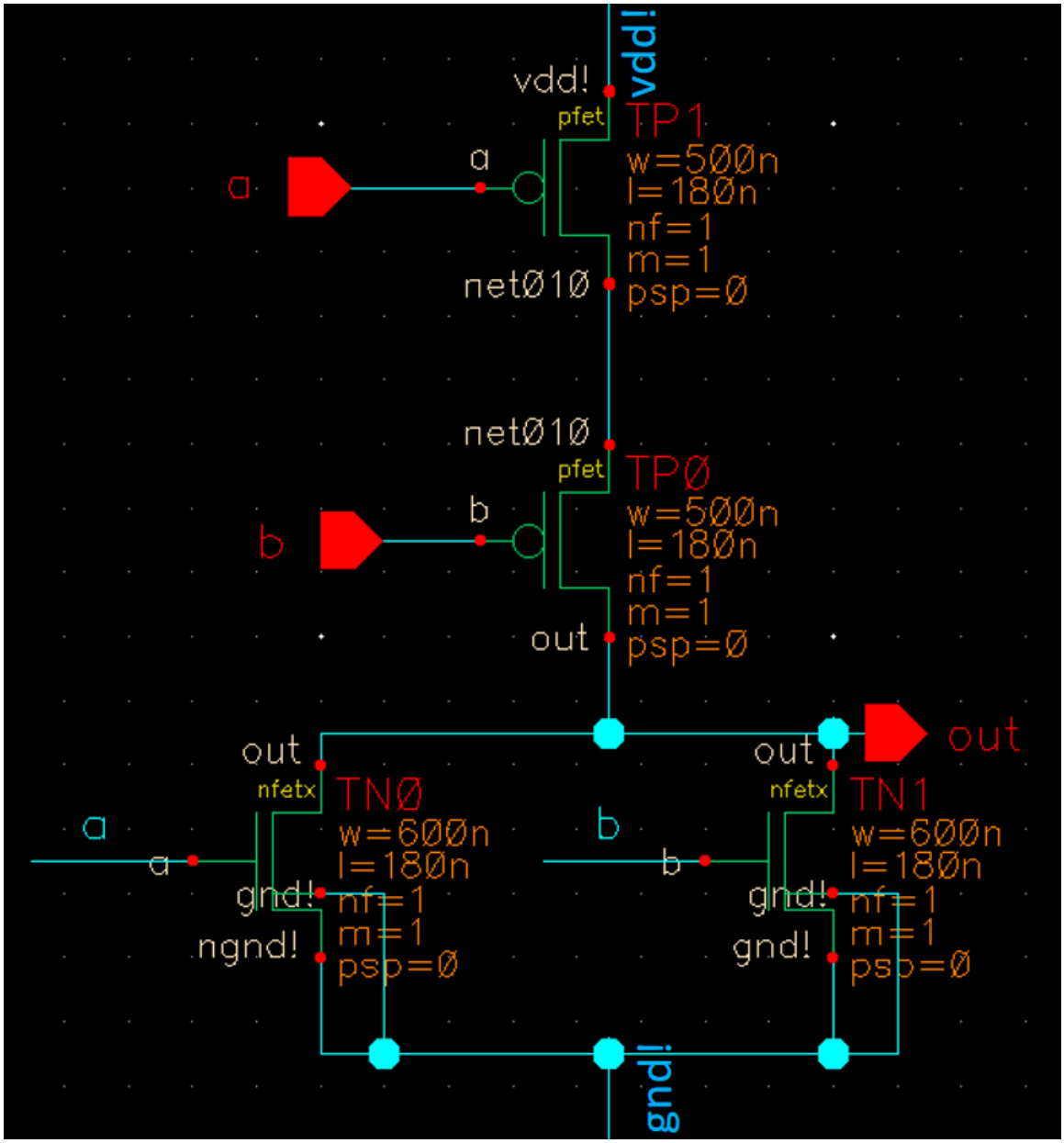

Figure 3: A schematic illustration of the *Nor* gate.