Predictable Performance and Fairness Through Accurate Slowdown Estimation in Shared Main Memory Systems

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This paper summarizes the ideas and key concepts of MISE (Memory Interference-induced Slowdown Estimation), which was published in HPCA 2013 [97], and examines the work's significance and future potential. Applications running concurrently on a multicore system interfere with each other at the main memory. This interference can slow down different applications differently. Accurately estimating the slowdown of each application in such a system can enable mechanisms that can enforce quality-of-service. While much prior work has focused on mitigating the performance degradation due to inter-application interference, there is little work on accurately estimating slowdown of individual applications in a multi-programmed environment. Our goal is to accurately estimate application slowdowns, towards providing predictable performance.

To this end, we first build a simple Memory Interference-induced Slowdown Estimation (MISE) model, which accurately estimates slowdowns caused by memory interference. We then leverage our MISE model to develop two new memory scheduling schemes: 1) one that provides soft quality-of-service guarantees, and 2) another that explicitly attempts to minimize maximum slowdown (i.e., unfairness) in the system. Evaluations show that our techniques perform significantly better than state-of-the-art memory scheduling approaches to address the above problems.

Our proposed model and techniques have enabled significant research in the development of accurate performance models [35, 59, 98, 110] and interference management mechanisms [66, 66, 99, 100, 108, 119, 120].

1. Problem: Unpredictable Slowdowns

In a multicore system, multiple applications are consolidated on the same machine. While consolidation may enable better resource utilization, it results in interference between applications at the shared resources, slowing down each application to a different degree. Specifically, main memory is a heavily contended shared resource between applications in a multicore system. Each application accessing the memory experiences different and unpredictable slowdowns depending on the available memory bandwidth and the other concurrently running applications.

A large body of work proposed several different approaches to mitigate memory interference between applications with the goal of improving overall system performance. This includes memory scheduling [2,18,27,32,42,43,50,72,76,77,80,99, 100, 103, 117], memory channel/bank partitioning [36, 64, 74], memory interleaving [38], source throttling [3, 7, 17, 19, 102], and thread scheduling [14, 101, 106, 121] techniques. However, few previous works (notably [15, 17, 19, 76]) have attempted to estimate individual application slowdowns online with the goal of providing predictable performance.

Our goal in our HPCA 2013 paper [97] is to provide predictable performance for individual applications. To this end, we first design a model to accurately estimate memory-interference-induced slowdowns of applications running concurrently on a multicore system. We then leverage this model to design effective mechanisms to enforce quality-of-service (QoS) and achieve fairness.

2. The Memory Interference-Induced Slowdown Estimation (MISE) Model

The slowdown of an application indicates the performance of the application, when it is sharing resources with other applications, relative to when the application is run alone. Slowdown can be expressed as

$$\text{Slowdown of an App.} = \frac{\text{alone-performance}}{\text{shared-performance}} \qquad (1)$$

Hence, estimating the slowdown of an individual application requires two pieces of information: 1) the performance of the application when it is run concurrently with other applications (i.e., *shared-performance*), and 2) the performance of the application when it is run alone on the same system (i.e., *alone-performance*). While the former can be directly measured, the key challenge is to estimate the performance the application would have if it were running alone *while* it is actually running alongside other applications. This requires quantifying the effect of interference on application performance.

2.1. Key Observations

In this work, we make two observations that lead to a simple and effective model to estimate the slowdown of individual applications.

Observation 1: *The performance of a memory-bound application is roughly proportional to the rate at which its memory requests are served.* This observation stems from a memory-bound application's characteristic to spend an overwhelmingly large fraction of its execution time stalling on memory accesses. Therefore, the rate at which such an application's requests are served has significant impact on its performance.

To validate this observation, we conducted a real-system experiment where we ran a memory-bound application from the SPEC CPU2006 benchmark suite [96] alongside three copies of a microbenchmark whose memory intensity can be varied, on a 4-core Intel Core i7 [31].[1] By varying the memory intensity, i.e., the last-level cache (LLC) miss rate, of the microbenchmark, we can change the rate at which the requests of the SPEC application are served. Figure 1 plots the results of this experiment for three memory-intensive benchmarks, *mcf*, *omnetpp*, and *astar*. The figure shows the performance of each application versus the rate at which its requests are served.
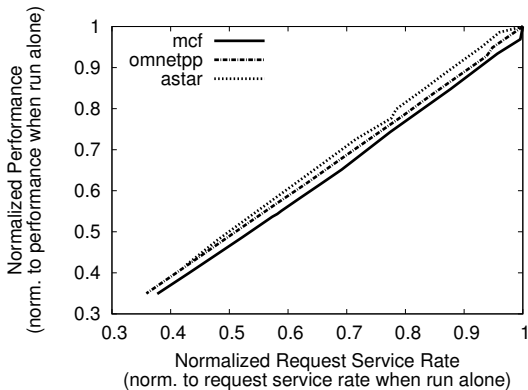
Figure 1: Request service rate vs. performance. Reproduced from [97].

The results of this experiment validate our observation. The performance of a memory-bound application is directly proportional to the rate at which its requests are served. This suggests that we can use the request-service-rate of an application as a proxy for its performance. More specifically, we can estimate the slowdown of an application, i.e., the ratio of its performance when it is run alone on a system vs. its performance when it is run alongside other applications on the same system, as follows:

$$\text{Slowdown of an App.} = \frac{alone\text{-}request\text{-}service\text{-}rate}{shared\text{-}request\text{-}service\text{-}rate} \quad (2)$$

Estimating the *shared-request-service-rate* (SRSR) of an application is straightforward. It only requires the memory controller to keep track of how many requests of the application are served in a given number of cycles. However, the challenge is to estimate the *alone-request-service-rate* (ARSR) of an application *while* it is run alongside other applications. A naive way of estimating ARSR of an application would be to prevent all other applications from accessing memory for a length of time and measure the application's ARSR. While this approach might provide an estimate of the application's ARSR, it would significantly slow down other applications in

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[1]The microbenchmark streams through a large region of memory (one block at a time). The memory intensity of the microbenchmark (last-level cache misses per kilo-instruction, i.e., LLC MPKI) is varied by changing the amount of computation performed between memory operations.

the system and is prone to incorrect estimations due to phase fluctuations in the application. Our second observation helps us to address this problem.

Observation 2: *The ARSR of an application can be estimated by giving the requests of the application the highest priority in accessing memory.*

Giving an application's requests the *highest priority* in accessing memory results in very little interference from the requests of other applications. Therefore, requests of the application are served almost as if the application were the only one running on the system. Based on the above observation, the ARSR of an application can be estimated as:

$$\text{ARSR of an App.} = \frac{\text{\# Requests with Highest Priority}}{\text{\# Cycles with Highest Priority}} \quad (3)$$

where *# Requests with Highest Priority* is the number of requests served when the application is given highest priority, and *# Cycles with Highest Priority* is the number of cycles an application is given highest priority by the memory controller.

The memory controller can use Equation 3 to periodically estimate the ARSR of an application. We add an interference counter to capture the remaining interference cycles. The details of the mechanisms we add to increase the accuracy of the model are described in Section 4 of our HPCA 2013 paper [97]. Once we estimate ARSR, Equation 2 can be used to estimate the slowdown of the application.

2.2. MISE Model for Non-Memory-Bound Applications

So far, we have described the key observations of the MISE model for a memory-bound application. We find that the model presented above has low accuracy for non-memory-bound applications. This is because a non-memory-bound application spends a significant fraction of its execution time in the *compute phase* (when the core is *not* stalled waiting for memory). Hence, varying the request service rate for such an application will not affect the length of the large compute phase. Therefore, we take into account the duration of the compute phase to make the model accurate for non-memory-bound applications.

Let α be the fraction of time spent by an application stalling at memory. Therefore, the fraction of time spent by the application in the compute phase is $1 - \alpha$. Since changing the request service rate affects only the memory phase, we augment Equation 2 to take into account α as follows:

$$\textit{Slowdown of an App.} = (1 - \alpha) + \alpha \frac{\text{ARSR}}{\text{SRSR}} \quad (4)$$

In addition to estimating ARSR and SRSR required by Equation 2, the above equation requires estimating the parameter α, the fraction of time spent in the memory phase. However, precisely computing α for a modern out-of-order processor is a challenge since such a processor overlaps computation

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with memory accesses. The processor stalls waiting for memory only when the oldest instruction in the reorder buffer is waiting on a memory request. For this reason, we estimate α as the fraction of time the processor spends stalling for memory:

$$\alpha = \frac{\text{\# Cycles spent stalling on memory requests}}{\text{Total number of cycles}} \quad (5)$$

More details of our MISE slowdown estimation model are described in Sections 3 and 4 of our HPCA 2013 paper [97]. More recently, we used this model to expand slowdown estimation to a memory hierarchy that also includes shared caches, as part of the Application Slowdown Model [98].

3. Evaluation of the MISE Model

We compare the MISE model against the slowdown estimation model employed by the Stall Time Fair Memory Scheduler (STFM) [76], which is the closest previous work on estimating memory interference-induced slowdown.[2] STFM estimates the slowdown of an application by estimating the number of cycles it stalls due to interference from other applications' requests. In this section, we qualitatively and quantitatively compare MISE with STFM.

There are two key differences between MISE and STFM in estimating slowdown. First, MISE uses request service rates rather than stall times to estimate slowdown. In MISE, the *alone-request-service-rate* of an application can be fairly accurately estimated by giving the application highest priority in accessing memory. Giving the application highest priority in accessing memory results in very little interference from other applications. In contrast, STFM attempts to estimate the alone-stall-time of an application while it is receiving significant interference from other applications, which turns out to be difficult to do accurately. Second, MISE takes into account the effect of the compute phase for non-memory-bound applications. STFM, on the other hand, has no such provision to account for the compute phase. As a result, MISE's slowdown estimates for non-memory-bound applications are significantly more accurate than STFM's estimates.

Figure 2 compares the accuracy of MISE with STFM for two representative memory-bound applications, lbm and leslie3d. Figure 3 compares the accuracy of MISE with STFM for two representative non-memory-bound applications, wrf and povray. Each of these applications is run on a 4-core system with three other applications. Our detailed experimental methodology is provided in Section 5 of our HPCA 2013 paper [97]. This includes detailed descriptions of our experimental setup, workloads and metrics. Furthermore, our simulator implementing the MISE model is available online [90]. As can be observed, MISE's slowdown estimates

are much closer to the actual slowdown than STFM's estimates. This is because the MISE model eliminates a significant portion of the interference received by an application while estimating slowdown, by prioritizing it in the memory controller. On the other hand, STFM estimates slowdown *while* an application is experiencing interference.
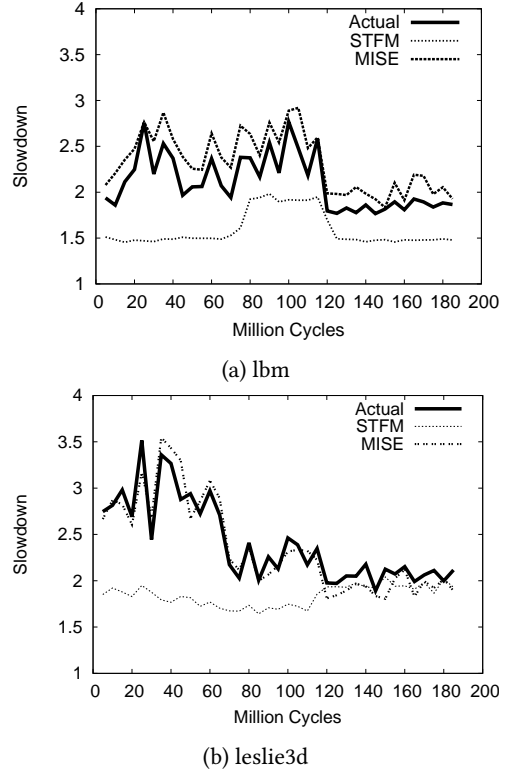

(a) lbm

(b) leslie3d

Figure 2: Comparison of MISE with STFM for representative memory-bound applications. Adapted from [97].

Table 1 shows the average slowdown estimation error for each benchmark, with STFM and MISE, across 300 4-core workloads of different memory intensities. As can be observed, MISE's slowdown estimates have significantly lower error than STFM's slowdown estimates across most benchmarks. Across *300* workloads, STFM's estimates deviate from the actual slowdown by 29.8%, whereas, our proposed MISE model's estimates deviate from the actual slowdown by only 8.1%. Therefore, we conclude that our slowdown estimation model provides better accuracy than STFM.

For a more detailed analysis of the MISE model's accuracy and characteristics, we refer the reader to our HPCA 2013 paper [97].

4. Leveraging the MISE Model

Accurate slowdown estimates are a key enabler towards designing mechanisms to better enforce quality-of-service (QoS) and fairness. Slowdown estimates from the MISE model could be leveraged in hardware to design memory scheduling policies to provide QoS guarantees and fairness. Alternatively, the slowdown estimates could be communicated to the

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[2]FST [17] and Du Bois et al.'s per-thread cycle accounting mechanism [15] are the other two previous works that estimate application slowdown. The mechanism to estimate main memory interference induced slowdown in both of these previous works is similar to STFM.
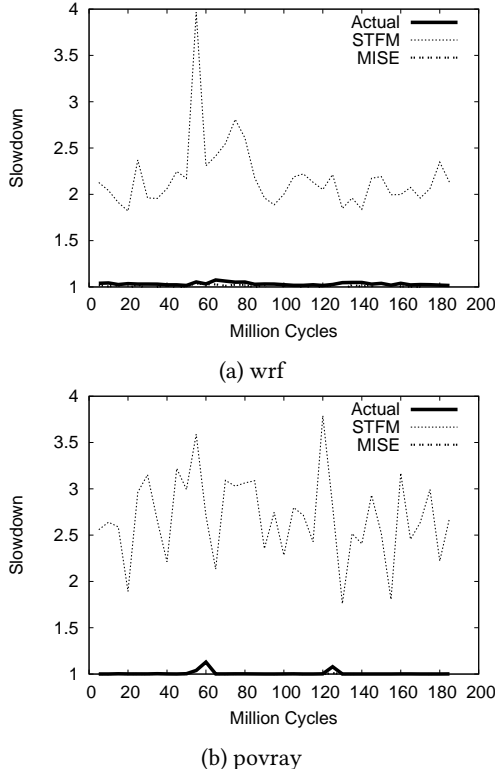
(a) wrf

(b) povray

Figure 3: Comparison of MISE with STFM for representative non-memory-bound applications. Adapted from [97].

Table 1: Average slowdown estimation error for each benchmark (in %). Adapted from [97].

Benchmark	STFM	MISE	Benchmark	STFM	MISE
453.povray	56.3	0.1	473.astar	12.3	8.1
454.calculix	43.5	1.3	456.hmmer	17.9	8.1
400.perlbench	26.8	1.6	464.h264ref	13.7	8.3
447.dealII	37.5	2.4	401.bzip2	28.3	8.5
436.cactusADM	18.4	2.6	458.sjeng	21.3	8.8
450.soplex	29.8	3.5	433.milc	26.4	9.5
444.namd	43.6	3.7	481.wrf	33.6	11.1
437.leslie3d	26.4	4.3	429.mcf	83.74	11.5
403.gcc	25.4	4.5	445.gobmk	23.1	12.5
462.libquantum	48.9	5.3	483.xalancbmk	18.0	13.6
459.GemsFDTD	21.6	5.5	435.gromacs	31.4	15.6
470.lbm	6.9	6.3	482.sphinx3	21	16.8
473.astar	12.3	8.1	471.omnetpp	26.2	17.5
456.hmmer	17.9	8.1	465.tonto	32.7	19.5

system software, which could leverage them to perform application scheduling, admission control and migration. We will describe two such mechanisms that leverage the MISE model: 1) MISE-QoS, a mechanism to provide soft QoS guarantees in the memory controller; and 2) MISE-Fair, a mechanism to minimize maximum slowdown [13, 14, 42, 43, 92, 99, 100, 103] to improve overall system fairness.

4.1. MISE-QoS: Providing Soft QoS Guarantees

MISE-QoS aims to provide soft slowdown guarantees to an application of interest (AoI) in a workload with many applications, while trying to maximize overall performance

for the remaining applications. There are two aspects of providing a soft slowdown guarantee. One is to ensure that the application of interest is not slowed down by more than a system-software-specified bound. The other aspect is to detect if the bound is *not met* for some reason.

MISE-QoS addresses both of these aspects by using slowdown estimates from the MISE model. It periodically obtains slowdown estimates from the MISE model and increases/decreases the memory bandwidth allocated to the AoI such that the AoI receives just enough bandwidth to meet its slowdown bound. This enables the other applications to use the remaining bandwidth, improving their performance. MISE-QoS addresses the second aspect by comparing slowdown estimates from the MISE model with the prescribed bound periodically. When the prescribed bound cannot be met despite always prioritizing the AoI, MISE-QoS detects that the bound cannot be met just by prioritizing the application at the memory controller.

Previous work [34] attempts to address the first aspect by *always* prioritizing the AoI. This may unnecessarily slowdown other applications in the system by excessively prioritizing the AoI, especially when the AoI is meeting its performance bound. Furthermore, such a mechanism, in the absence of accurate slowdown estimates, does not have the provision to detect whether or not the bound is met.

Slowdown Evaluation. We evaluate the MISE-QoS mechanism across 300 workloads with 10 different slowdown bounds for each workload. Our results show that the MISE-QoS mechanism meets the prescribed slowdown bound for 97.5% of the workloads for which the naive mechanism that always prioritizes the AoI meets the bound, while improving overall system performance by 12%. Furthermore, MISE-QoS also predicts whether or not the bound is met with an accuracy of 95.7%, while previous work [34] has no such provision.

To show the effectiveness of MISE-QoS, we compare the AoI's slowdown due to MISE-QoS and the mechanism that always prioritizes the AoI (*Always Prioritize*) [34]. Figure 4 presents representative results for 8 different AoIs when they are run alongside three other applications. The label MISE-QoS-n corresponds to a slowdown bound of $\frac{10}{n}$. (Note that *Always Prioritize* does not take into account the slowdown bound.) Note that the slowdown bound decreases (i.e., becomes tighter) from left to right for each benchmark in Figure 4 (as well as in other figures).

We draw three conclusions from the results. First, for most applications, the slowdown of *Always Prioritize* is considerably more than one. This indicates that always prioritizing the AoI does not completely prevent other applications from interfering with the AoI. Second, as the slowdown bound for the AoI is decreased (left to right), MISE-QoS gradually increases the bandwidth allocation for the AoI, eventually allocating all the available bandwidth to the AoI. At this point, MISE-QoS performs very similarly to the *Always Prioritize* mechanism. Third, in almost all cases (in this figure and
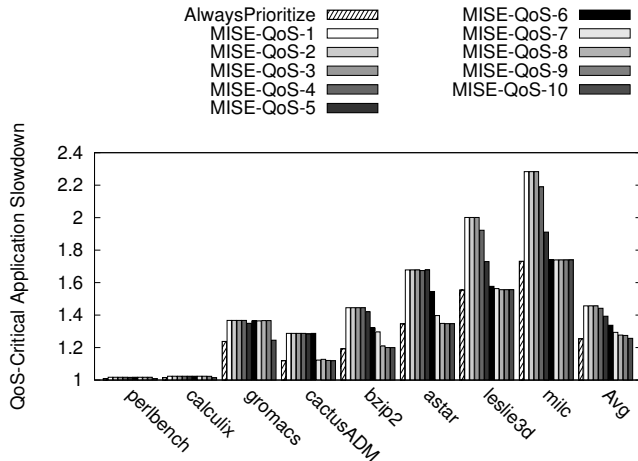
Figure 4: AoI performance: MISE-QoS vs. *AlwaysPrioritize*. **Reproduced from [97].**

across all our 3000 data points), MISE-QoS meets the specified slowdown bound *if Always Prioritize* is able to meet the bound (see Section 8.1 of our HPCA 2013 paper [97] for details).

System Performance and Fairness. Figure 5 compares the system performance (harmonic speedup) and fairness (maximum slowdown) of MISE-QoS and *Always Prioritize* for different values of the bound. We omit the AoI from the performance and fairness calculations. The results are categorized into four workload categories (0, 1, 2, 3) indicating the number of memory-intensive benchmarks in the workload. For clarity, the figure shows results only for a few slowdown bounds. Three conclusions are in order.

First, MISE-QoS significantly improves performance compared to *Always Prioritize*, especially when the slowdown bound for the AoI is large. On average, when the bound is $\frac{10}{3}$, MISE-QoS improves harmonic speedup [67] by 12% and weighted speedup [22, 95] by 10% (not shown due to lack of space) over *Always Prioritize*, while reducing maximum slowdown [13, 14, 42, 43, 92, 99, 100, 103] by 13%. Second, as expected, the performance and fairness of MISE-QoS approach that of *Always Prioritize* as the slowdown bound is decreased (going from left to right for a set of bars). Finally, the benefits of MISE-QoS increase with increasing memory intensity because always prioritizing a memory intensive application will cause significant interference to other applications.

Based on our results, we conclude that MISE-QoS can effectively ensure that the AoI meets the specified slowdown bound while achieving high system performance and fairness across the other applications.

4.2. MISE-Fair: Minimizing Maximum Slowdown

The second mechanism we build on top of our MISE model is one that seeks to improve overall system fairness. Specifically, this mechanism attempts to minimize the maximum slowdown across all applications in the system. Ensuring that no application is unfairly slowed down while maintain-

ing high system performance is an important goal in multicore systems where co-executing applications are similarly important. Many prior works evaluate fairness in such scenarios in terms of the maximum slowdown of any application [13, 14, 42, 43, 92, 99, 100, 103].

At a high level, our mechanism works as follows. The memory controller maintains two pieces of information: 1) a target slowdown bound (*B*) for *all* applications, and 2) a bandwidth allocation policy that partitions the available memory bandwidth across all applications. The memory controller enforces the bandwidth allocation policy using a lottery-scheduling technique proposed in [105]. The controller attempts to ensure that the slowdown of all applications is within the bound *B*. To this end, it modifies the bandwidth allocation policy so that applications that are slowed down more get more memory bandwidth. Should the memory controller find that bound *B* is not possible to meet, it increases the bound. On the other hand, if the bound is easily met, it decreases the bound.

Interaction with the Operating System. As we will show in Section 4.2, our mechanism provides the best fairness compared to three state-of-the-art approaches for memory request scheduling [42, 43, 76]. In addition to this, there is another benefit to using our approach. Our mechanism, based on the MISE model, can accurately estimate the slowdown of each application. Therefore, the memory controller can potentially communicate the estimated slowdown information to the operating system (OS). The OS can use this information to make more informed scheduling and mapping decisions in order to further improve system performance or fairness. Since prior memory scheduling approaches do *not* explicitly attempt to minimize maximum slowdown by accurately estimating the slowdown of individual applications, such a mechanism to interact with the OS is *not* possible with them. Evaluating the benefits of the interaction between our mechanism and the OS is beyond the scope of this paper but is an important area of future work.

Evaluation. Figure 6 compares the system fairness (maximum slowdown) of different mechanisms with increasing number of cores. The figure shows results with four previously proposed memory scheduling policies (FRFCFS [89,122], ATLAS [42], TCM [43], and STFM [76]), and our proposed mechanism using the MISE model (MISE-Fair). We draw three conclusions from our results.

First, MISE-Fair provides the best fairness compared to all other previous approaches. The reduction in the maximum slowdown due to MISE-Fair when compared to STFM (the best previous mechanism) increases with increasing number of cores. With 16 cores, MISE-Fair provides 7.2% better fairness compared to STFM.

Second, STFM, as a result of prioritizing the most slowed down application, provides better fairness than all other previous approaches. While the slowdown estimates of STFM are not as accurate as those of our mechanism, they are good
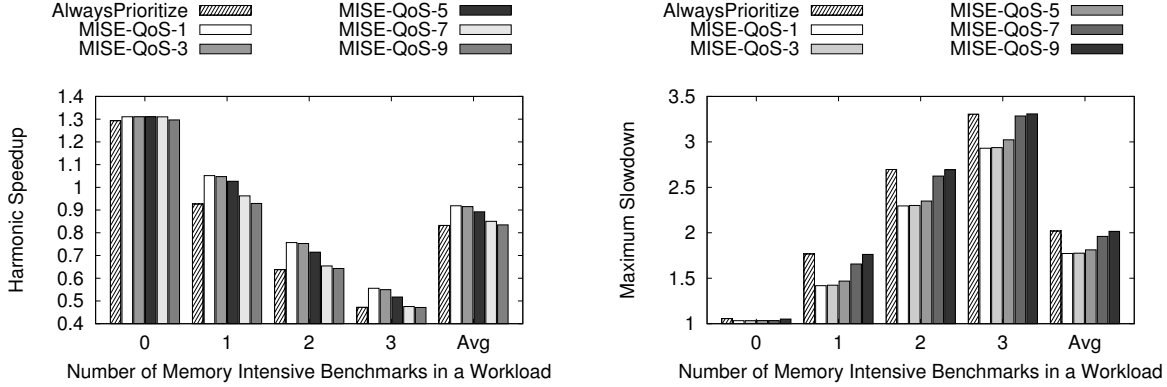
Figure 5: Average system performance and fairness across 300 workloads of different memory intensities. Reproduced from [97].
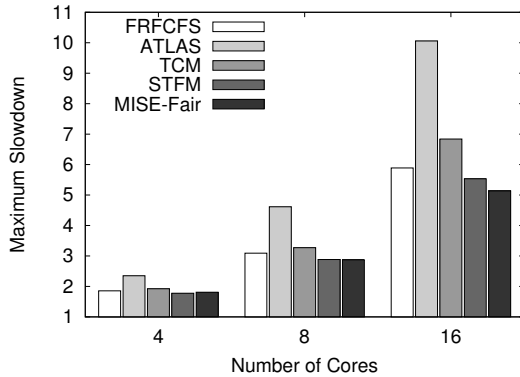

Figure 6: Fairness with different core counts. Reproduced from [97].

enough to identify the most slowed down application. However, as the number of concurrently-running applications increases, simply prioritizing the most slowed down application may not lead to better fairness. MISE-Fair, on the other hand, works towards reducing maximum slowdown by stealing bandwidth from those applications that are less slowed down compared to others. As a result, the fairness benefits of MISE-Fair compared to STFM increase with increasing number of cores.

Third, ATLAS and TCM are more unfair compared to FR-FCFS. As shown in prior work [42, 43], ATLAS trades off fairness to obtain better performance. TCM, on the other hand, is designed to provide high system performance and fairness. Further analysis showed us that the cause of TCM's unfairness is the strict ranking employed by TCM. TCM ranks all applications based on its clustering and shuffling techniques [43] and strictly enforces these rankings. We found that such strict ranking destroys the row-buffer locality of low-ranked applications. This increases the slowdown of such applications, leading to high maximum slowdown.[3]

We conclude that the MISE model's slowdown estimates can be used to design a better and more fair memory scheduler. We expect future works can take advantage of the MISE model

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[3]Note that this observation later led us to develop the Blacklisting Memory Scheduler (BLISS) [99, 100].

to design even better memory scheduling and other resource management mechanisms.

5. Related Work

To our knowledge, this is the first paper to 1) provide a *simple and accurate* model to estimate application slowdowns in the presence of main memory interference, and 2) use this model to devise two new memory scheduling techniques that either aim to satisfy slowdown bounds of applications or improve system fairness and performance. In this section, we discuss several related works. We discuss works that build upon MISE in Section 6.1.

Slowdown Estimation. Stall Time Fair Memory Scheduling (STFM) [76] attempts to estimate each application's slowdown, with the goal of improving fairness by prioritizing the most slowed down application. STFM estimates an application's slowdown as the ratio of its memory stall time when it is run alone versus when it is concurrently run alongside other applications. The challenge is in determining the alone stall time of an application *while* the application is actually running alongside other applications. STFM proposes to address this challenge by counting the number of cycles an application is stalled due to interference from other applications at the DRAM channels, banks and row-buffers. STFM uses this interference cycle count to estimate the alone-stall-time of the application, and hence the application's slowdown.

Fairness via Source Throttling (FST) [17] estimates application slowdowns due to inter-application interference at the shared caches and memory, as the ratio of uninterfered to interfered execution times. FST uses the slowdown estimates to make informed source throttling decisions, to improve fairness. The mechanism to account for memory interference to estimate uninterfered execution time is similar to that employed in STFM. Prefetch-Aware Shared Resource Management [19] extends the FST model to take into account prefetch requests.

A concurrent work by Du Bois et al. [15] proposes per-thread cycle accounting (PTCA) for multicore processors, which determines an application's standalone execution time when it shares cache and memory with other applications

in a multicore system. In order to quantify memory interference, PTCA counts the number of waiting cycles due to inter-application interference and factors out these waiting cycles to estimate alone execution times, which is similar to STFM's alone stall time estimation mechanism.

Eyerman and Eeckhout [23] and Cazorla et al. [5] propose mechanisms to determine an application's slowdown while it is running alongside other applications on an SMT processor. Luque et al. [68] estimate application slowdowns in the presence of shared cache interference. Lin and Balasubramonian [60] propose a regression-based model to estimate performance for different cache allocations. None of these studies take into account inter-application interference at the main memory. Therefore, MISE, which estimates slowdown due to main memory interference, can be combined with the above approaches to quantify interference at the SMT processor and shared cache to build a comprehensive mechanism.

Quality-of-Service (QoS). Several prior works provide QoS guarantees in shared memory CMP systems. Mars et al. [69] propose a mechanism to estimate an application's sensitivity towards interference and its propensity to cause interference. They utilize this knowledge to make informed mapping decisions between applications and cores. However, this mechanism 1) assumes *a priori* knowledge of applications, which may not always be possible to have, and 2) is designed for only 2 cores, and it is not clear how it can be extended to more than 2 cores. In contrast, MISE does not assume any *a priori* knowledge of applications and works well with large core counts, as we have shown in this paper. That said, MISE can possibly be used to provide feedback to the mapping mechanism proposed by [69] to overcome the shortcomings of their mechanism.

Iyer et al. [30, 33, 34] propose mechanisms to provide guarantees on shared cache space, memory bandwidth or IPC for different applications. The slowdown guarantee provided by MISE-QoS is stricter than these mechanisms as MISE-QoS takes into account the alone-performance of each application. Nesbit et al. [80] propose a mechanism to enforce a bandwidth allocation policy, by partitioning the available bandwidth across concurrently running applications based on some policy. While we use a scheduling technique similar to lottery-scheduling [85, 105] to enforce the bandwidth allocation policies of MISE-QoS and MISE-Fair, the mechanism proposed by Nesbit et al. can also be used in our proposal to allocate bandwidth instead of our lottery-scheduling approach.

Memory Interference Mitigation. Many prior works focus on the problem of mitigating inter-application interference at the main memory to improve system performance and/or fairness. Most of these approaches address memory interference by modifying the memory request scheduling algorithm [2, 18, 27, 32, 34, 42, 43, 50, 51, 52, 53, 72, 73, 76, 77, 80, 99, 100, 115, 117]. We quantitatively compare MISE-Fair to

STFM [76], ATLAS [42], and TCM [43] in Section 4.2, and show that MISE-Fair provides better fairness than these prior approaches.

Other works examine approaches such as sub-row interleaving [38], channel/bank partitioning [36, 64, 74, 109], bandwidth partitioning [61, 97], source throttling [3, 7, 17, 19, 39, 81, 82, 102], thread scheduling [14, 101, 106, 121], and changes to DRAM design [44, 58]. These approaches are complementary to MISE, and can be combined to achieve better fairness.

Prior Work on Analytical Performance Modeling. Prior works attempt to quantify the impact of cache/memory contention through offline profiling. Mars et al. [69] estimate an application's sensitivity/propensity to receive/cause interference. Other previous works propose to estimate an application's sensitivity to cache capacity [20, 91] and memory bandwidth [21] through profiling. Yang et al. [111] attempt to estimate applications' sensitivity to interference online. However, this work assumes that latency-critical applications run alone at times, when they can be profiled (which could degrade system throughput). These works assume the ability to profile (1) entire applications offline; or (2) specific execution scenarios, such as an application executing alone. In contrast, MISE can estimate the slowdown of any application *online*, in the general scenario of multiple applications running together.

Several previous works [24, 25, 37, 104] propose analytical models to estimate processor performance, as an alternative to time consuming simulations. The goal of our MISE model, in contrast, is to estimate slowdowns at runtime, in order to enable mechanisms to provide QoS and high fairness. Its use in simulation is possible, but is left to future work.

6. Significance

To our knowledge, our HPCA 2013 paper [97] is the first to build a *simple yet accurate* hardware-based model to estimate application slowdowns due to main memory interference online *with the goal of providing predictable performance*. Previous works [15, 17, 19, 76] propose mechanisms to estimate application slowdowns. However, these mechanisms are not accurate enough (as we demonstrate in Section 3) since they were not designed with the goal of providing predictable performance. Rather, the slowdown estimates were used to make prioritization/throttling decisions to improve overall fairness.

This work is also the first to design a hardware-based mechanism to i) provide soft guarantees on slowdown for applications and ii) detect when a prescribed slowdown bound is not being met, by leveraging slowdown estimates from the MISE model, while also improving overall system performance. Previous work [34], in the absence of a model to accurately estimate application slowdowns, always prioritizes the application that needs guaranteed performance, degrading the performance of other co-running applications. Furthermore, previous work also does not have the provision

to detect whether or not the prescribed slowdown bounds are being met (as we describe in Section 4).

6.1. Retrospective and Works Building on Our HPCA 2013 Paper

Adoption of the Principles of the MISE Model. The principles employed in the MISE model have been adopted towards slowdown estimation in several works that followed. The application slowdown model (ASM) [98], a follow-on work, builds on top of MISE's memory slowdown estimation model and extended it to take into account shared cache interference. In doing so, ASM also addressed one of the major caveats of the MISE model, the estimation of slowdown for non-memory-intensive applications. While MISE has a mechanism to address the slowdown of non-memory-intensive applications, this mechanism relies on the estimation of the memory-bound fraction of an application. Estimating the fraction of an application's execution that is memory bound, with high fidelity, is challenging. ASM addresses this challenge by applying the observation on request service rate as a proxy for performance at the input to the shared caches. This seamlessly enables slowdown estimation for applications with different memory and cache intensities/sensitivities. The ASM work shows that it can accurately estimate slowdowns with only 9.9% error across 100 workloads. We refer the reader to [98] for details.

A later work by Xiong et al. [110] proposes a slowdown estimation model that adopts the principle of giving an application highest priority in order to estimate its alone run behavior. This work directly measures alone-IPC during such high priority periods, rather than estimating alone request service rate and employs this alone-IPC estimate towards determining slowdown.

Applications of the MISE Model. The MISE model has been applied towards slowdown estimation in multiple contexts. Zhou and Wentzlaff [120] employ the MISE model in the context of throttling memory traffic at the source, based on inter-arrival times between requests. Specifically, they employ a set of bins, each corresponding to a range of inter-arrival times, and allocate a certain number of credits to each bin, depending on an application's request inter-arrival times. In order to determine the optimal credit allocation in different bins corresponding to different arrival times, they employ a genetic algorithm. This credit allocation determines the eventual number of requests that can be served corresponding to different inter-arrival times, for an application, and hence, shapes the memory traffic of the application. Slowdown estimates from the MISE model are leveraged to determine the optimal bins/credits configuration, to effectively shape memory traffic. Camouflage [119] employs the MISE model for the purposes of traffic shaping, but in the context of providing security. Camouflage shapes memory traffic into a predetermined distribution, in order to prevent attackers from probing the memory bus to infer the program's memory access and response patterns. Slowdown estimates from the MISE model are used to determine the optimal bins/credits configuration.

Employing Slowdown-Proportional Resource Allocation. The general principle of allocating resources proportionally, to the estimated slowdown at that resource is a key principle employed in the MISE-QoS and MISE-Fair schemes. Two prior works [66, 108] apply a similar principle in the context of addressing interference at the on-chip network. Towards mitigating on-chip network contention, they build a scheme that allocates channel bandwidth proportional to the aggregate rate of flow of traffic from each thread.

These works [66, 98, 110, 119, 120] are clear instances of the applicability of the MISE model itself and its principles in various contexts. The works that build on our original MISE paper [97] are strongly indicative of the potential impact this work could have in the long term, as we describe in the next section.

6.2. Long-Term Impact

Predictable Performance in Current and Future Systems. Building predictable systems is a grand research challenge [12, 75, 78]. Predictable performance is a key requirement in current and future systems where 1) multiple applications are consolidated onto the same machine, sharing resources *and* 2) some applications need a certain guaranteed performance. Data centers, virtualized systems, interactive mobile systems and real- time systems are all examples of scenarios where predictable performance is desirable or necessary. We expect the need for predictable performance to increase in the future as more systems will likely move towards consolidation as a means to effectively utilize resources. Given this trend, accurately quantifying the effect of shared resource interference on performance is an important enabler towards providing predictable performance. Therefore, we believe that slowdown estimates from the MISE model and the hardware/software techniques that can be built on top of our model are important steps towards providing predictable performance.

Request Service Rate a Proxy for Performance. One of the key ideas behind MISE is to use memory request service rate as a proxy for performance for memory-bound applications. We hypothesize that the performance of an application that is bottlenecked at a certain resource is likely correlated with the request service rate at that resource. Hence, the notion of using request service rate as a proxy for performance can be used as a primitive for performance prediction and applied more generally to other shared resources such as shared caches, storage and network. ASM [98], described in Section 6.1, is one such work that takes advantage of this key idea of request service rate as a proxy for performance, measured at the shared caches.

Accurate and Efficient Estimation of Alone Performance. Another key idea behind MISE is to periodically give each application the highest priority in order to estimate

alone-request-service-rate. In doing so, the highest priority application receives minimal interference when its slowdown is being estimated, while also not disrupting other applications' execution. This leads to better accuracy than previous work [15, 17, 19, 76] that estimates an application's slowdown *while* it is receiving interference from other applications. We believe that the principle of estimating slowdown while using techniques such as prioritization to minimize interference can be applied at other shared resources such as I/O, storage and network as well.

Enabling Better Resource Management. The ability to accurately estimate slowdown in the presence of shared resource interference can enable a range of resource management techniques to provide QoS in both hardware and software. Slowdown estimates can be leveraged in the hardware for resource management (as we demonstrate with memory bandwidth). Slowdown estimates can also be communicated to the software, enabling more effective and informed admission control and migration mechanisms across a cluster of machines. Therefore, we believe MISE's slowdown estimates can enable substantial future research on resource allocation policies.

Simplicity of the Technique. The MISE model requires only simple hardware changes to the memory controller and scheduling logic, while providing high accuracy. By virtue of the memory bandwidth partitioning scheme we employ, the memory scheduler only needs to give one application the highest priority at any point in time, while treating other applications' requests similarly. On the other hand, previously proposed memory scheduling policies such as ATLAS, TCM [42, 43] employ ranking policies where an ordered ranking is enforced across all applications' requests. Hence, MISE requires simpler comparator logic compared to previous proposals and can be more easily incorporated into today's memory controllers than previous proposals.

Applicability to Other Memory Technologies. In our HPCA 2013 paper [97], we described MISE within the context of a system using DRAM as main memory, for which the reader can find detailed background information in our prior works [6, 8, 9, 10, 28, 29, 40, 41, 42, 43, 44, 45, 54, 55, 56, 57, 58, 62, 63, 83, 93, 94]. We believe the principles of MISE are easily applicable to other memory technologies, e.g., phase-change memory [47, 48, 49, 87, 107, 112, 118], STT-MRAM [46, 70, 79], and hybrid memory systems [1, 4, 11, 16, 26, 59, 65, 70, 71, 84, 86, 87, 88, 113, 114, 116]. We leave a detailed exploration of these to future works.

7. Conclusion

Application slowdowns induced by memory interference are a significant deterrent to high and predictable performance. Towards tackling such application slowdowns, our HPCA 2013 paper [97] (1) builds a simple Memory Interference-induced Slowdown Estimation (MISE) model to accurately estimate application slowdowns, and (2) demon-

strates two use cases that leverage our MISE model to achieve predictable performance and fairness. Since our original HPCA 2013 paper [97] on the MISE model and its applications, several works have adopted and employed the MISE model and its principles in different contexts. We conclude that the MISE model and the principles behind it can fuel and inspire many more such works on high performance, predictable, and fair memory systems.

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