Pulse Shaping and Clock Data Recovery for Multi-Gigabit Standard Compliant 60 GHz Digital Radio

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***Abstract* — This paper presents the first ultra low power (5 mW) multi-gigabit pulse-shaping filter and clock data recovery circuits fully integrated in a 90-nm CMOS wireless digital radio meeting the specifications of 60 GHz wireless standards. The architecture features a 4.4 Gsps capable 13-tap FIR pulse shaping filter on the TX side, and a dual loop clock data recovery with on-chip loop filter on the RX side to suppress the high frequency jitter introduced by the pulse shaping. Using a fully integrated 60 GHz TDD transceiver embedding the presented solution, a 95% reduction of the high frequency jitter has been measured at the standard nominal 1.728 Gbps data rate. The solution features a minimal power overhead of 5 mW from 1 V voltage supply.**

***Index Terms* — 60GHz, CMOS, 90nm, transceivers, pulse shaping circuits, phase locked loops.**

I. Introduction

Wireless communications standards addressing the use of the unlicensed 57 to 66 GHz band are rapidly converging with the effort of several organizations (ISO-DS13156 [1], ECMA 387 [2], IEEE 802.15.3c, IEEE 802.11.ad…). Recently, several fully integrated CMOS 60 GHz transceivers have been presented [3-6], but little details have been provided on how to address the challenge of meeting the frequency plan and spectral mask requirement in each wireless channel in these specific standards. Considering the very limited power budget for battery operated portable consumer electronics, the conventional pulse shaping techniques cannot meet the data rate and power consumption specifications for multi-gigabit wireless applications, which require more efficient spectral compression by means of complex modulation schemes or ultra low power pulse shaping.

This paper presents the first ultra low power (5 mW) pulse shaping and clock data recovery solution integrated in a multi gigabit wireless standard compliant 60 GHz transceiver. The solution incorporates an ultra low power multi gigabit 13-tap digital pulse shaping filter in the transmitter. On the receiver side it includes a linear clock data recovery (CDR) circuit with fully integrated loop filter and embedded programmable digital lock detect algorithm. The solution has been incorporated into a 90-nm CMOS fully integrated 60 GHz single-chip radio that includes, for the first time, digital-to-analog/analog-to-digital conversion and embedded multi gigabit mixed-signal modem solution requiring no external baseband processing. The solution has been validated by measured results and it meets the ISO and IEEE standard spectral mask requirements.

This paper is organized as follows. In section II the overall transceiver architecture is presented. In section III the transmitter side pulse shaping 13-tap FIR filter is described, while section IV deals with the clock and data recovery circuit embedded in the receiver. Section V presents the measured results over the 60 GHz wireless link, while in section VI the conclusions are drawn.

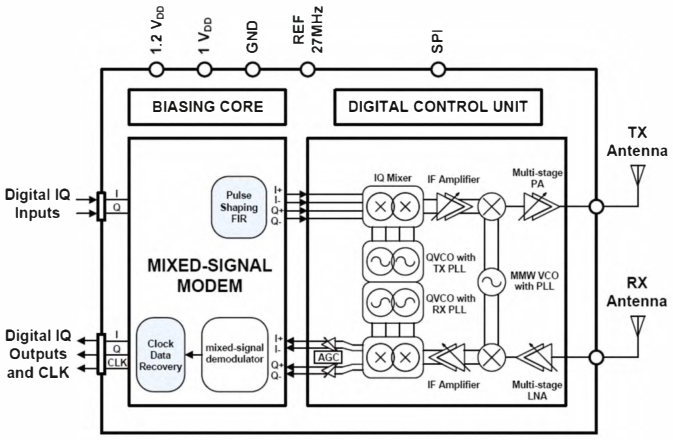
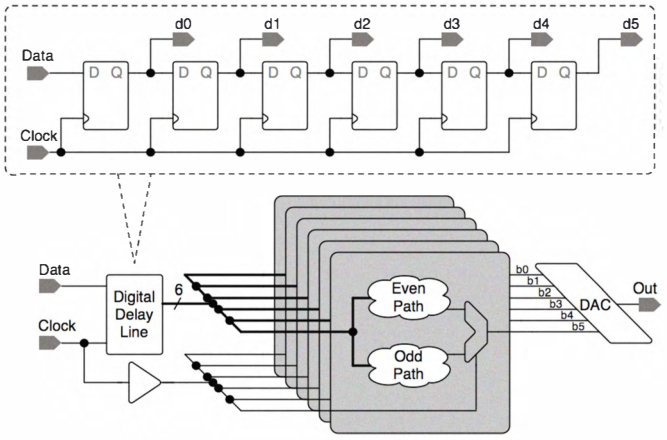


Fig. 1. Overall 60 GHz transceiver architecture.

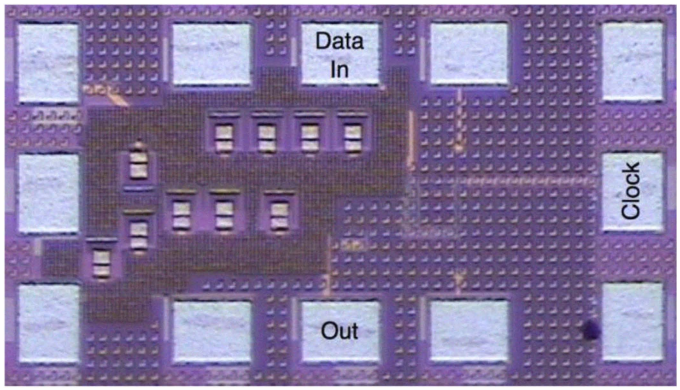
II. 60 GHz Transceiver Architecture

A simplified block diagram of the integrated 60 GHz single-chip CMOS 90 nm digital radio is shown in Fig. 1. The transmitter incorporates a baseband processor including multi-gigabit digital PHY processing, pulse shaping filters, and DAC. The transmitter up-converts the baseband to about 13 GHz intermediate frequency (IF) using the IQ mixer and the QVCO, then to 60 GHz using the millimeter wave mixer and a VCO generating the local oscillator (LO) signal. The receiver down-converts the pass-band signal using the same frequency plan and demodulates the data with an embedded multi gigabit mixed-signal demodulator. To perform the digital baseband signal processing, the clock is recovered from the demodulated data with the dual loop CDR. The high frequency jitter introduced by the pulse shaping and by the wireless channel is

filtered out by the CDR block, which re-samples the I/Q digital data as well.



(a)

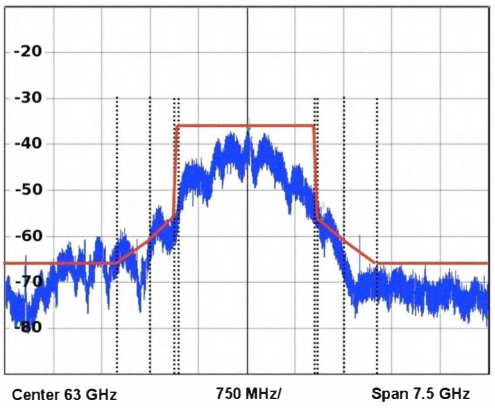


(b)

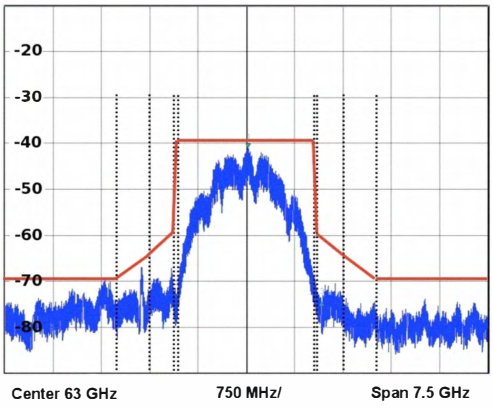
Fig. 2. (a) Pulse shaping filter implementation. (b) Pulse shaping filter test structure.

III. Pulse Shaping

On the transmitter side the baseband data is pulse-shaped using a 13-tap raised cosine look-up table based FIR digital filter with a roll-off factor of 0.25 and an oversampling factor of 2. The tap coefficients are: [0.0000, 0.0866, -0.0000, -0.1856, 0.0000, 0.6274, 1.0000, 0.6274, 0.0000, -0.1856, -0.0000, 0.0866, 0.0000]. The implementation of the FIR filter is shown in Fig. 2(a). Oversampling by a factor of 2, by definition, introduces a zero in between every two samples. This implies that at any given time, either all even coefficients are being multiplied by zeroes or all the odd coefficients are being multiplied by zeroes. This enables the implementation of the high-speed pulse shaping filter in an interleaved manner, with two parallel paths (namely even path and odd path) that are combined only at the very end before the digital-to-analog conversion by utilizing a parallel-to-serial converter. The pulse shaping filter uses a 6-bit DAC and hence has 6 implementations of even and odd paths. Since there is only one non-zero coefficient in the odd set, the output of this path can assume just two different values. However, the output of the even path can be anyone of the 2^6 possible outcomes since there are 6 non-zero even coefficients. To run at extremely high speed, all the possible 2^6 outcomes are pre-calculated and stored in a look-up table at addresses representing the last 6 data inputs. To run at high speed and very low power consumption, this memory block is implemented as a combinational logic block with the 6 address bits as inputs and a pair of outputs for each DAC bit representing the even and odd paths. For a nominal rate of 1.728 Gbps, the presented pulse-shaping filter operates at 3.456 GS/s, and consumes only 4 mA from 1 V voltage supply, while the measured maximum operating speed is 4.4 Gbps (8.8 GS/s). The measured output spectra of the pulse shaping filter after 60 GHz up-conversion are shown in Fig. 3 for 1.728 Gbps data rate. The ISO and IEEE spectral mask is reported as well.



(a)



(b)

Fig. 3. Measured output spectrum of the 60 GHz transmitted signal at 1.728 Gsps (a) without pulse shaping and (b) with pulse shaping. ISO and IEEE mask is indicated in red.

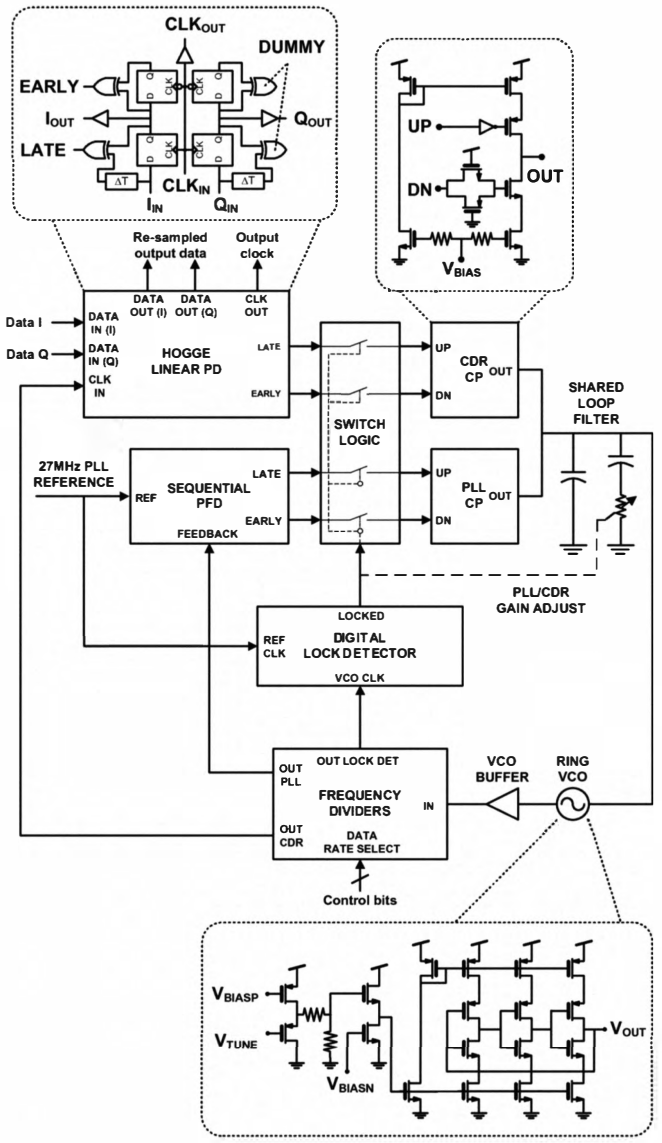


Fig. 4. Block level diagram of the clock and data recovery embedded in the receiver.

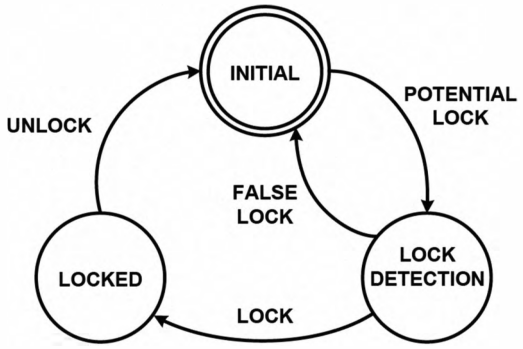


Fig. 5. Lock detection algorithm description using signal flow graph.

IV. Clock and Data Recovery

The CDR architecture is shown in Fig. 4. The system features a linear Hogge phase detector based type-2 third-order dual loop (frequency/phase detection) architecture. Two charge pumps with complementary tri-state outputs share the same loop filter in current mode. Initially, the frequency loop (employing the sequential PFD) recovers the frequency error using the 27 MHz external reference. Then, the CDR loop (employing the Hogge linear PD) takes over and locks on the I/Q input data stream. The frequency loop features 2 MHz bandwidth while the CDR loop bandwidth is 5 MHz.

As shown in Fig. 4, the CDR system employs a three-stage current starved VCO featuring very low power consumption (1 mW total from 1 V supply). The input complementary source follower buffer is used to enhance the linearity of the control characteristic and to reduce the VCO gain to about 2 GHz/V. The measured phase noise of the VCO is -82 dBc/Hz at 1 MHz offset from the carrier. Given the nominal operating frequency of 1.728 GHz, it has been possible to implement the frequency dividers using a standard digital cell approach. To support multiple data rates (1.728/1.485/0.864 Gbps) the PLL division ratio can be set to either 64 or 55, while the CDR loop division ratio can either be 1 or 2.

In the event of an excessively long run of consecutive bits of the same value or in the absence of a transmitted signal, the leakage current from the loop filter output node would cause the VCO control voltage to drift, causing the VCO output frequency to fall outside the lock-in range of the CDR loop. To overcome this issue an innovative integrated digital lock detector implementing the control algorithm has been designed, and its working principle is illustrated in Fig. 5. Upon initialization, the lock detector finite-state machine leaves the INTIAL state and waits in the LOCK DETECTION state until the VCO output cycles falling within 1 reference cycle are within a *fine tolerance* (±1 cycle) from the nominal 64 cycles. When the above condition has been met 5 times in a row, the state changes to LOCKED and the control is given to the phase loop and the frequency loop remains disabled as long as the VCO cycles are within a *coarse* tolerance (±2 cycles) from the nominal value. The coarse tolerance is twice the fine tolerance to accommodate short data runs. If the coarse tolerance is violated at least 3 times in a row, the frequency mismatch between the VCO output and the nominal data rate is assumed to fall outside the lock-in range of the CDR loop and the control is given back to the frequency loop by starting over from the algorithm from the INITIAL state.

The CDR with the lock detector achieves lock within ±50MHz around the nominal data rate of 1.728 Gbps. When operating at the nominal data rate of 1.728 Gbps, the overall CDR and lock detector power consumption is 5 mW from a 1 V voltage supply, while the CDR area including the on-chip loop filter is 130x360 μm^2, which represents, to the author's knowledge, the smallest die area and power consumption reported to date in similar works in the recent literature [7-9].

V. Measured Results

The pulse shaping FIR filter and the CDR have been tested independently and as part of a 60 GHz wireless link. The link has been implemented using the fully integrated CMOS 90 nm 60 GHz digital radio including the baseband signal processor described in section II. The complete integrated transceiver occupies 2.5x2.5 mm^2 and it is shown in Fig. 6. A 2^{31}-1 PRBS source has been used to generate the 1.728 Gbps baseband stream and to measure the bit-error-rate (BER). The following measurement results are relative to the transmission over a 1.5 m wireless link with the transceiver achieving a BER<10^{-11}. Given the data rate and the limited time over which the measurement has been taken, the achieved BER represents error-free transmission. The pulse shaping filter has been applied to the incoming data stream and observed after demodulation at the receiver end with and without CDR. The resulting eye diagrams are shown in Fig. 7. Without CDR the demodulated data stream is affected by a peak-to-peak jitter of 450 ps, mainly due to the pulse shaping. After enabling the CDR the peak-to-peak jitter is reduced to 50 ps, thus demonstrating the effectiveness of the proposed approach. Disabling the lock detector, the CDR fails to lock unless the VCO frequency is brought in close proximity of the data rate by manually handling the PLL/CDR handover, therefore demonstrating the validity of the lock detection algorithm.

VI. Conclusion

This work represents the first successful demonstration of an ultra low power (5 mW) pulse shaping and clock data recovery solution integrated in a 60 GHz single chip CMOS 90 nm digital radio, and tested in a 60 GHz point-to-point wireless link. The experimental setup confirmed the validity of the proposed solution featuring standard compatible error-free 1.728 Gbps data transmission a distance of 1.5 m.

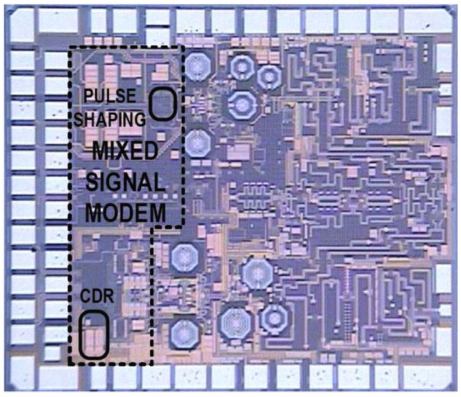


Fig. 6. Photo of the fully integrated 60 GHz single-chip CMOS 90 nm digital radio with embedded multi-gigabit mixed-signal modem solution, highlighting the CMOS pulse shaping and clock data recovery blocks.

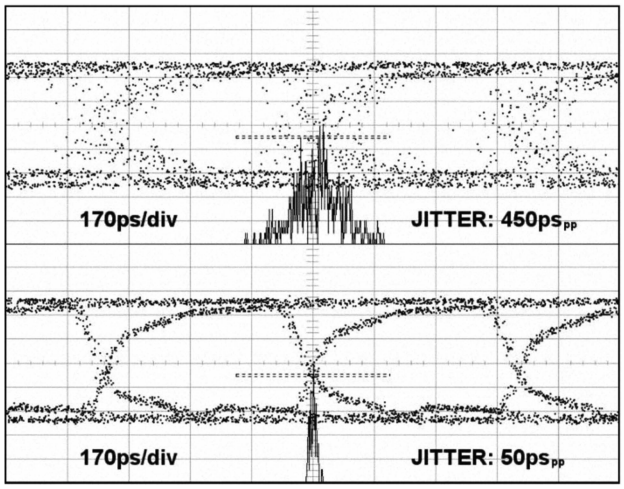


Fig. 7. Measured eye diagrams and histograms of the received baseband data after pulse shaping: without CDR (top), and with CDR (bottom).

Acknowledgement

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