IMPLEMENTATION OF BOOLEAN LOGIC IN FPGA

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Abstract

To Obtain the Boolean Expression for the Logic circuit shown below

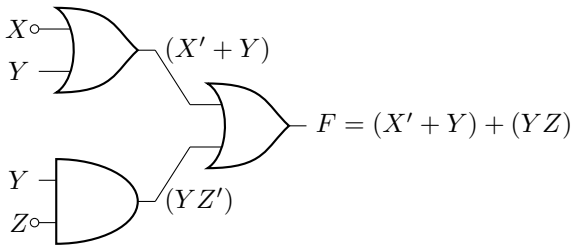

Fig. 1

1 Components

Components	Values	Quantity
Vaman		1
JumperWires	M-F	5
Breadboard		1
USB-C cable		1

2 Setup

1. Connect the Vaman to the Laptop through USB.
2. There is a button and an LED to the left of the USB port on the Vaman.There is another button to the right of the LED.
3. Press the right button first and immediately press the left button.The LED will be blinking green.The Vaman is now in bootloader mode.

2.1 Steps for implementation

1. Login to termux-ubuntu on the android device and execute the following commands:
   Make sure that the required installation and tool builds of pygmy-sdk had done prior executing below commands

```
proot−distro login debian
cd /data/data/com.termux/files/home/
mkdir fpga
svn co https://github.com/dudekulauseni123/
    Module1/trunk/fpga/codes
cd codes
ql_symbiflow −compile −src /data/data/com.termux
    /files/home/fpga/codes −d ql−eos−s3 −P
    PU64 −v helloworldfpga.v −t helloworldfpga −p
     quickfeather.pcf −dump binary
```

   This will generate **helloworldfpga.bin** file in codes directory transfer this bin file to laptop by executing the following command

```
scp /data/data/com.termux/files/home/fpga/codes/
    helloworldfpga.bin username_of_pc@IP_address:/
    home/username
```

   Make sure that the appropriate username,IP address of the Laptop is given in the above command.

2. Now execute the following commands on the Laptop terminal
   Make sure that required installation of programmer application had done prior executing below command

```
python3 /home/username/TinyFPGA−Programmer−
    Application/tinyfpga−programmer−gui.py −−
    port /dev/ttyACM0 −−appfpga /home/
    username/helloworldfpga.bin −−mode fpga
```

3. After finishing the process of flashing with the programmer application press the button to the right of the USB port to reset. Vaman is now flashed with our source code

3 Implementation

The truth table for Fig. 1 is available in Table-1 Using Boolean logic, output F in Table 1 can be expressed in terms of the inputs X, Y, Z as F=(X'+Y)+(Y.Z').....(2.1)

Karnugh Map : The expression in (2.1) can be minimized using the K-map in Fig 2. In Fig.2 ,the implicants in boxes 0,1,2,3 result in X' The implicants in boxes 2,3,6,7 result in Y Thus, after minimization using Fig. 2, (2.1) can be expressed as F=X'+ Y.....(2.2). Verify the truth table for F in TABLE 1.

[4][2][1][YZ][X] 0,1,2,3,6,7 4,5 02 36

X	Y	Z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Table-1

Fig. 2

2,4,6 GPIO Pins of J3 Bank in Vaman Board are configured as input pins and the required Logic for X,Y,Z are drawn from 5V (Digital '1'),GND (Digital '0'). Built in led will glow based on F satisfying the Table-1

Input variables	**IO PIN**	**QFN**
X	IO2	6
Y	IO4	3
Z	IO6	62

Output variable	**IO PIN**	**QFN**
F	IO18	38

The code below realizes the Boolean logic for F in (2.2) using 5V,GND of Vaman Board using Verilog Language

https://github.com/dudekulauseni123/Module1/blob/main/fpga/codes/helloworldfpga.v